Enhanced ESD, 8Mbps Dual-Channel Digital Isolators

Data Sheet

Pai12xSxxC

FEATURES

- **Maximum data rate: 8Mbps**
- **High common-mode transient immunity: 100 kV/μs**
- **High robustness to radiated and conducted noise**
- **Low idle current: 0.6mA/side**
- **High ESD rating:**
  - **Human body model (HBM): ±8kV**
  - **Charged device model (CDM): ±2kV**
- **Safety and regulatory approvals：**
  - **UL certificate number: Pending**
    - **3.75kV$_{RMS}$ for 1 minute per UL 1577, -SR device**
    - **5.7kV$_{RMS}$ for 1 minute per UL 1577, -W5R device**
    - **5.7kV$_{RMS}$ for 1 minute per UL 1577, -W1R device**
  - **CSA Component Acceptance Notice 5A**
  - **VDE certificate number: Pending**
    - **DIN VDE V 0884-17:2021-10**
    - **V_{IORM} = 637V_{Peak}, -SR device**
    - **V_{IORM} = 2121V_{Peak}, - W5R device**
    - **V_{IORM} = 2121V_{Peak}, -W1R device**
  - **CQC certification per GB4943.1-2011**
- **3V to 5.5V level translation**
- **Wide temperature range: -40°C to 125°C**
- **AEC-Q100 qualification**
- **RoHS-compliant, NB SOIC-8, WB SOIC-8 and WB SOIC-16 package**

APPLICATIONS

- **General-purpose multichannel isolation**
- **Industrial field bus isolation**
- **Isolation Industrial automation systems**
- **Isolated switch mode supplies**
- **Isolated ADC, DAC**
- **Motor control**

GENERAL DESCRIPTION

The Pai1xxxxxC is a 2PaiSemi digital isolators product family that includes over hundreds of digital isolator products. By using maturated standard semiconductor CMOS technology and 2PaiSemi ***iDivider®*** technology, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators.

Intelligent voltage divider technology (***iDivider®*** technology) is a new generation digital isolator technology invented by 2PaiSemi. It uses the principle of capacitor voltage divider to transmit voltage signal directly cross the isolator capacitor without signal modulation and demodulation.

The Pai1xxSxC isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 5.7kV$_{RMS}$ and the data rate from DC up to 8Mbps. The devices operate with the supply voltage on either side ranging from 3.0V to 5.5V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. The fail-safe state is available in which the outputs transition to a preset state when the input power supply is not applied. For example, if input power loses, the output will be logic high for Pai1xxSx1C and logic low for Pai1xxSx0C.

Compared to the old π1xxUxx series, Pai1xxSxxC digital isolators can provide lower propagation delay, higher data rate and better system-level ESD performance.

FUNCTIONAL BLOCK DIAGRAMS

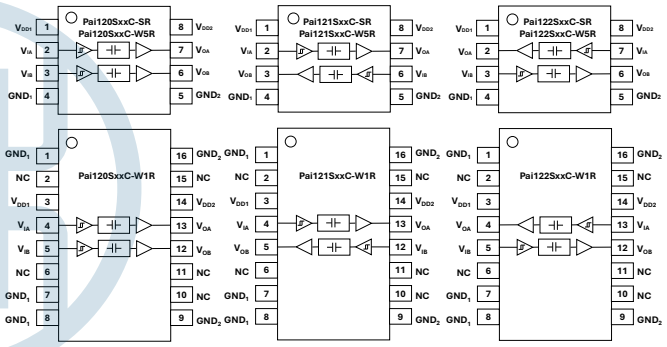


Figure 1.Pai120SxxC/Pai121SxxC/Pai122SxxC functional Block Diagram

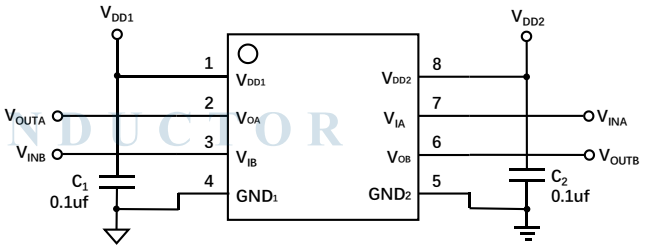


Figure 2.Pai122xxxC Typical Application Circuit

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Floor 2, Building 28, No.498, Guoshoujing Road , Pudong New District, Shanghai, 201203, China
021-50850681
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PIN CONFIGURATIONS AND FUNCTIONS

Table 1. Pai120S3xC-SR/Pai120S6xC-W5R Pin Function Descriptions

Pin No.	Name	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

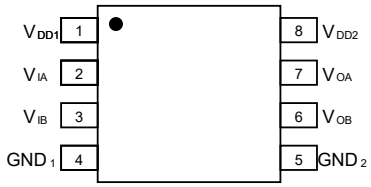


Figure 3. Pai120S3xC-SR/ Pai120S6xC-W5R Pin Configuration

Table 2. Pai121S3xC-SR/Pai121S6xC-W5R Pin Function Descriptions

Pin No.	Name	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{OB}	Logic Output B.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V_{IB}	Logic Input B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

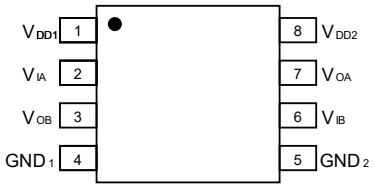


Figure 4. Pai121S3xC-SR/ Pai121S6xC-W5R Pin Configuration

Table 3. Pai122S3xC-SR/Pai122S6xC-W5R Pin Function Descriptions

Pin No.	Name	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{OA}	Logic Output A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{IA}	Logic Input A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

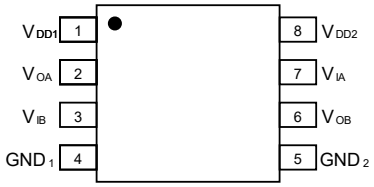


Figure 5. Pai122S3xC-SR/Pai122S6xC-W5R Pin Configuration

Table 4.Pai120S6xC-W1R Pin Function Descriptions

Pin No.	Name	Description
1	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
2	NC	No connect.
3	V_{DD1}	Supply Voltage for Isolator Side 1.
4	V_{IA}	Logic Input A.
5	V_{IB}	Logic Input B.
6	NC	No Connect.
7	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
8	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC	No Connect.
11	NC	No Connect.
12	V_{OB}	Logic Output B.
13	V_{OA}	Logic Output A.
14	V_{DD2}	Supply Voltage for Isolator Side 2.
15	NC	No Connect.
16	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.

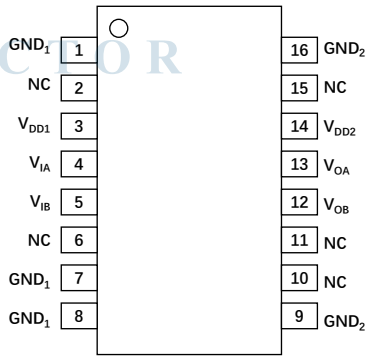


Figure 6.Pai120S6xC-W1R Pin Configuration

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Table 5.Pai121S6xC-W1R Pin Function Descriptions

Pin No.	Name	Description
1	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
2	NC	No Connect.
3	V_{DD1}	Supply Voltage for Isolator Side 1.
4	V_{IA}	Logic Input A.
5	V_{OB}	Logic Output B.
6	NC	No Connect.
7	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
8	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC	No Connect.
11	NC	No Connect.
12	V_{IB}	Logic Input B.
13	V_{OA}	Logic Output A.
14	V_{DD2}	Supply Voltage for Isolator Side 2.
15	NC	No Connect.
16	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.

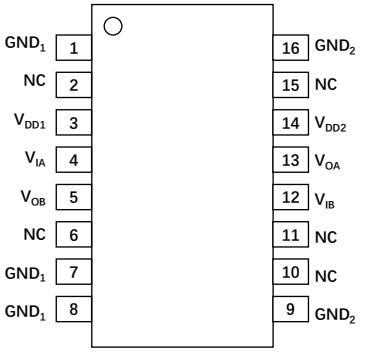


Figure 7.Pai121S6xC-W1R Pin Configuration

Table 6.Pai122S6xC-W1R Pin Function Descriptions

Pin No.	Name	Description
1	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
2	NC	No Connect.
3	V_{DD1}	Supply Voltage for Isolator Side 1.
4	V_{OA}	Logic Output A.
5	V_{IB}	Logic Input B.
6	NC	No Connect.
7	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
8	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC	No Connect.
11	NC	No Connect.
12	V_{OB}	Logic Output B.
13	V_{IA}	Logic Input A.
14	V_{DD2}	Supply Voltage for Isolator Side 2.
15	NC	No Connect.
16	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.

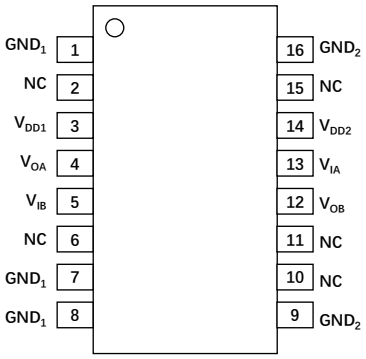


Figure 8.Pai122S6xC-W1R Pin Configuration

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.Absolute Maximum Ratings[4]

Parameter	Rating
Supply Voltages (V_{DD1}-GND_1, V_{DD2}-GND_2)	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB})[1]	−0.5 V to V_{DDx} + 0.5 V
Output Voltages (V_{OA}, V_{OB})[1]	−0.5 V to V_{DDx} + 0.5 V
Average Output Current per Pin[2] Side 1 Output Current (I_{O1})	−10 mA to +10 mA
Average Output Current per Pin[2] Side 2 Output Current (I_{O2})	−10 mA to +10 mA
Common-Mode Transients Immunity [3]	−200 kV/µs to +200 kV/µs
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C

Notes:

[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

[2] See *Figure 9* for the maximum rated current values for various temperatures.

[3] See *Figure 20* for Common-mode transient immunity (CMTI) measurement.

[4] Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 8.Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DDx} [1]	3		5.5	V
High Level Input Signal Voltage	V_{IH}	0.6*V_{DDx}[1]		V_{DDx}[1]	V
Low Level Input Signal Voltage	V_{IL}	0		0.3*V_{DDx}[1]	V
High Level Output Current	I_{OH}	-6			mA
Low Level Output Current	I_{OL}			6	mA
Data Rate		0		8	Mbps
Junction Temperature	T_J	-40		150	°C
Ambient Operating Temperature	T_A	-40		125	°C

Notes:

[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

Truth Tables

Table 9.Pai12xSxxC Truth Table

V_{Ix} Input[1]	V_{DDI} State[1]	V_{DDO} State[1]	Default Low	Default High	Test Conditions /Comments
			V_{Ox} Output[1]	V_{Ox} Output[1]	
Low	Powered[2]	Powered[2]	Low	Low	Normal operation
High	Powered[2]	Powered[2]	High	High	Normal operation
Open	Powered[2]	Powered[2]	Low	High	Default output
Don't Care[4]	Unpowered[3]	Powered[2]	Low	High	Default output[5]
Don't Care[4]	Powered[2]	Unpowered[3]	High Impedance	High Impedance	

Notes:

[1] V_{Ix}/V_{Ox} are the input/output signals of a given channel (A or B). V_{DDI}/V_{DDO} are the supply voltages on the input/output signal sides of this given channel.

[2] Powered means V_{DDx}≥ 2.95 V

[3] Unpowered means V_{DDx} < 2.30V

[4] Input signal (V_{Ix}) must be in a low state to avoid powering the given V_{DDI}[1] through its ESD protection circuitry.

[5] If the V_{DDI} goes into unpowered status, the channel outputs the default logic signal after around 1us. If the V_{DDI} goes into powered status, the channel outputs the input status logic signal after around 5us.

SPECIFICATIONS

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ELECTRICAL CHARACTERISTICS

Table 10.Pai12xSxxC Switching Specifications

V_{DD1} - GND_1 = V_{DD2} - GND_2 = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, C_L = 0pF and parasitic capacitance (C_p) is 10pF, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Pulse Width	PW	0.125			µs	
Data Rate		DC		8	Mbps	Under certain test condition[5]
Propagation Delay Time[1]	t_{pHL}, t_{pLH}		0.05	0.2	µs	@ 5V_{DC} supply
			0.05	0.2	µs	@ 3.3V_{DC} supply
Pulse Width Distortion	PWD		0.03	0.1	µs	The max different time between t_{pHL} and t_{pLH}@ 5V_{DC} supply. And The value is | t_{pHL} - t_{pLH} |
			0.03	0.1	µs	The max different time between t_{pHL} and t_{pLH}@ 3.3V_{DC} supply. And The value is | t_{pHL} - t_{pLH} |
Output Signal Rise Time[4]	t_r		1.5	5	ns	See *Figure 12*
Output Signal Fall Time[4]	t_f		1.5	5	ns	See *Figure 12*
Common-Mode Transient Immunity[3]	CMTI		100		kV/µs	V_{IN} = V_{DDx}[2] or 0V, V_{CM} = 1000V.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ESD[5]	HBM		±8		kV	Human body model, ESDA/JEDEC JS-001-2024
	CDM		±2		kV	Charged device model, ESDA/JEDEC JS -002-2022
	System[6]		±8		kV	Contact discharge per IEC 61000-4-2; Isolation barrier withstand test

Notes:

[1] t_{pLH} = low-to-high propagation delay time, t_{pHL} = high-to-low propagation delay time. See *Figure 13*.

[2] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

[3] See *Figure 20* for Common-mode transient immunity (CMTI) measurement. Not tested in production, guaranteed by design.

[4] t_r means is the time from 10% amplitude to 90% amplitude of the rising edge of the signal, t_f means is the time from 90% amplitude to 10% amplitude of the falling edge of the signal. Not tested in production, guaranteed by design.

[5] Only one channel is activated at the same time, 100% tested at production.

[6] IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device. Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

Table 11.DC Specifications

V_{DD1} - GND_1 = V_{DD2} - GND_2 =3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Rising Input Signal Voltage Threshold	V_{IT+}		0.5*V_{DDx}[1]	0.6*V_{DDx}[1]	V	
Falling Input Signal Voltage Threshold	V_{IT-}	0.3* V_{DDX}[1]	0.35* V_{DDX}[1]		V	
High Level Output Voltage	V_{OH}	V_{DDx} – 0.1	V_{DDx}		V	−20 µA output current
		V_{DDx} – 0.2	V_{DDx} – 0.1		V	−2 mA output current
Low Level Output Voltage	V_{OL}		0	0.1	V	20 µA output current
			0.1	0.2	V	2 mA output current
Input Current per Signal Channel	$\|I_{IN}\|$[2]	0	2	10	µA	0 V ≤ Signal voltage ≤ V_{DDX}[1]
V_{DDx}[1] Undervoltage Rising Threshold	V_{DDxUV+}	2.45	2.7	2.95	V	
V_{DDx}[1] Undervoltage Falling Threshold	V_{DDxUV-}	2.3	2.6	2.8	V	
V_{DDx}[1] Hysteresis	V_{DDxUVH}		0.15		V	

Notes:

[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2. The direction of the input current is related to the fail-safe output state.

[2] High fail-safe output state devices have a pull-up input current and low fail-safe output state devices have a pull-down input current.

Table 12.Quiescent Supply Current

V_{DD1} - GND_1 = V_{DD2} - GND_2 = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, C_L = 0pF and parasitic capacitance (C_p) is 10pF, unless otherwise noted.

Part	Symbol	Min	Typ	Max	Unit	Test Conditions	
						Supply voltage	Input signal
Pai120SxxC	$I_{DD1 (Q)}$	0.10	0.28	0.50	mA	5V_{DC}	VI=0V for Pai12xSx0C VI=5V for Pai12xSx1C
	$I_{DD2 (Q)}$	0.33	0.63	1.04	mA		
	$I_{DD1 (Q)}$	0.14	0.34	0.59	mA		VI=5V for Pai12xSx0C VI=0V for Pai12xSx1C
	$I_{DD2 (Q)}$	0.34	0.63	1.05	mA		
	$I_{DD1 (Q)}$	0.06	0.23	0.41	mA	3.3V_{DC}	VI=0V for Pai12xSx0C VI=3.3V for Pai12xSx1C
	$I_{DD2 (Q)}$	0.32	0.62	1.02	mA		
	$I_{DD1 (Q)}$	0.08	0.26	0.47	mA		VI=3.3V for Pai12xSx0C VI=0V for Pai12xSx1C
	$I_{DD2 (Q)}$	0.33	0.62	1.03	mA		
Pai121SxxC	$I_{DD1 (Q)}$	0.46	0.79	1.66	mA	5V_{DC}	VI=0V for Pai12xSx0C VI=5V for Pai12xSx1C
	$I_{DD2 (Q)}$	0.32	0.73	1.20	mA		
	$I_{DD1 (Q)}$	0.44	0.76	1.25	mA		VI=5V for Pai12xSx0C VI=0V for Pai12xSx1C
	$I_{DD2 (Q)}$	0.41	0.74	1.22	mA		
	$I_{DD1 (Q)}$	0.39	0.74	1.44	mA	3.3V_{DC}	VI=0V for Pai12xSx0C VI=3.3V for Pai12xSx1C
	$I_{DD2 (Q)}$	0.31	0.69	1.14	mA		
	$I_{DD1 (Q)}$	0.40	0.72	1.19	mA		VI=3.3V for Pai12xSx0C VI=0V for Pai12xSx1C
	$I_{DD2 (Q)}$	0.38	0.70	1.15	mA		

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Part	Symbol	Min	Typ	Max	Unit	Test Conditions	
						Supply voltage	Input signal
Pai122SxxC	$I_{DD1 (Q)}$	0.46	0.79	1.66	mA	$5V_{DC}$	VI=0V for Pai12xSx0C VI=5V for Pai12xSx1C
	$I_{DD2 (Q)}$	0.32	0.73	1.20	mA		
	$I_{DD1 (Q)}$	0.44	0.76	1.25	mA		VI=5V for Pai12xSx0C VI=0V for Pai12xSx1C
	$I_{DD2 (Q)}$	0.41	0.74	1.22	mA		
	$I_{DD1 (Q)}$	0.39	0.74	1.44	mA	$3.3V_{DC}$	VI=0V for Pai12xSx0C VI=3.3V for Pai12xSx1C
	$I_{DD2 (Q)}$	0.31	0.69	1.14	mA		
	$I_{DD1 (Q)}$	0.40	0.72	1.19	mA		VI=3.3V for Pai12xSx0C VI=0V for Pai12xSx1C
	$I_{DD2 (Q)}$	0.38	0.70	1.15	mA		

Table 13.Total Supply Current vs. Data Throughput

V_{DD1} - GND_1 = V_{DD2} - GND_2 = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, C_L = 0pF and parasitic capacitance (C_p) is 10pF, unless otherwise noted.

Part	Symbol	150kbps			1Mbps			6Mbps			Unit	Supply voltage
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Pai120SxxC	I_{DD1}		0.29	0.60		0.35	0.77		0.71	1.82	mA	$5V_{DC}$
	I_{DD2}		0.65	1.30		0.76	1.53		1.38	2.90		
	I_{DD1}		0.23	0.47		0.27	0.58		0.50	1.24	mA	$3.3V_{DC}$
	I_{DD2}		0.63	1.26		0.70	1.42		1.13	2.37		
Pai121SxxC	I_{DD1}		0.83	1.5		1.03	1.86		2.43	3.89	mA	$5V_{DC}$
	I_{DD2}		0.8	1.44		1.02	1.84		2.54	4.07		
	I_{DD1}		0.75	1.36		0.88	1.58		1.79	2.87	mA	$3.3V_{DC}$
	I_{DD2}		0.72	1.3		0.86	1.55		1.84	2.94		
Pai122SxxC	I_{DD1}		0.83	1.5		1.03	1.86		2.43	3.89	mA	$5V_{DC}$
	I_{DD2}		0.8	1.44		1.02	1.84		2.54	4.07		
	I_{DD1}		0.75	1.36		0.88	1.58		1.79	2.87	mA	$3.3V_{DC}$
	I_{DD2}		0.72	1.3		0.86	1.55		1.84	2.94		

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 14.Insulation Specifications

Parameter	Symbol	Value	Value	Value	Unit	Test Conditions/Comments
Device		Pai12xS3xC-SR	Pai12xS6xC-W5R	Pai12xS6xC-W1R		
Package		NB SOIC-8	WB SOIC-8	WB SOIC-16		
Rated Dielectric Insulation Voltage	V_{ISO}	3750	5700	5700	V_{RMS}	1-minute duration, certificated
Minimum External Air Gap (Clearance)	CLR	⩾4	⩾8.5	⩾8	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	CRP	⩾4	⩾8.5	⩾8	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)	DTI	⩾21	⩾21	⩾21	μm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	⩾400	⩾400	⩾400	V	DIN EN 60112 (VDE 0303-11):2010-05
Material Group		II	II	II		IEC 60112:2003 + A1:2009

PACKAGE CHARACTERISTICS

Table 15.Package Characteristics

Parameter	Symbol	Value	Value	Value	Unit	Test Conditions/Comments
Device		Pai12xS3xC-SR	Pai12xS6xC-W5R	Pai12xS6xC-W1R		
Package		NB SOIC-8	WB SOIC-8	WB SOIC-16		
Capacitance (Input to Output)[1]	C_{I-O}	1.5	1.5	1.5	pF	@300kHz
Input Capacitance[2]	C_I	3	3	3	pF	@1MHz, ensured by design
IC Junction to Ambient Thermal Resistance	θ_{JA}	105	86.5	45	°C/W	

Notes:

[1] The device is considered a 2-terminal device; Short-circuit all terminals on the V_{DD1} side as one terminal and short-circuit all terminals on the V_{DD2} side as the other terminal. Not tested in production, guaranteed by design

[2] Testing from the input signal pin to ground. Not tested in production, guaranteed by design.

REGULATORY INFORMATION

See Table 16 for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table 16.Regulatory

Regulatory	UL	VDE	CQC
Pai12xS3xC-SR	Recognized under UL 1577 Component Recognition Program[1] Single Protection, 3750V_{RMS} Isolation Voltage File number: Pending	DIN EN IEC 60747-17 (VDE 0884-17): 2021-10[2] Basic insulation, V_{IORM} = 637V_{Peak}, V_{IOSM} = 5000V_{Peak}; File number: Pending	Certified under CQC11-471543-2012 and GB4943.1-2011 Basic insulation at 500V_{RMS} (707V_{Peak}) working voltage, altitude ≤ 5000m Reinforced insulation at 400V_{RMS} (565V_{Peak}) working voltage, altitude ≤ 2000m File number: Pending
Pai12xS6xC-W5R	Recognized under UL 1577 Component Recognition Program[1] Single Protection, 5700 V_{RMS} Isolation Voltage File number: Pending	DIN EN IEC 60747-17 (VDE 0884-17): 2021-10[2] Reinforced insulation, V_{IORM} = 2121V_{Peak}, V_{IOSM} = 12800$V_{Peak;}$ File number: Pending	Certified under CQC11-471543-2022 and GB4943.1-2022 Altitude ≤ 5000 m, Tropical Climate, Basic insulation at 1118V_{RMS} (1580V_{Peak}) maximum working voltage, Reinforced insulation at 422V_{RMS} (600V_{Peak}) maximum working voltage. File number: Pending
Pai12xS6xC-W1R	Recognized under UL 1577 Component Recognition Program[1] Single Protection, 5700 V_{RMS} Isolation Voltage File number: Pending	DIN EN IEC 60747-17 (VDE 0884-17): 2021-10[2] Reinforced insulation, V_{IORM} = 2121V_{Peak}, V_{IOSM} = 12800$V_{Peak;}$ File number: Pending	Certified under CQC11-471543-2022 and GB4943.1-2022 Altitude ≤ 5000 m, Tropical Climate, Basic insulation at 1118V_{RMS} (1580V_{Peak}) maximum working voltage, Reinforced insulation at 422V_{RMS} (600V_{Peak}) maximum working voltage. File number: Pending

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Notes:

[1] In accordance with UL 1577, each Pai12xS3xC is proof tested by applying an insulation test voltage ≥ 4500 V_{RMS} for 1 sec; each Pai12xS6xC is proof tested by applying an insulation test voltage ≥ 6840 V_{RMS} for 1 sec.

[2] In accordance with DIN V VDE V 0884-11, each Pai12xS3xC is proof tested by applying an insulation test voltage ≥ 956 V_{Peak} for 1 sec (partial discharge detection limit = 5 pC), each Pai12xS6xC is proof tested by applying an insulation test voltage ≥ 3977V_{Peak} for 1 sec (partial discharge detection limit = 5 pC).

DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS

Table 17.VDE Insulation Characteristics

Description	Test Conditions/ Comments	Symbol	Characteristic		Unit
Device			Pai12xS3xC-SR	Pai12xS6xC-W5R Pai12xS6xC-W1R	
Overvoltage category per IEC 60664-1					
For Rated Mains Voltage ≤ 150 V_{RMS}			I to IV	I to IV	
For Rated Mains Voltage ≤ 300 V_{RMS}			I to IV	I to IV	
For Rated Mains Voltage ≤ 400 V_{RMS}			I to III	I to IV	
For Rated Mains Voltage ≤ 600 V_{RMS}			N/A	I to IV	
Climatic Classification			40/125/21	40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	
Maximum repetitive peak isolation voltage	Time dependent dielectric breakdown test	V_{IORM}	637	2121	V_{peak}
Maximum isolation working voltage	AC voltage (sine wave)	V_{IOWM}	450	1500	V_{RMS}
	DC Voltage		637	2121	V_{peak}
Method b1					
100% production test, no pre-condition tests	$V_{IORM} \times 1.5 = V_{pd\,(m)}$, $t_{ini} = t_m = 1$ sec, partial discharge < 5pC	$V_{pd\,(m)}$	956	N/A	V_{peak}
	$V_{IORM} \times 1.875 = V_{pd\,(m)}$, $t_{ini} = t_m = 1$ sec, partial discharge < 5pC	$V_{pd\,(m)}$	N/A	3977	V_{peak}
Method a					
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd\,(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5pC	$V_{pd\,(m)}$	829	N/A	V_{peak}
	$V_{IORM} \times 1.6 = V_{pd\,(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5pC		N/A	3394	
Method a					
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd\,(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5pC	$V_{pd\,(m)}$	765	2545	V_{peak}
Highest Allowable Overvoltage	$V_{TEST} = V_{IOTM}$ t = 60s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$ t= 1s (100% production)	V_{IOTM}	4243	8062	V_{peak}
Maximum Surge Isolation Voltage	Reinforced insulation, 1.2/50 µs combination wave, tested voltage (qualification)[1]	V_{IOSM}	5000	12800	V_{peak}
Maximum Impulse Voltage	Tested in air, 1.2/50 µs combination wave, $V_{IMP} \times 1.6 \leq V_{IOSM}$	V_{IMP}	3846	8000	V_{peak}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 9)				
Maximum Safety Temperature		T_S	150	150	°C
Maximum Power Dissipation at 25°C		P_S	1.25	W5R Device: 1.44 W1R Device: 2.78	W
Insulation Resistance	V_{IO} = 500V, T_A= 25°C	R_{I-O}	$\geqslant 10^{12}$	$\geqslant 10^{12}$	Ω
Insulation Resistance	V_{IO} = 500V, 100°C ⩽ T_A ⩽ 125°C	R_{I-O}	$\geqslant 10^{11}$	$\geqslant 10^{11}$	Ω
Insulation Resistance at T_S	V_{IO} = 500V, T_S = 150°C	R_{I-O}	$\geqslant 10^{9}$	$\geqslant 10^{9}$	Ω

Notes:

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[1]In accordance with DIN V VDE V 0884-11, Pai12xS3xC is proof tested by applying a surge isolation voltage of 5000V, Pai12xS6xC is proof tested by applying a surge isolation voltage of 12800V.

Typical Thermal Characteristic

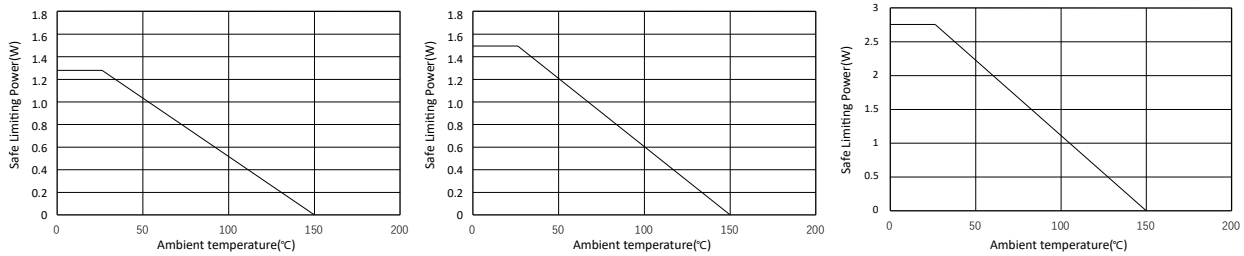


Figure 9.Thermal Derating Curve, Dependence Of Safety Limiting Values with Ambient Temperature per VDE (left: '-SR' device, middle: '-W5R' device, right: '-W1R' device.)

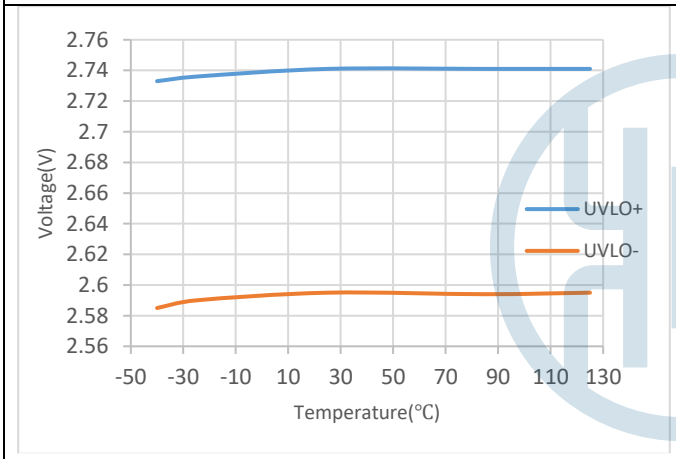


Figure 10. UVLO vs. Free-Air Temperature

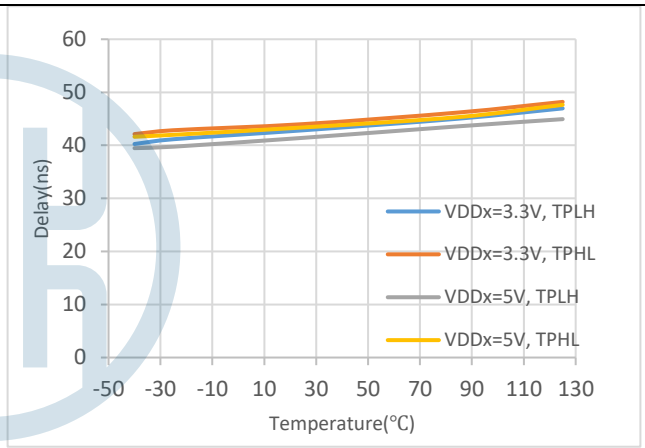


Figure 11. Pai12xSxxC *Propagation Delay Time vs. Free-Air Temperature*

Timing test information

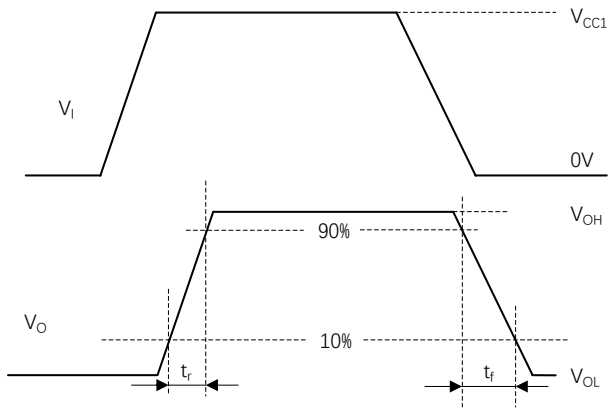


Figure 12.Transition time waveform measurement

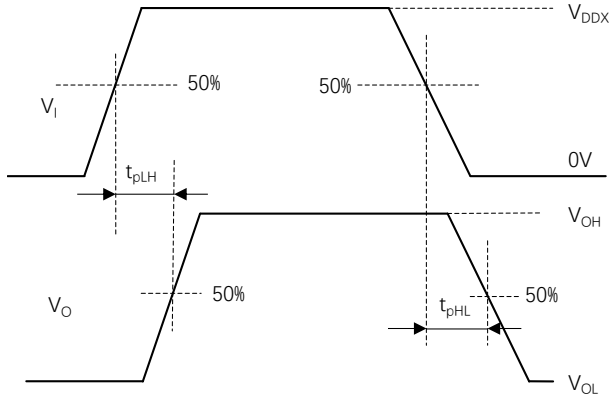
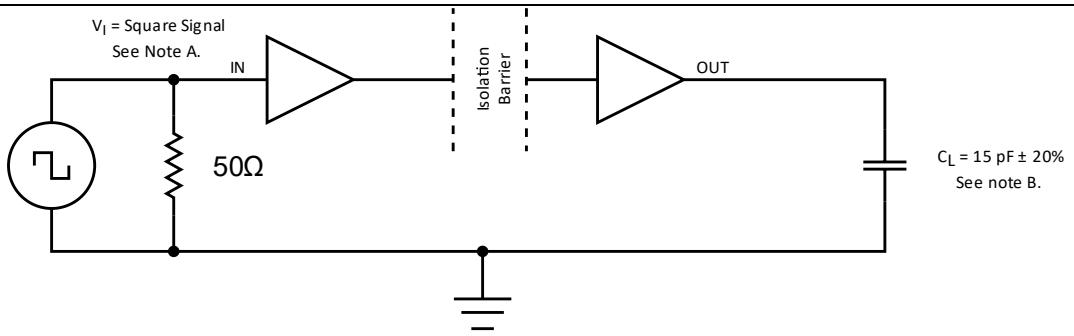


Figure 13. Propagation delay time waveform measurement



A. The input square signal is supplied by a generator having the following spec: frequency = 500kHz, 50% duty cycle, t_r < 2.5ns, t_f < 2.5ns, Z_O = 50 ohm.
B. C_L includes instrumentation and fixture capacitance within ±20%.

Figure 14. Switching Specifications Test Circuit

APPLICATIONS INFORMATION

Overview

The Pai1xxSxC isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 5.0kV$_{RMS}$ and the data rate from DC up to 8Mbps. The devices operate with the supply voltage on either side ranging from 3.0V to 5.5V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier.
The fail-safe state is available in which the outputs transition to a preset state when the input power supply is not applied. For example, if input power loses, the output will be logic high for Pai1xxSx1C and logic low for Pai1xxSx0C.
Compared to the old π1xxUxx series, Pai1xxSxxC digital isolators can provide lower propagation delay, higher data rate and better system-level ESD performance.

Theory of Operation

Device Startup

The Pai12xSxxC digital isolator requires a startup time of 10μs. During the startup, the outputs of Pai12xSxxC are held in high-impedance state. After VDD is above the UVLO rising threshold, the outputs follow the states of inputs.

Device I/O Schematics

Inputs of Pai12xSxxC have an internal current source. While the input ports are floating, the current source will keep the signal channel in the fail-safe output state. Therefore, the direction of the input current is related to the fail-safe output state. High fail-safe output state devices have a pull-up input current and low fail-safe output state devices have a pull-down input current, as shown in Figure 15 and Figure 16.
The output port of Pai12xSxxC uses a push-pull circuit, with the equivalent output impedance being approximately 50 ohms in both output high and low states, as shown in Figure 17.

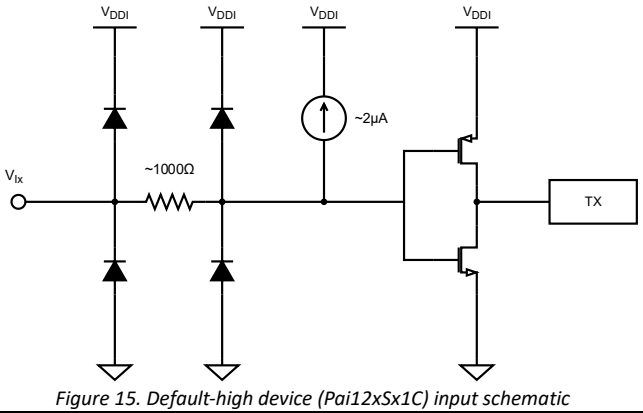


Figure 15. Default-high device (Pai12xSx1C) input schematic

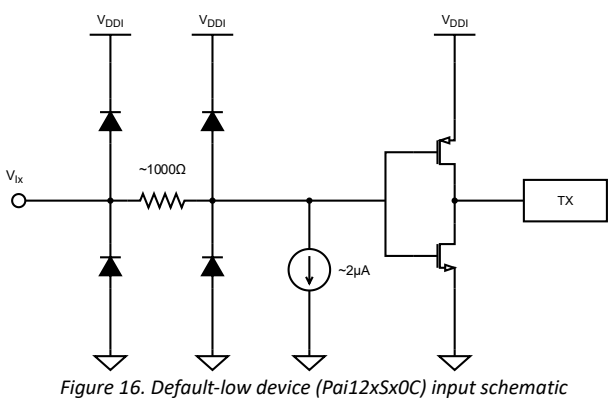


Figure 16. Default-low device (Pai12xSx0C) input schematic

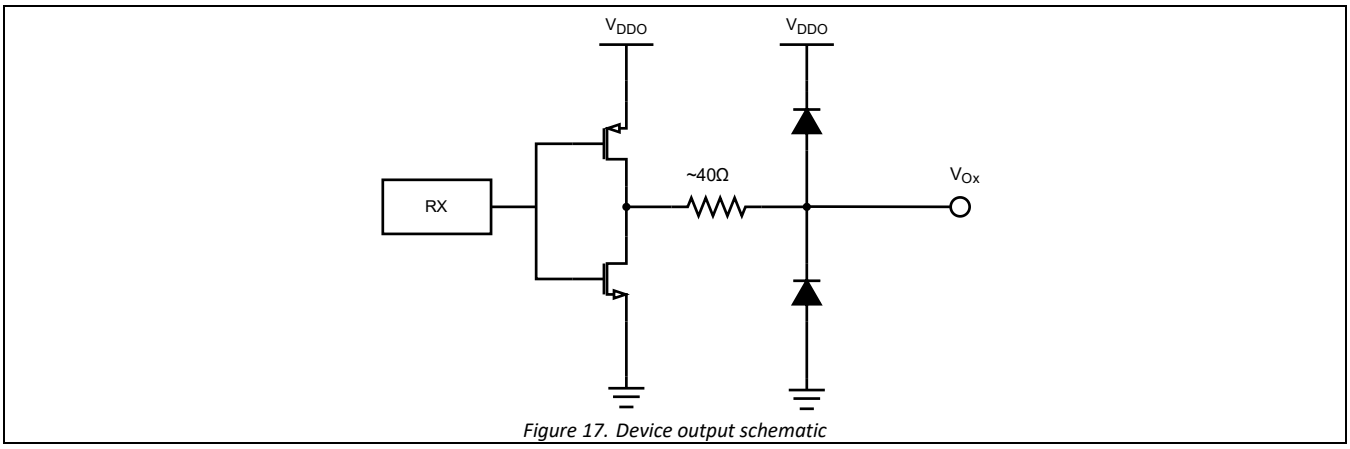


Figure 17. Device output schematic

PCB layout recommendations

The low-ESR ceramic bypass capacitors must be connected between V_{DD1} and GND_1 and between V_{DD2} and GND_2. The bypass capacitors are placed on the PCB as close to the isolator device as possible, and the capacitance should be selected between 0.1µF and 10µF.

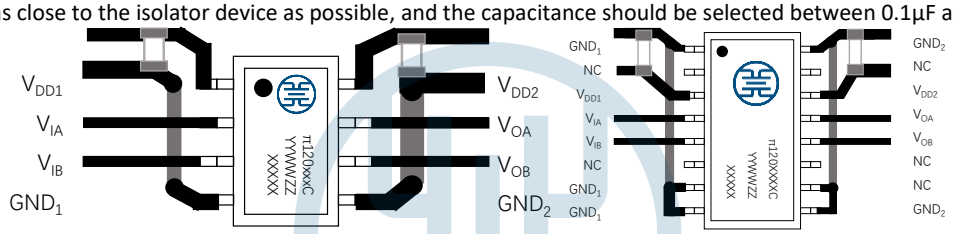
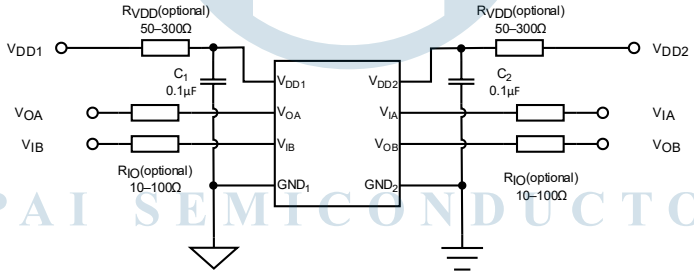


Figure 18.Recommended Printed Circuit Board Layout (left: Pai12xS3xC-SR/Pai12xS6xC-W5R, right: Pai12xS6xC-W1R)

If the V_{DDx} power lines are excessively noisy and the supply voltages. If excessive noise, voltage spikes, or glitches are present in the V_{DDx} power supply circuit, a resistor (50–300 Ω) may need to be connected in series. The resistors, combined with bypass capacitors, forms a filter to enhance the robustness of a design.



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Figure 19. Robustness-enhanced Application Circuit

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30V_{RMS} AC) must be physically separated from the safety extra-low voltage circuits (a circuit with <30V_{RMS} AC) by a certain distance (creepage/clearance).

CMTI measurements

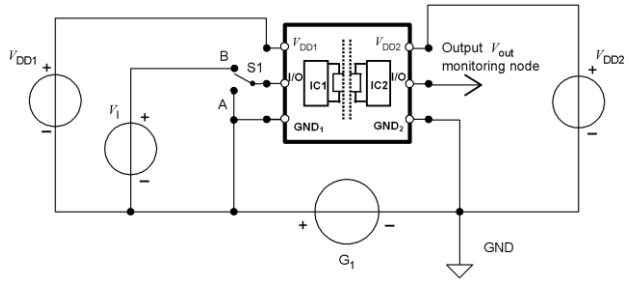


Figure 20.Common-mode transient immunity (CMTI) measurement

To measure the Common-Mode Transient Immunity (CMTI) of digital opto-couplers under specified common-mode pulse magnitude (V_{CM}) and specified slew rate of the common-mode pulse (dV_{CM}/dt) and other specified test or ambient conditions, the common-mode pulse

generator (G_1) will be capable of providing fast rising and falling pulses of specified magnitude and duration of the common-mode pulse (V_{CM}) and the maximum common-mode slew rates (dV_{CM}/dt) can be applied to digital opto-couplers under measurement. The common-mode pulse is applied between one side ground GND1 and the other side ground GND2 of digital opto-couplers and shall be capable of providing positive transients as well as negative transients.

OUTLINE DIMENSIONS

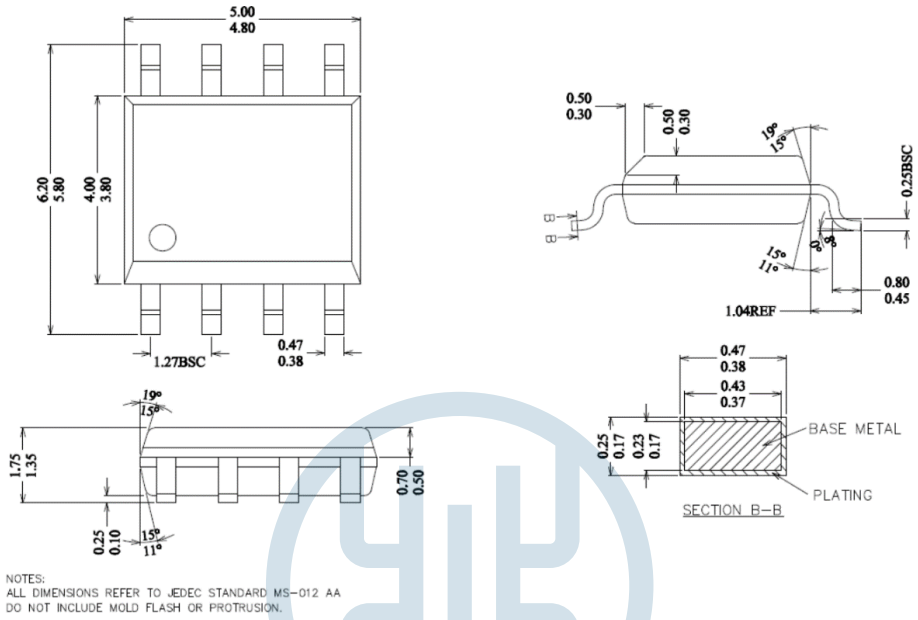
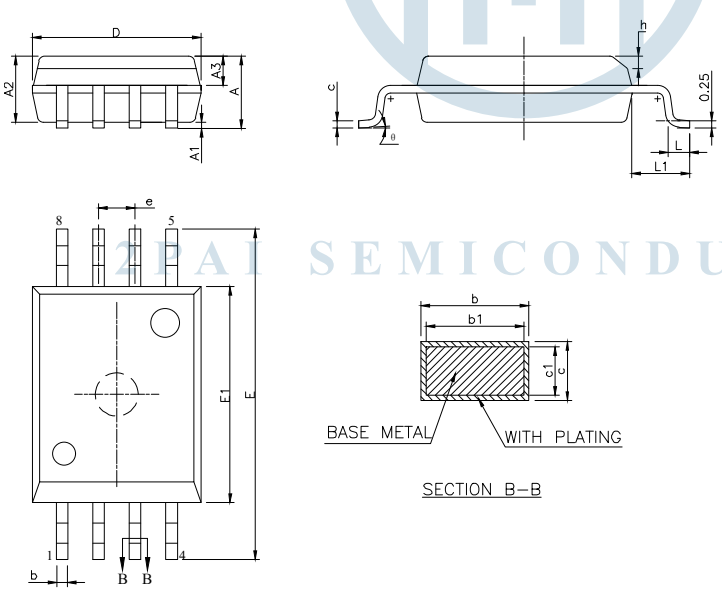


Figure 21. 8-Lead Narrow Body SOIC [NB SOIC-8] Outline Package–dimension unit(mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	5.75	5.85	5.95
E	11.30	11.50	11.70
E1	7.40	7.50	7.60
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	1.00
L1	2.00REF		
θ	0	—	8°

Figure 22. 8-Lead Wide Body SOIC [WB SOIC-8] Outline Package–dimension unit(mm)

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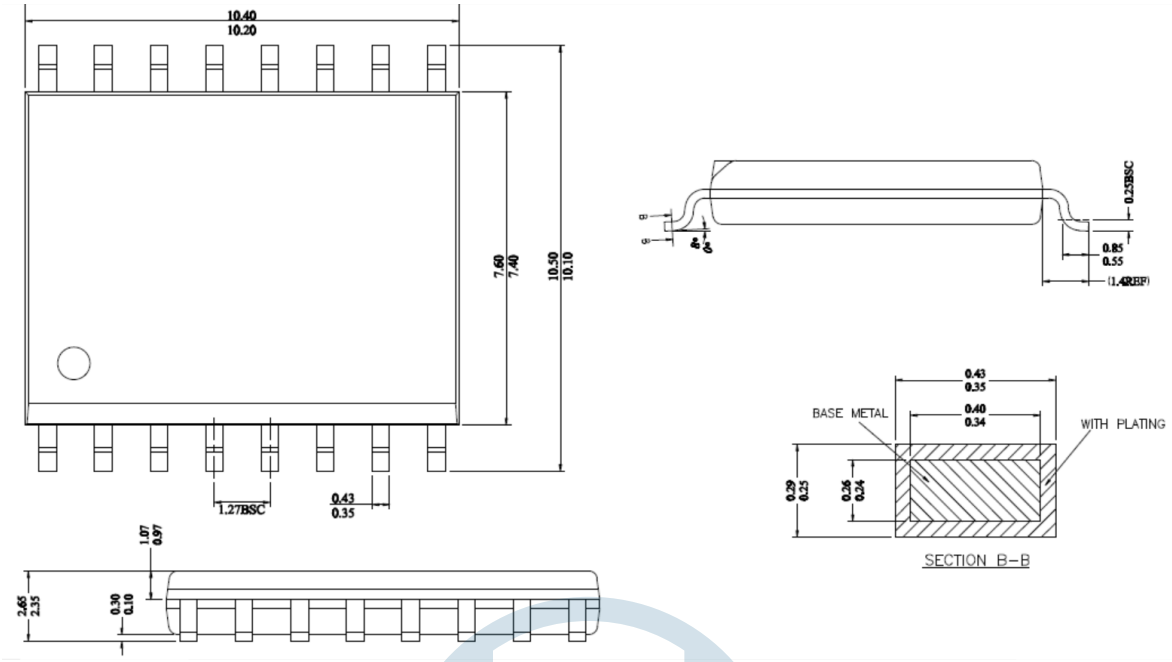
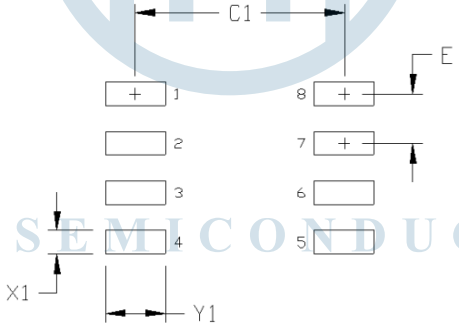


Figure 23.16-Lead Wide Body SOIC Package [WB SOIC-16] Outline Package–dimension unit(mm)

Land Patterns

8-Lead Narrow Body SOIC [NB SOIC-8]

The Figure 24 below illustrates the recommended land pattern details for the Pai1xxxxxC-SR in an 8-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.



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*Figure 24.*8-Lead Narrow Body SOIC [NB SOIC-8] Land Pattern

Table 18.8-Lead Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	Parameter	Unit
C1	Pad column spacing	5.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.55	mm

Note：

1.This land pattern design is based on IPC -7351.

2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

8-Lead Wide Body SOIC [WB SOIC-8]

The Figure 25 below illustrates the recommended land pattern details for the Pai1xxxxxC-W5R in an 8-pin wide-body SOIC. The table below lists the values for the dimensions shown in the illustration.

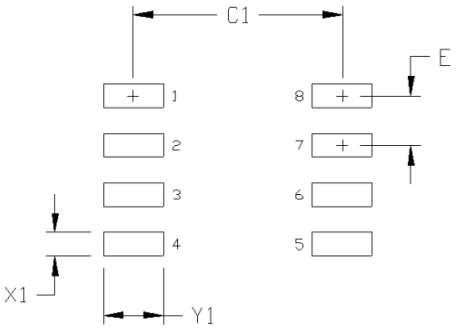


Figure 25. 8-Lead Wide Body SOIC [WB SOIC-8] Land Pattern

Table19. 8-Lead Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	Parameter	Unit
C1	Pad column spacing	10.90	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	2.00	mm

Note：

(1) This land pattern design is based on IPC -7351.

(2) All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

16-Lead Wide Body SOIC [WB SOIC-16]

The Figure 26 below illustrates the recommended land pattern details for the Pai1xxxxxC-W1R in a 16-pin Wide Body SOIC. The table below lists the values for the dimensions shown in the illustration.

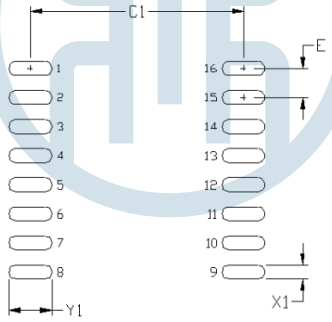


Figure 26.16-Lead Wide Body SOIC [WB SOIC-16] Land Pattern

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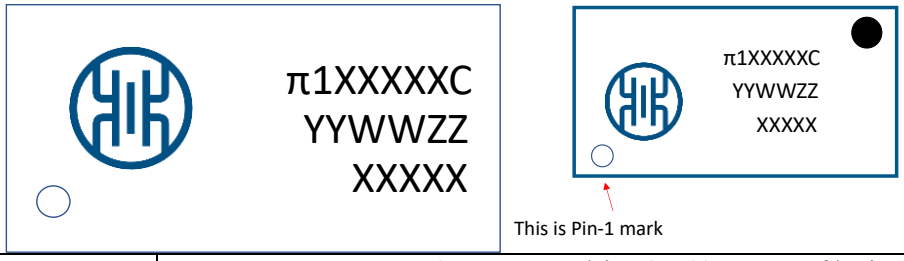
Table 20. 16-Lead Wide Body SOIC [WB SOIC-16] Land Pattern Dimensions

Dimension	Feature	Parameter	Unit
C1	Pad column spacing	9.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.90	mm

Note：

1. This land pattern design is based on IPC -7351.
2. All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.
3. Board assembly site may have different recommendations for stencil design.

Top Marking

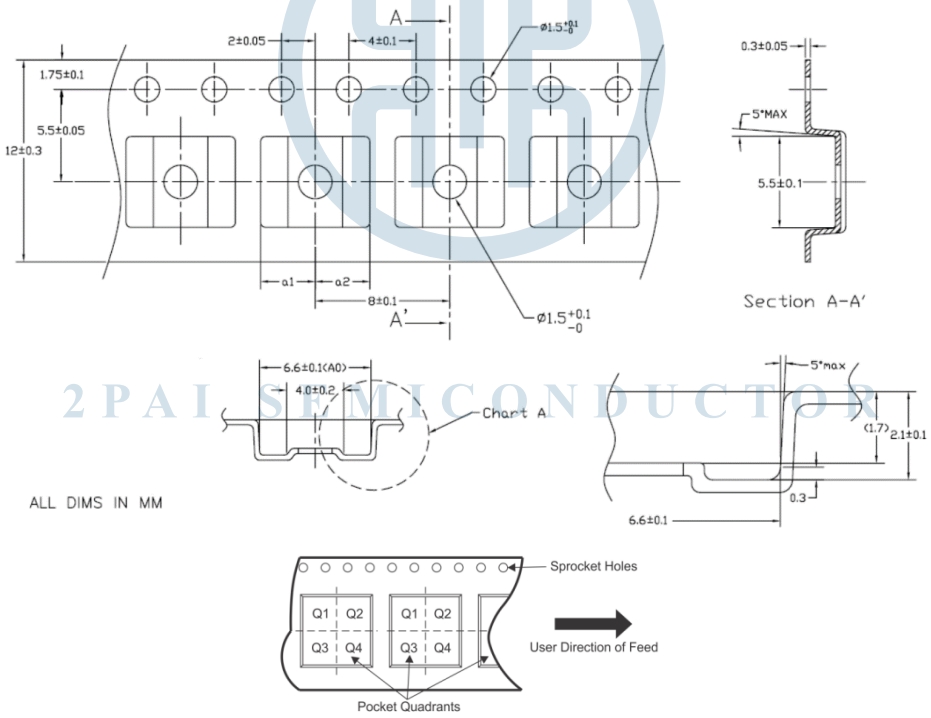


Line 1	π1xxxxxC=Pai1xxxxxC =Product name, use 'π' as the abbreviation of 'Pai' in top marking.
Line 2	YY = Work Year WW = Work Week ZZ=Manufacturing code from assembly house
Line 3	XXXXX, no special meaning

Figure 27. Top Marking, left: Pai12xS3xC-SR/Pai12xS6xC-W1R, right: Pai12xS6xC-W5R

REEL INFORMATION

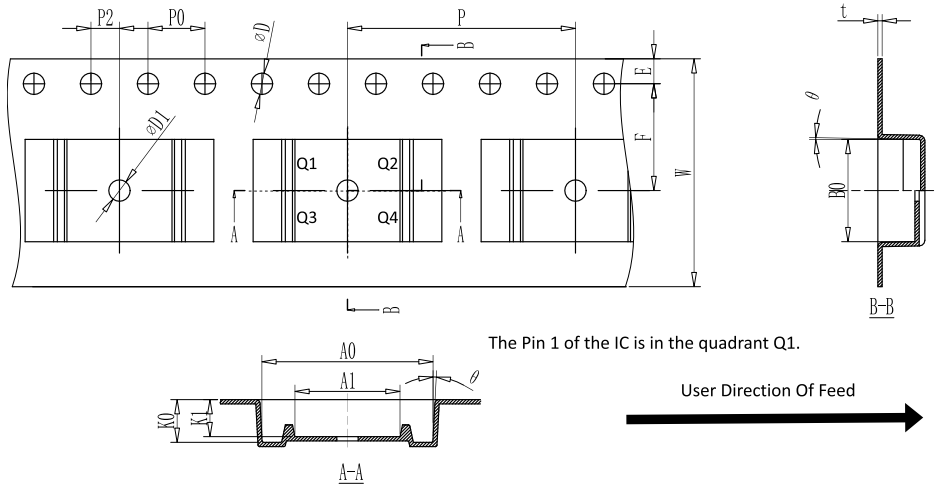
8-Lead Narrow Body SOIC [NB SOIC-8]



Note：The Pin 1of the chip is in the quadrant Q1.

Figure 28. 8-Lead Narrow Body SOIC [NB SOIC-8] Reel Information–dimension unit(mm)

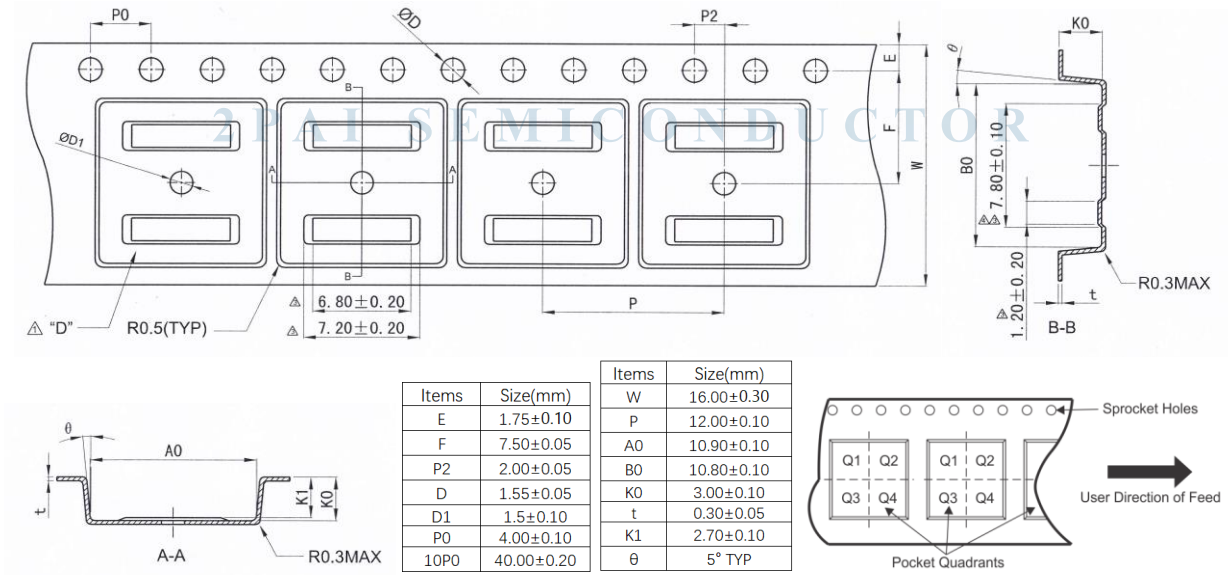
8-Lead Wide Body SOIC [WB SOIC-8]



Items	Size	Unit	Items	Size	Unit
E	1.75 ± 0.10	mm	W	16.00 ± 0.30	mm
F	7.50 ± 0.10	mm	P	16.00 ± 0.10	mm
P2	2.00 ± 0.10	mm	A0	11.98 ± 0.10	mm
D	$1.50^{+0.10}_{0}$	mm	A1	7.37 ± 0.10	mm
D1	$1.50^{+0.10}_{0}$	mm	B0	6.11 ± 0.10	mm
P0	4.00 ± 0.10	mm	K0	3.00 ± 0.10	mm
10P0	40.0 ± 0.20	mm	K1	2.60 ± 0.10	mm
			t	0.30 ± 0.05	mm
			θ	5 typical	Degree

Figure 29. 8-Lead Wide Body SOIC [WB SOIC-8] Reel Information–dimension unit(mm)

16-Lead Wide Body SOIC [WB SOIC-16]



Items	Size(mm)
E	1.75±0.10
F	7.50±0.05
P2	2.00±0.05
D	1.55±0.05
D1	1.5±0.10
P0	4.00±0.10
10P0	40.00±0.20

Items	Size(mm)
W	16.00±0.30
P	12.00±0.10
A0	10.90±0.10
B0	10.80±0.10
K0	3.00±0.10
t	0.30±0.05
K1	2.70±0.10
θ	5° TYP

Note：The Pin 1of the chip is in the quadrant Q1

Figure 30.16-Lead Wide Body SOIC [WB SOIC-16] Reel Information

ORDERING GUIDE

Table 21. ORDERING GUIDE

Model Name [1]	Temperature Range	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Isolation Rating (kV rms)	Fail-Safe Output State	Package	MSL Peak Temp [2]	MOQ/ Quantity per reel[3]
Pai120S31C-SR	−40~125°C	2	0	3.75	High	NB SOIC-8	Level 2, verifying	4000
Pai120S30C-SR	−40~125°C	2	0	3.75	Low	NB SOIC-8	Level 2, verifying	4000
Pai121S31C-SR	−40~125°C	1	1	3.75	High	NB SOIC-8	Level 2, verifying	4000
Pai121S30C-SR	−40~125°C	1	1	3.75	Low	NB SOIC-8	Level 2, verifying	4000
Pai122S31C-SR	−40~125°C	1	1	3.75	High	NB SOIC-8	Level 2, verifying	4000
Pai122S30C-SR	−40~125°C	1	1	3.75	Low	NB SOIC-8	Level 2, verifying	4000
Pai120S61C-W5R	−40~125°C	2	0	5.7	High	WB SOIC-8	Level 3, verifying	1000
Pai120S60C-W5R	−40~125°C	2	0	5.7	Low	WB SOIC-8	Level 3, verifying	1000
Pai121S61C-W5R	−40~125°C	1	1	5.7	High	WB SOIC-8	Level 3, verifying	1000
Pai121S60C-W5R	−40~125°C	1	1	5.7	Low	WB SOIC-8	Level 3, verifying	1000
Pai122S61C-W5R	−40~125°C	1	1	5.7	High	WB SOIC-8	Level 3, verifying	1000
Pai122S60C-W5R	−40~125°C	1	1	5.7	Low	WB SOIC-8	Level 3, verifying	1000
Pai120S61C-W1R	−40~125°C	2	0	5.7	High	WB SOIC-16	Level 3, verifying	1500
Pai120S60C-W1R	−40~125°C	2	0	5.7	Low	WB SOIC-16	Level 3, verifying	1500
Pai121S61C-W1R	−40~125°C	1	1	5.7	High	WB SOIC-16	Level 3, verifying	1500
Pai121S60C-W1R	−40~125°C	1	1	5.7	Low	WB SOIC-16	Level 3, verifying	1500
Pai122S61C-W1R	−40~125°C	1	1	5.7	High	WB SOIC-16	Level 3, verifying	1500
Pai122S60C-W1R	−40~125°C	1	1	5.7	Low	WB SOIC-16	Level 3, verifying	1500

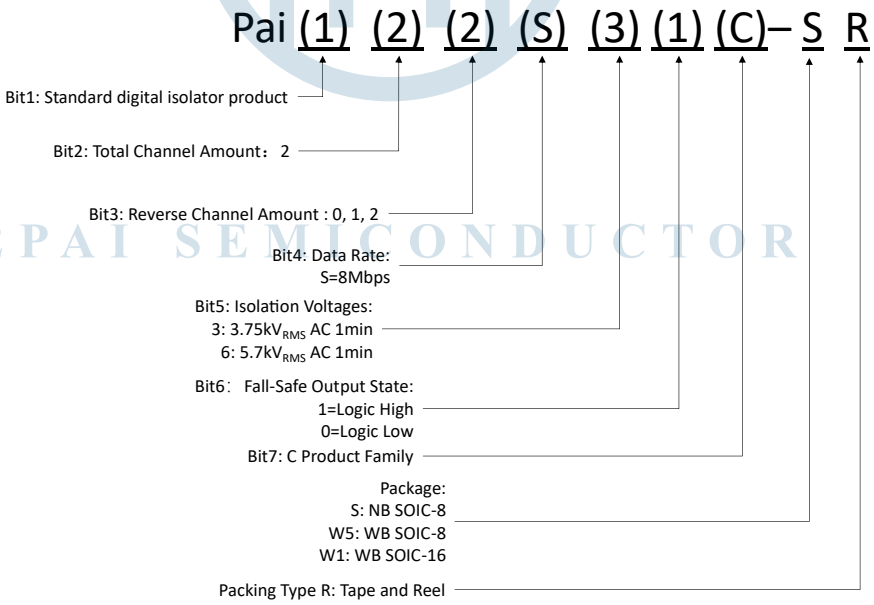
Note:

[1] "-SR", "-W5R" and "-W1R" shows the package of the chip.

[2] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[3] MOQ, minimum ordering quantity.

PART NUMBER NAMED RULE



Notes:

Pai1xxxxx is equals to π1xxxxx in the customer BOM

Figure 31. Part Number Named Rule

2PAI SEMICONDUCTOR

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REVISION HISTORY

Revision	Date	Page	Change Record
0.1	2025/04/07	All	Initial version
0.2	2026/6/1	1, 5, 6, 7	Updated specs in Table 12, Table 13 Updated Regulatory information Updated ESD specification Updated UVLO specification Updated input current specification

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