

TDSEMIC

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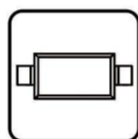
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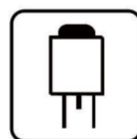
電源管理



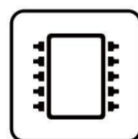
顯示驅動



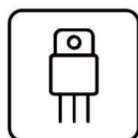
二三極管



LDO穩壓器



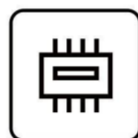
觸摸芯片



MOS管



運算放大器



存儲芯片



MCU



串口通信

TD4435

產品規格說明書

TD4435

-30V P-Channel Enhancement Mode MOSFET

$V_{DS} = 30V$ $I_D = 15A$

General Features

$R_{DS(ON)} = 13m\Omega$ @

$V_{GS}=10V$

Static On-Resistance

$R_{DS(ON)} = 19m\Omega$ @

$V_{GS}=4.5V$

Static On-Resistance

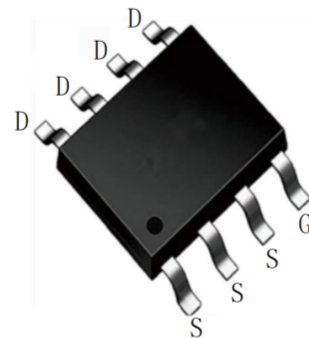
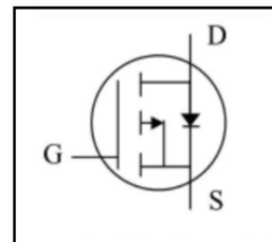
Description

The TD4435-TD uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

Application

- Battery protection
- Load switch
- Uninterruptible power supply

SOP-8L Pin Configuration



Package Marking and Ordering Information

Product ID	Package	Marking	QTY(PCS)	Packing method
TD4435	SOP-8L	4435	3000	Reel

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_A=25^\circ C$	Drain Current ³ , V_{GS} @ 10V	-15	A
$I_D@T_A=70^\circ C$	Drain Current ³ , V_{GS} @ 10V	-11	A
I_{DM}	Pulsed Drain Current ¹	-40	A
$P_D@T_A=25^\circ C$	Total Power Dissipation	2.5	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	50	$^\circ C/W$

Electrical Characteristics @T_J=25°C (unless otherwise specified)

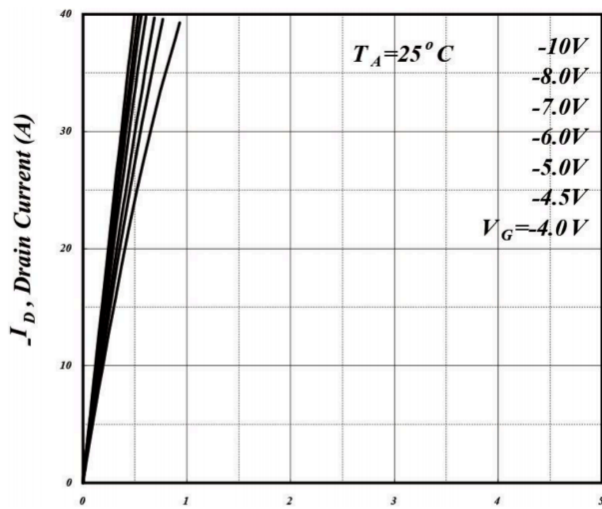
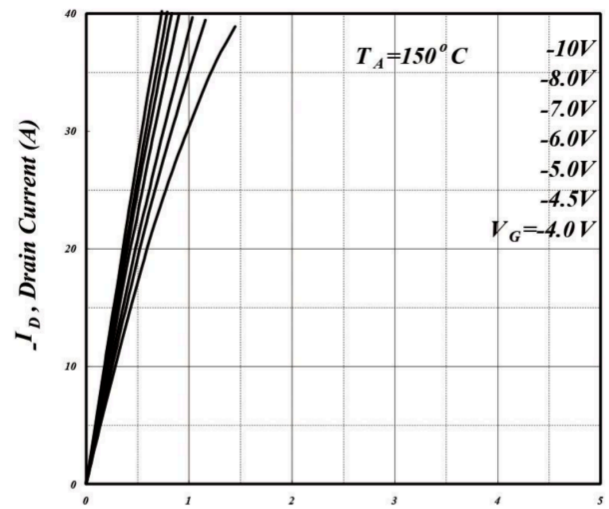
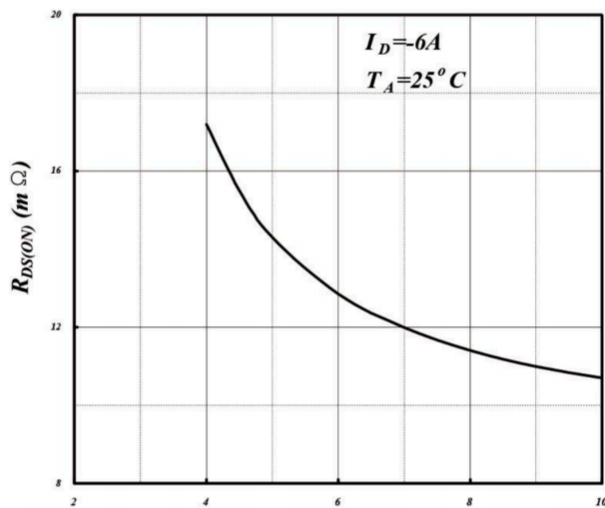
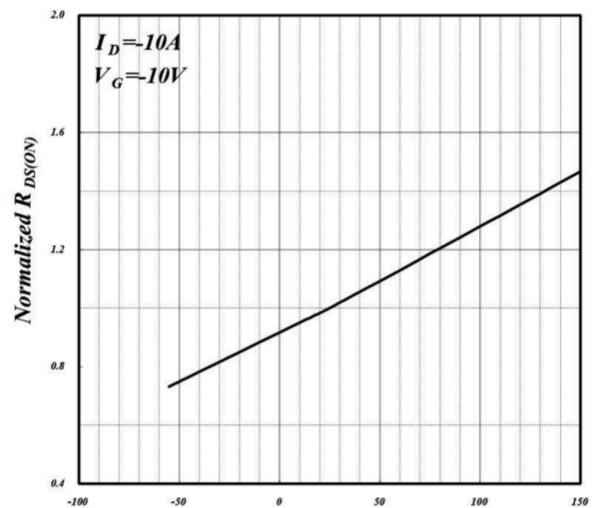
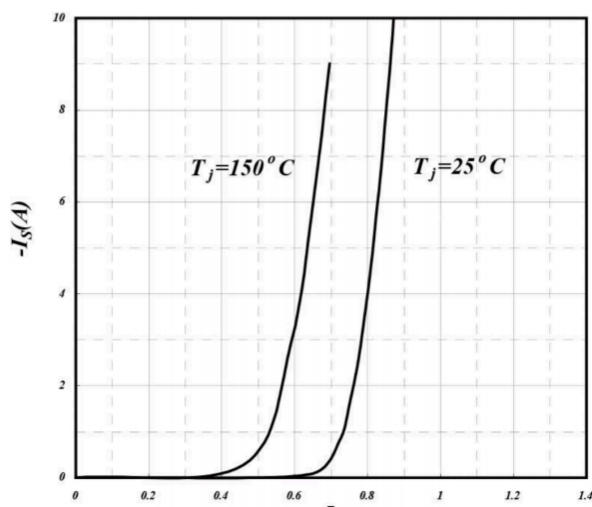
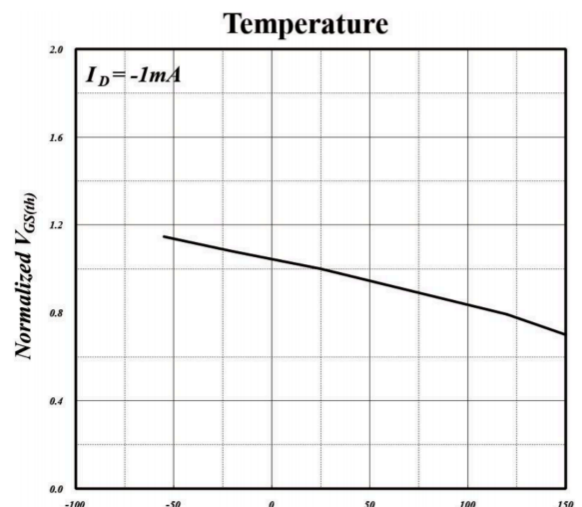
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-20A	-	13	15	mΩ
		V _{GS} =-4.5V, I _D =-20A	-	19	26	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1.2	-1.6	-2.0	V
g _{fs}	Forward Transconductance	V _{DS} =-10V, I _D =-10A	-	22	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-30V, V _{GS} =0V	-	-	-1	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =-6A V _{DS} =-15V V _{GS} =-4.5V	-	28	45	nC
Q _{gs}	Gate-Source Charge		-	7	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge		-	11	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =-15V I _D =-1A R _G =3.3Ω V _{GS} =-10V	-	13	-	ns
t _r	Rise Time		-	10	-	ns
t _{d(off)}	Turn-off Delay Time		-	80	-	ns
t _f	Fall Time		-	37	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V V _{DS} =-15V f=1.0MHz	-	2940	4700	pF
C _{oss}	Output Capacitance		-	290	-	pF
C _{rss}	Reverse Transfer Capacitance		-	210	-	pF
R _g	Gate Resistance	f=1.0MHz	-	6.2	12.4	Ω
V _{SD}	Forward On Voltage ²	I _S =-2.1A, V _{GS} =0V	-	-	-1.2	V
t _{rr}	Reverse Recovery Time	I _S =-10A, V _{GS} =0V, dI/dt=100A/μs	-	19	-	ns
Q _{rr}	Reverse Recovery Charge		-	6	-	nC

Notes:

1. Pulse width limited by Max. junction temperature.

2. Pulse test

3. Surface mounted on 1 in² copper pad of FR4 board, t ≤ 10s ; 125 °C/W when mounted on Min. copper pad.



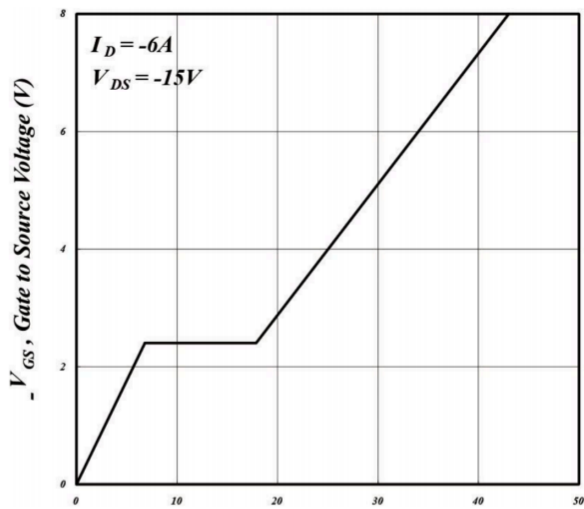


Fig 7. Gate Charge Characteristics

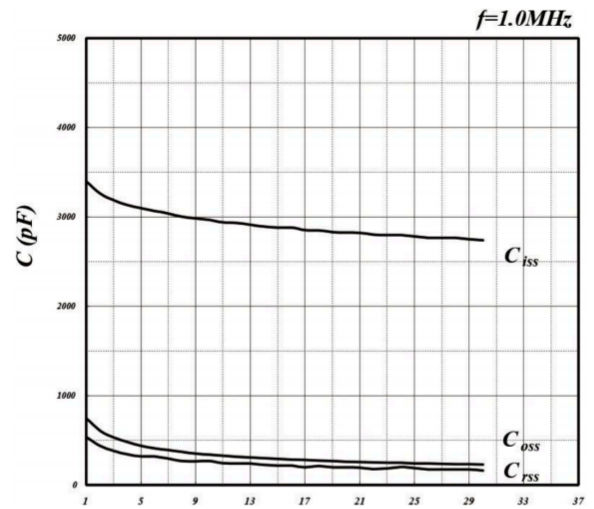


Fig 8. Typical Capacitance Characteristics

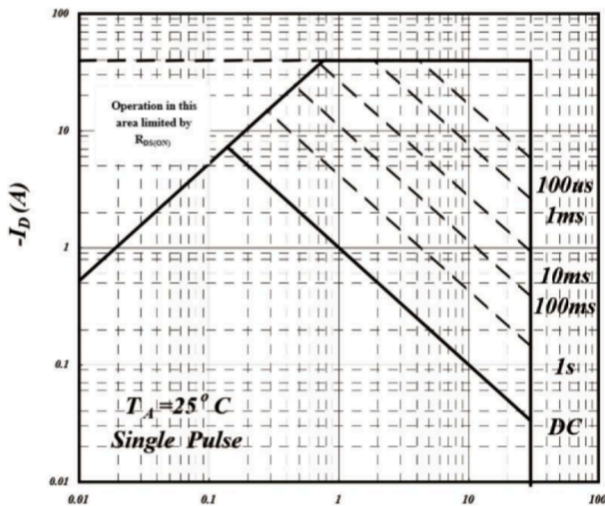


Fig 9. Maximum Safe Operating Area

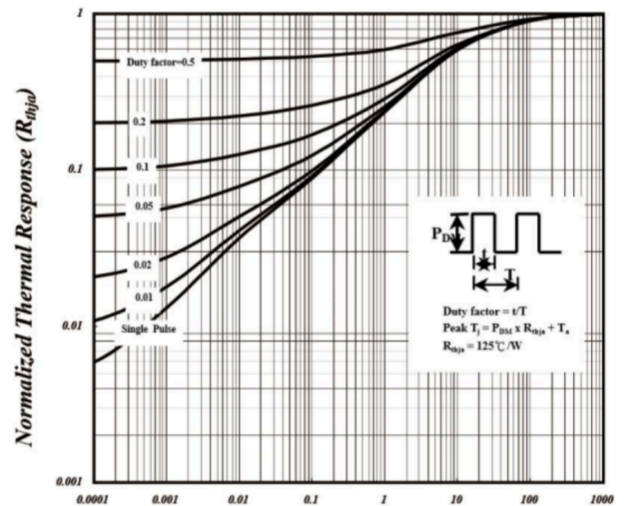


Fig 10. Effective Transient Thermal Impedance

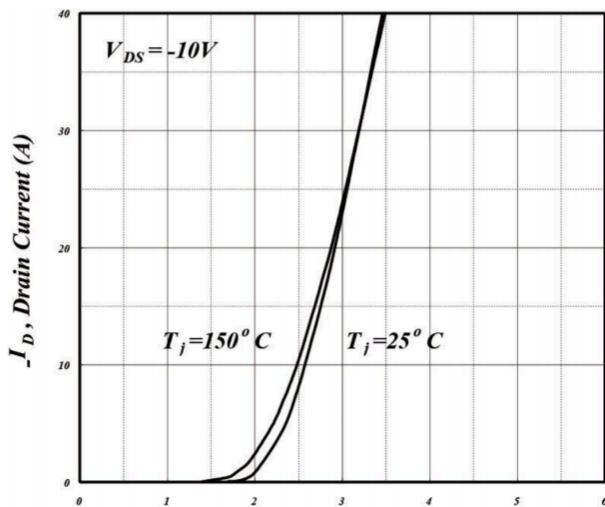


Fig 11. Transfer Characteristics

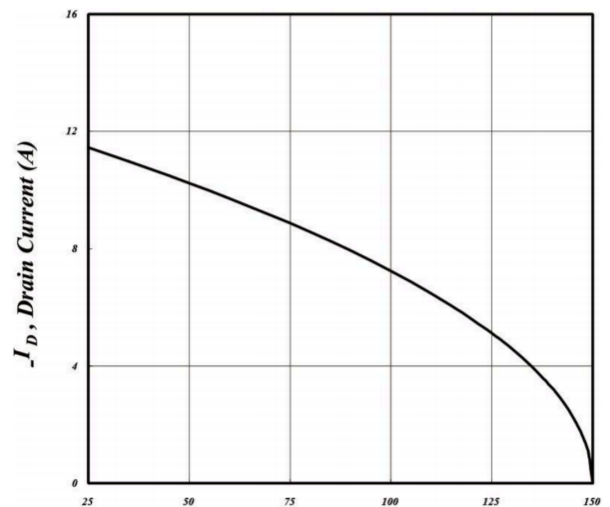
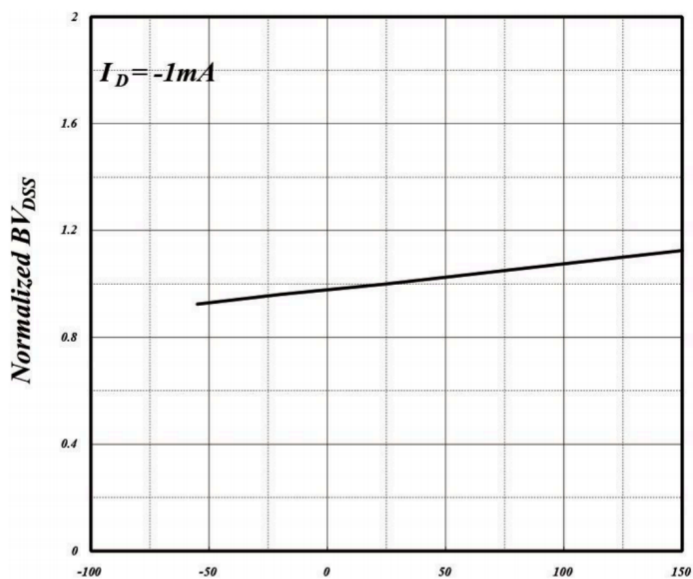
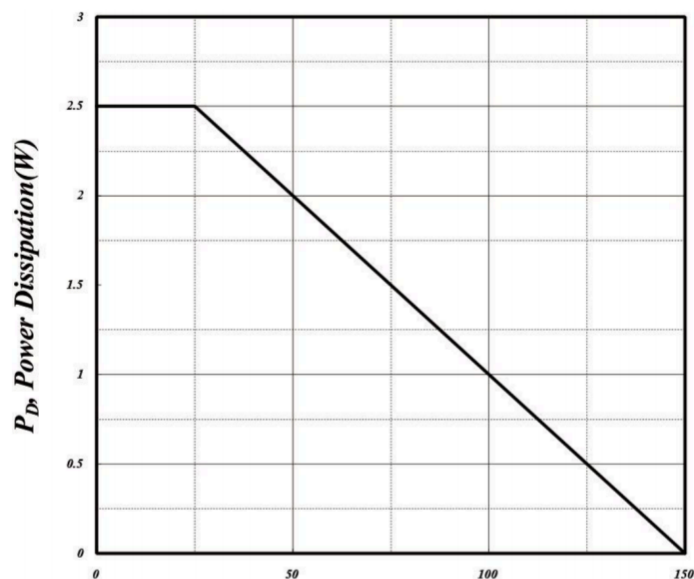
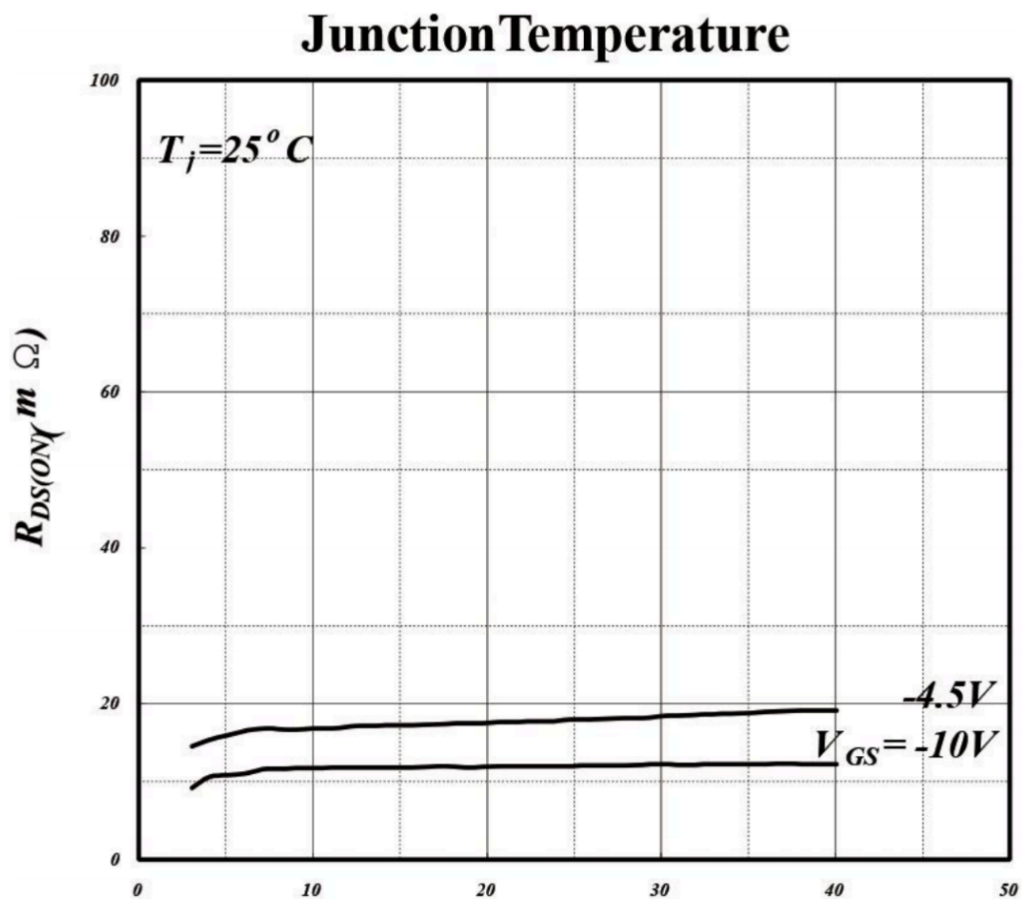
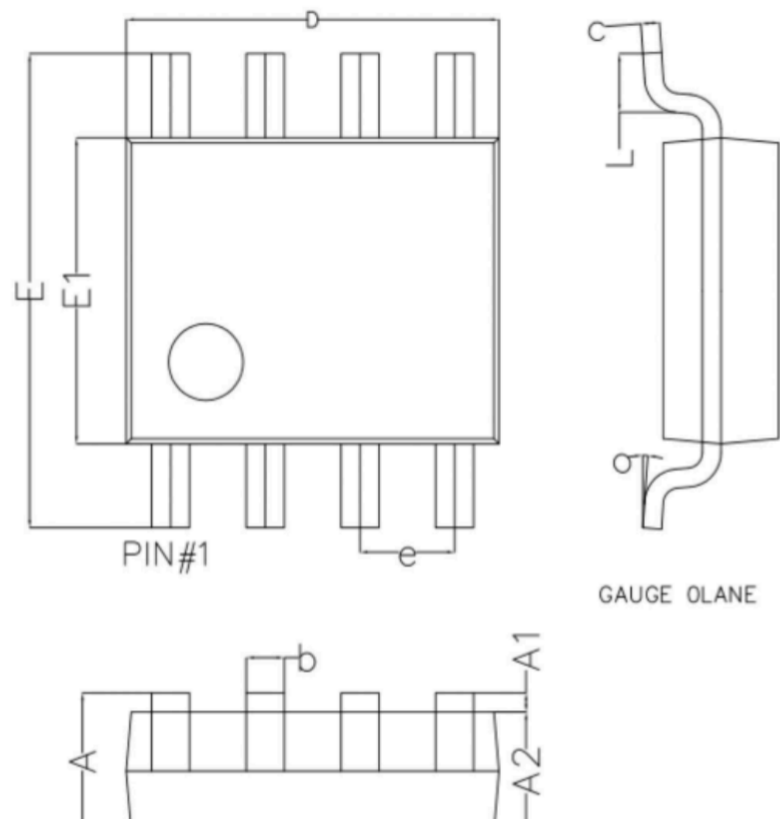


Fig 12. Drain Current v.s. Ambient Temperature



PACK SOP-8

SOP8 Package outline



SOP8 Package outline

Symbol	Dim in mm		
	Min	Nor	Max
A	1.350	1.550	1.750
A1	0.100	0.175	0.250
A2	1.350	1.450	1.550
b	0.330	0.420	0.510
c	0.170	0.210	0.250
D	4.800	4.900	5.000
e	1.270 (BSC)		
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.400	0.835	1.2700
o	0°	4°	8°