

TDSEMIC

拓電半導體

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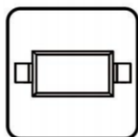
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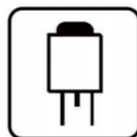
電源管理



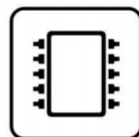
顯示驅動



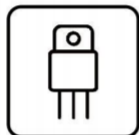
二三極管



LDO穩壓器



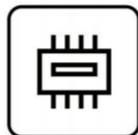
觸摸芯片



MOS管



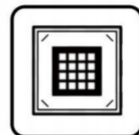
運算放大器



存儲芯片



MCU



串口通信

TD8554ARZ

產品規格說明書

TD8551, TD8552, TD8554 Zero-Drift, Low-Noise Rail-to-Rail I/O, CMOS Operational Amplifiers

Features

- Rail-to-Rail Input and Output
- Input Offset Drift: 0.005 $\mu\text{V}/^\circ\text{C}$
- Low Offset Voltage: 1 μV
- Supply Voltage Range: 1.8V to 5.5V
- Gain Bandwidth Product: 1.7MHz
- Slew Rate: 1.0V/ μs
- Micro Power: 0.46mA/Amplifier Typical Supply Current
- Overload Recovery Time: 8.5 μs
- Low Noise: 1 $\mu\text{Vp-p}$ (0.01-10Hz)
- High Gain: 130dB
- CMRR: 125dB; PSRR: 130dB
- Small Packaging: Available in Green SOT/SOP/DFN/MSOP/TSOP Packages

Applications

- Active Filters
- Photodiode Amplifier
- Piezoelectric Sensors
- Test Equipment
- Medical Instrumentation
- Audio Output
- Portable Systems
- Smoke Detectors
- Notebook PC
- Mobile Communication
- Sensor Interface
- Battery Equipment
- DSP Interface
- ASIC Input

Descriptions

The TD8551, TD8552, TD8554 families of products are CMOS operational amplifier offering very low offset voltage (1 μV typical) and near-zero drift over time and temperature.

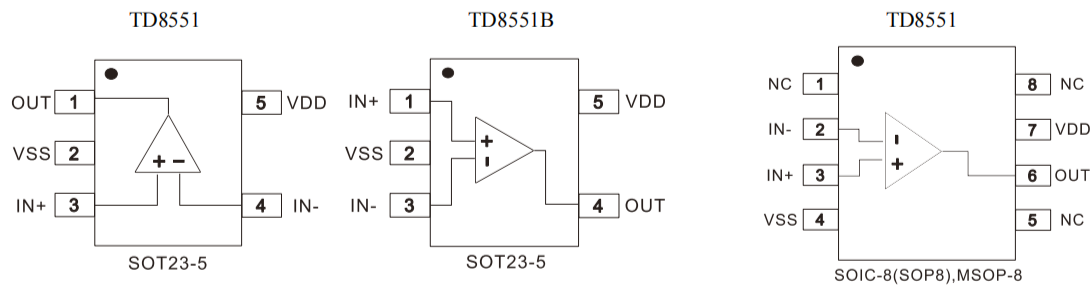
The op-amps provide 1.7MHz bandwidth at a low current consumption of 460 μA per amplifier and slew rate of 1V/ μs , offering excellent CMRR without the crossover associated with traditional complementary input stage, making this device an excellent choice for sensor interface, active filter, low voltage or battery-operated systems.

The TD8551, TD8552, TD8554 families of product are offered in Green SOT/SOP/DFN/MSOP/TSOP packages, and are specified over the extended -40 $^\circ\text{C}$ to +125 $^\circ\text{C}$ temperature range.

Device Information⁽¹⁾

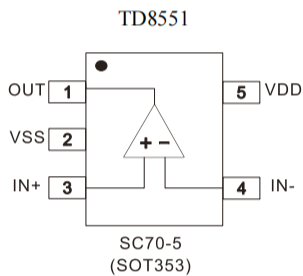
PART NUMBER	PACKAGE	BODY SIZE(NOM)
TD8551	SOT23-5	2.92mm×1.62mm
	SOT23-6	2.92mm×1.62mm
	SC70-5 (SOT353)	2.10mm×1.25mm
	SOIC-8 (SOP8)	4.90mm×3.90mm
TD8552	SOIC-8 (SOP8)	4.90mm×3.90mm
	MSOP-8	3.00mm×3.00mm
	TSSOP-8	3.00mm×4.40mm
	MSOP-10	3.00mm×3.00mm
	TDFN2×2-8L	2.00mm×2.00mm
TD8554	SOIC-14 (SOP14)	8.60mm×3.90mm
	TSSOP-14	5.00mm×4.40mm

Pin Configuration and Functions (Top View)



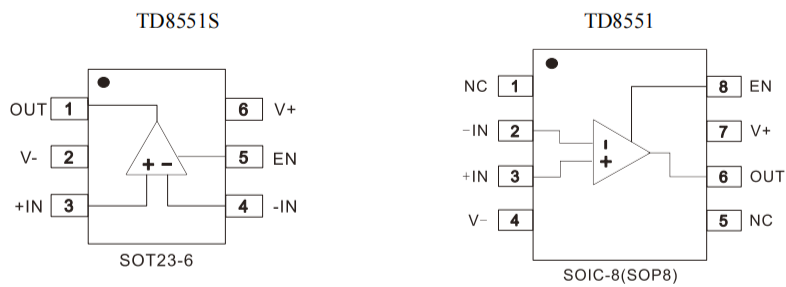
Pin Description

NAME	PIN			I/O	DESCRIPTION
	TD8551	TD8551B	TD8551		
	SOT23-5	SOT23-5	SOIC-8(SOP8)/MSOP8		
-IN	4	3	2	I	Negative (inverting) input
+IN	3	1	3	I	Positive (noninverting) input
NC	-	-	1,5,8	-	No internal connection (can be left floating)
OUT	1	4	6	O	Output
V-	2	2	4	-	Negative (lowest) power supply
V+	5	5	7	-	Positive (highest) power supply



Pin Description

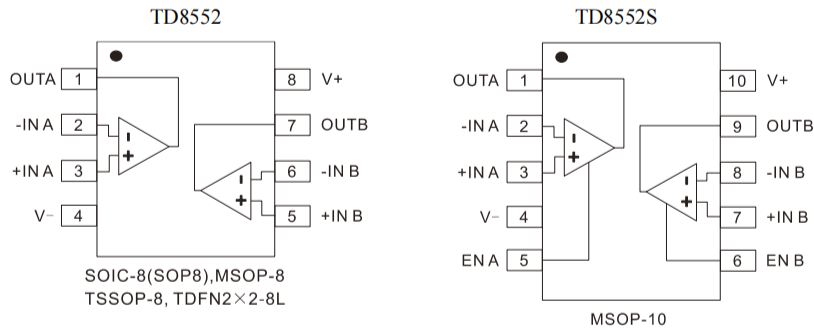
NAME	PIN	I/O	DESCRIPTION
	TD8551		
	SC70-5 (SOT353)		
-IN	4	I	Negative (inverting) input
+IN	3	I	Positive (noninverting) input
OUT	1	O	Output
V-	2	-	Negative (lowest) power supply
V+	5	-	Positive (highest) power supply



Pin Description

NAME	PIN		I/O	DESCRIPTION
	TD8551			
	SOT23-6	SOIC-8(SOP8)		
-IN	4	2	I	Negative (inverting) input
+IN	3	3	I	Positive (noninverting) input
OUT	1	1,5,8	O	No internal connection (can be left floating)
EN	5	6	I	Enable pin, this pin turns the regulator on or off. Low=disabled, high = normal operation (pin must be driven)
NC	-	1,5	-	No internal connection (can be left floating)
V-	2	4	-	Negative (lowest) power supply
V+	6	7	-	Positive (highest) power supply

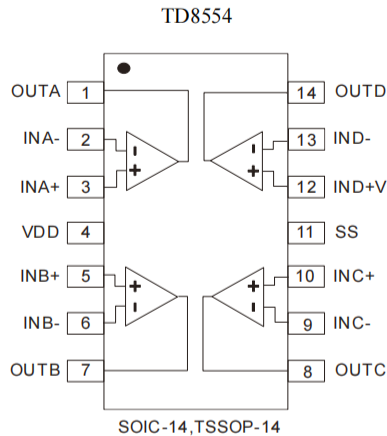
Pin Configuration and Functions (Top View)



Pin Description

NAME	PIN		I/O	DESCRIPTION
	TD8552	TD8552S		
	SOIC-8(SOP8), MSOP-8, TSSOP-8, TDFN2×2-8L,	MSOP10		
-INA	2	2	I	Inverting input, channel A
+INA	3	3	I	Noninverting input, channel A
-INB	6	8	I	Inverting input, channel B
+INB	5	7	I	Noninverting input, channel B
OUTA	1	1	O	Output, channel A
OUTB	7	9	O	Output, channel B
EnA	-	5	I	Enable pin, channel A. This pin turns the regulator on or off. Low = disabled, high = normal operation (pin must be driven)
EnB	-	6	I	Enable pin, channel A. This pin turns the regulator on or off. Low = disabled, high = normal operation (pin must be driven)
V-	4	4	-	Negative (lowest) power supply
V+	8	10	-	Positive (highest) power supply

Pin Configuration and Functions (Top View)



Pin Description

NAME	PIN	I/O	DESCRIPTION
	TD8554		
	SOIC-14(SOP14), TSSOP-14,		
-INA	2	I	Inverting input, channel A
+INA	3	I	Noninverting input, channel A
-INB	6	I	Inverting input, channel B
+INB	5	I	Noninverting input, channel B
-INC	9	I	Inverting input, channel C
+INC	10	I	Noninverting input, channel C
-IND	13	I	Inverting input, channel D
+IND	12	I	Noninverting input, channel D
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
OUTC	8	O	Output, channel C
OUTD	14	O	Output, channel D
V-	11	-	Negative (lowest) power supply
V+	4	-	Positive (highest) power supply

SPECIFICATIONS

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply, $V_S=(V^+) - (V^-)$		7	V
	Signal input pin (2)	(V^-)-0.5	(V^+)+0.5	
	Signal output pin (3)	(V^-)-0.5	(V^+)+0.5	
Current	Signal input pin (2)	-10	10	mA
	Signal output pin (3)	-120	120	mA
	Output short-circuit (4)	Continuous		
Temperature	Operating range, T_A	-40	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	-65	150	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.

(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5V beyond the supply rails should be current-limited to ± 20 mA or less.

(4) Short-circuit to ground, one amplifier per package.

ESD Ratings

			VALUE	UNIT
V(ESD)	Electrostatic discharge	Human-body model (HBM)	± 8000	V
		Machine Model (MM)	± 400	

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, $V_S=(V^+) - (V^-)$	Single-supply	1.8		5.5	V
	Dual-supply	± 0.9		± 2.75	

Thermal Information: TD8551

THERMAL METRIC ⁽¹⁾		TD8551				UNIT
		5PINS		8PINS		
		SOT23-5	SOT23-6	SOIC-8	MSOP8	
R _{ΘJA}	Junction-to-ambient thermal resistance	273.8	187.3	116	165	°C/W
R _{ΘJC(top)}	Junction-to-case(top) thermal resistance	126.8	126.5	60	53	°C/W
R _{ΘJB}	Junction-to-board thermal resistance	85.9	32.6	56	87	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	10.9	24.1	12.8	4.9	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	84.9	32.1	98.3	85	°C/W
R _{ΘJC(bot)}	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

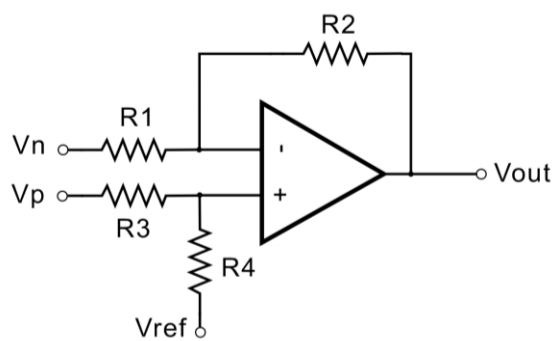
Thermal Information: TD8552

THERMAL METRIC ⁽¹⁾		TD8552						UNIT
		8PINS						
		SOIC-8	MSOP-8	TSSOP-8	MSOP-10	TDFN2 × 2-8L	TDFN33 × 2-8L	
R _{ΘJA}	Junction-to-ambient thermal resistance	116	165	200.7	169.5	80.1	66.9	°C/W
R _{ΘJC(top)}	Junction-to-case(top) thermal resistance	60	53	95.4	84.1	100	54.5	°C/W
R _{ΘJB}	Junction-to-board thermal resistance	56	87	128.6	113	45	40.4	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	12.8	4.9	27.2	15.8	6.8	1.9	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	98.3	85	127.2	111.6	45.2	40.4	°C/W
R _{ΘJC(bot)}	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	°C/W

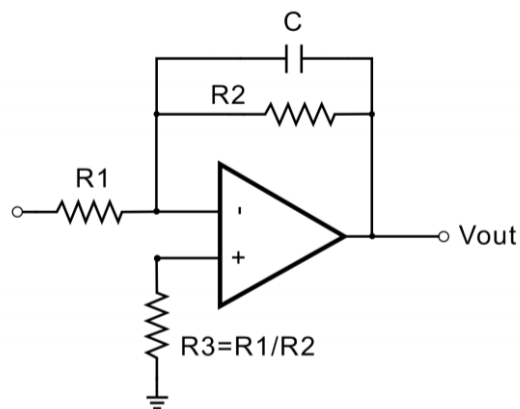
Thermal Information: TD8554

THERMAL METRIC ⁽¹⁾		TD8554		UNIT
		14PINS		
		SOIC-14	TSSOP-14	
R _{ΘJA}	Junction-to-ambient thermal resistance	83.8	120.8	°C/W
R _{ΘJC(top)}	Junction-to-case(top) thermal resistance	70.7	34.3	°C/W
R _{ΘJB}	Junction-to-board thermal resistance	59.5	62.8	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	11.6	1	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	37.7	56.5	°C/W
R _{ΘJC(bot)}	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

Typical Application Circuit



Difference Amplifier



Low Pass Active Filter

Electrical Characteristics: VS = +5V

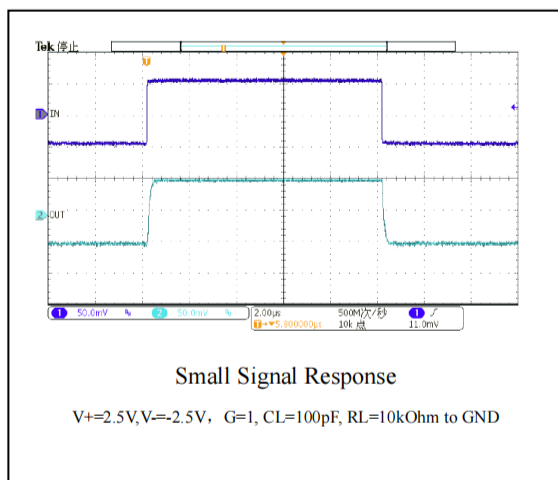
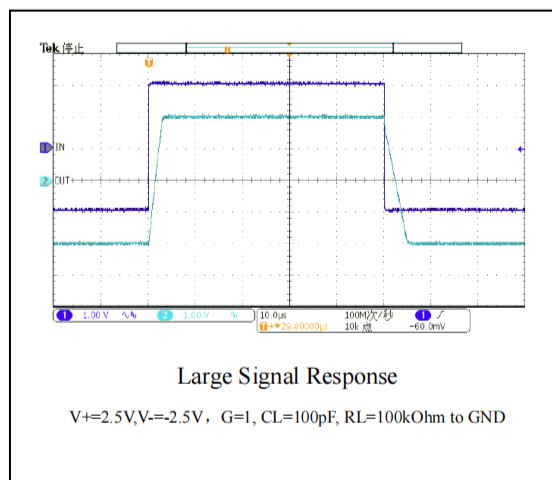
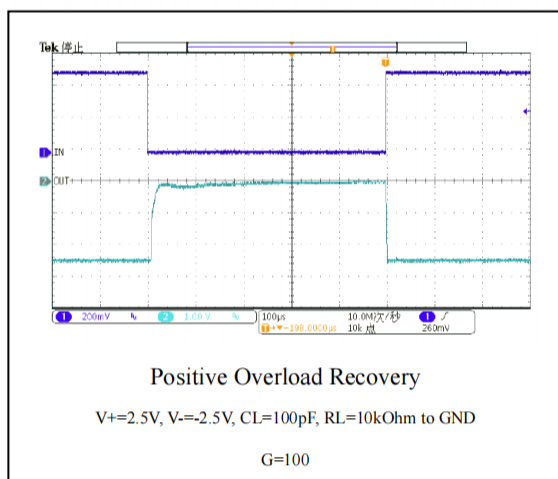
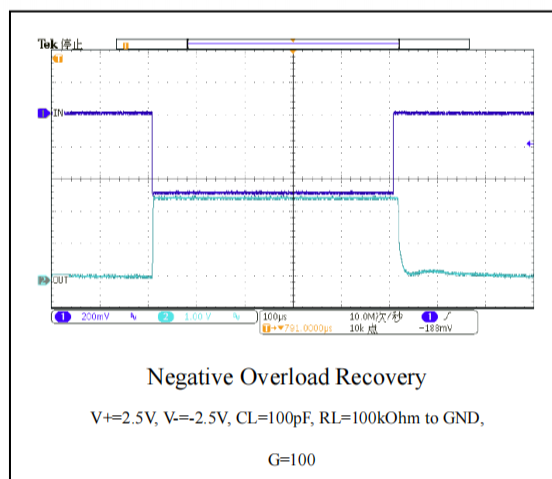
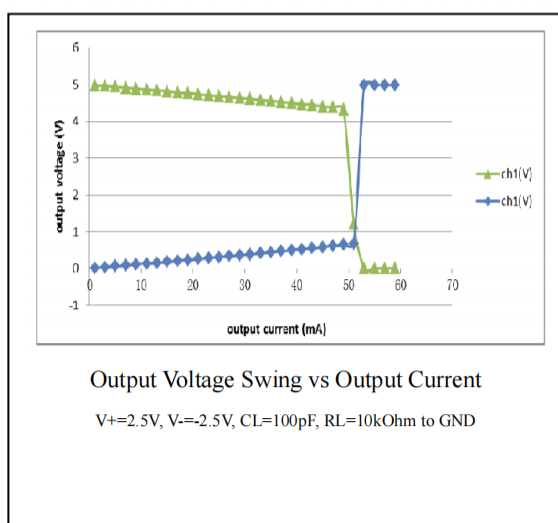
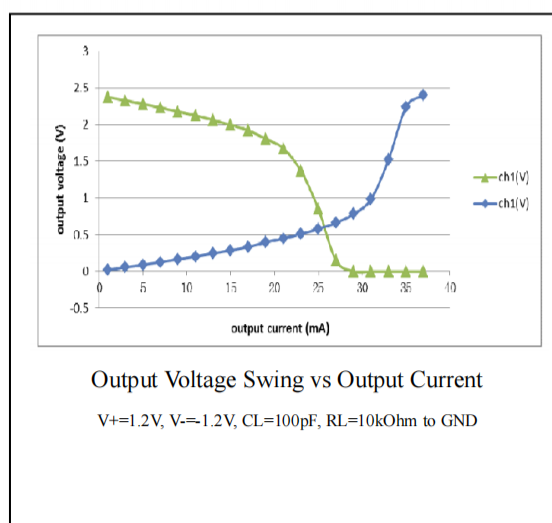
(At VS = 5V, TA = +25°C, RL = 100kΩ connected to Vs/2, unless otherwise noted)

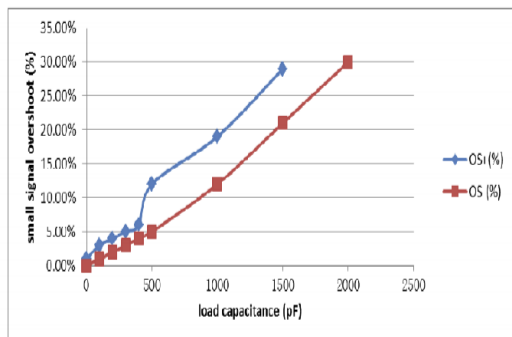
Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DYNAMIC PERFORMANCE					
Gain-Bandwidth Product (GBP)	RL = 100kΩ		1.7		MHz
Slew Rate	CL=60Pf, G=+1		1		V/us
Positive Overload Recovery Time	Gain=-100X, VIN=500mVpp		8		us
Negative Overload Recovery Time	Gain=-100X, VIN=500mVpp		9		us
DC PERFORMANCE					
Input Offset Voltage (VOS)	VCM = 2.5V		1	5	uV
Input Offset Voltage Drift	RL = 100kΩ, VOUT = 0.15V to 4.85V		0.005		uV/deg
Large Signal Voltage Gain (AVO)			130		dB
INPUT CHARACTERISTICS					
Input Common Mode Voltage Range (VCM)	G=101, V+=2.5/0.9	-0.1		+0.1	V
Common Mode Rejection Ratio (CMRR)	V-=2.5/0.9V		125		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing from Rail	RL=10K		30	50	mV
	RL=10K, TA=-40°C to 125°C		70	70	mV
Output Current (IOUT)	VCC=5V		46		mA
POWER SUPPLY					
Operating Voltage Range	IOUT = 0mA	1.8		5.5	V
Quiescent Current (per Amplifier)	VS = 5V,		0.43		mA
Power Supply Rejection Ratio (PSRR)	VCM = (-VS) + 0.5V		130		dB
NOISE/DISTORTION PERFORMANCE					
Voltage Noise Density (en)	f=10kHz		40		nV/rtHz
Total Harmonic Distortion (THD)	V+=5V, Vo=1Vpp 1KHz		0.006		%

Note 1: Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Typical Performance Characteristics

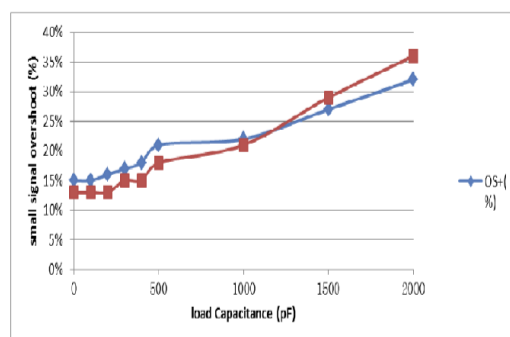
At $T_A = +25^\circ\text{C}$, $V_S = \pm 2.5\text{V}$, $R_L = 10\text{k}\Omega$ connected to GND, unless otherwise noted.





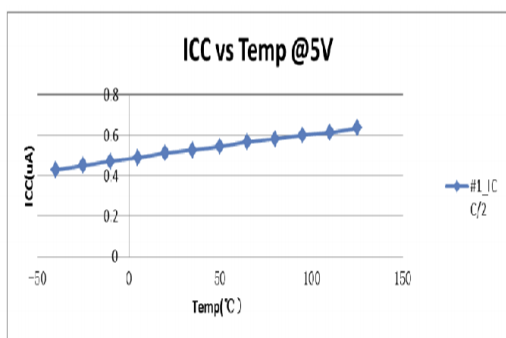
Overshoot (OS) vs Load Capacitance

V+=2.5V, V-=-2.5V, RL=10kOhm to GND



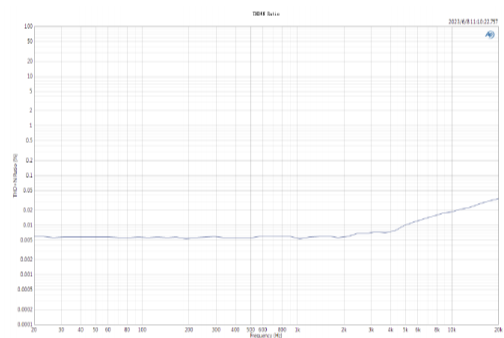
Overshoot (OS) vs Load Capacitance

V+=1.2V, V-=-1.2V, RL=10kOhm to GND



ICC vs Temp

V+=2.5V, V-=-2.5V, CL=100pf RL=10kOhm to GND



THD vs Frequency

V+=2.5V, V-=-2.5V, Vin=1Vpp, CL=100pf RL=10kOhm to GND

Power Supply Layout and Bypass

The TD855X OPA's power supply pin (VDD for single-supply) should have a local bypass capacitor (i.e., 0.01 μ F to 0.1 μ F) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1 μ F or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts. Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA's inputs and outputs. To decrease stray capacitance, minimize PC board lengths and resistor leads, and place external components as close to the op amps' pins as possible.

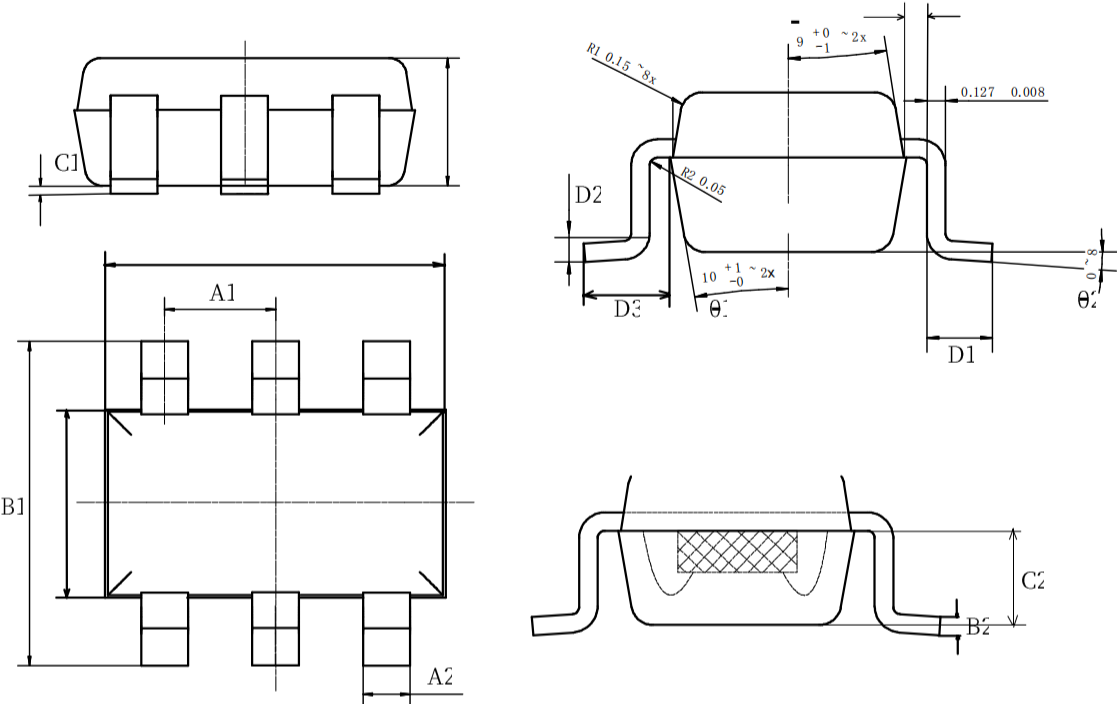
Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board. Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the feedback voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

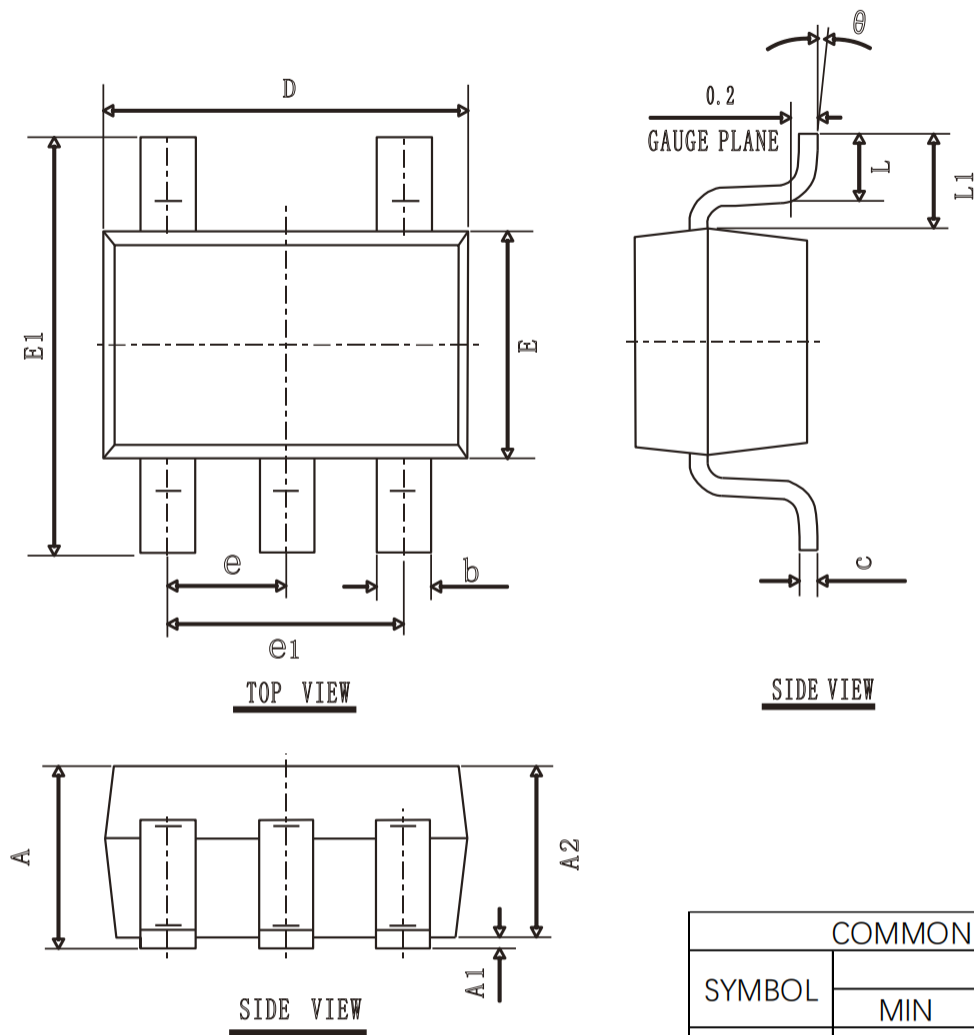
The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

Package Outline And Physical Dimensions: SOT23-6L



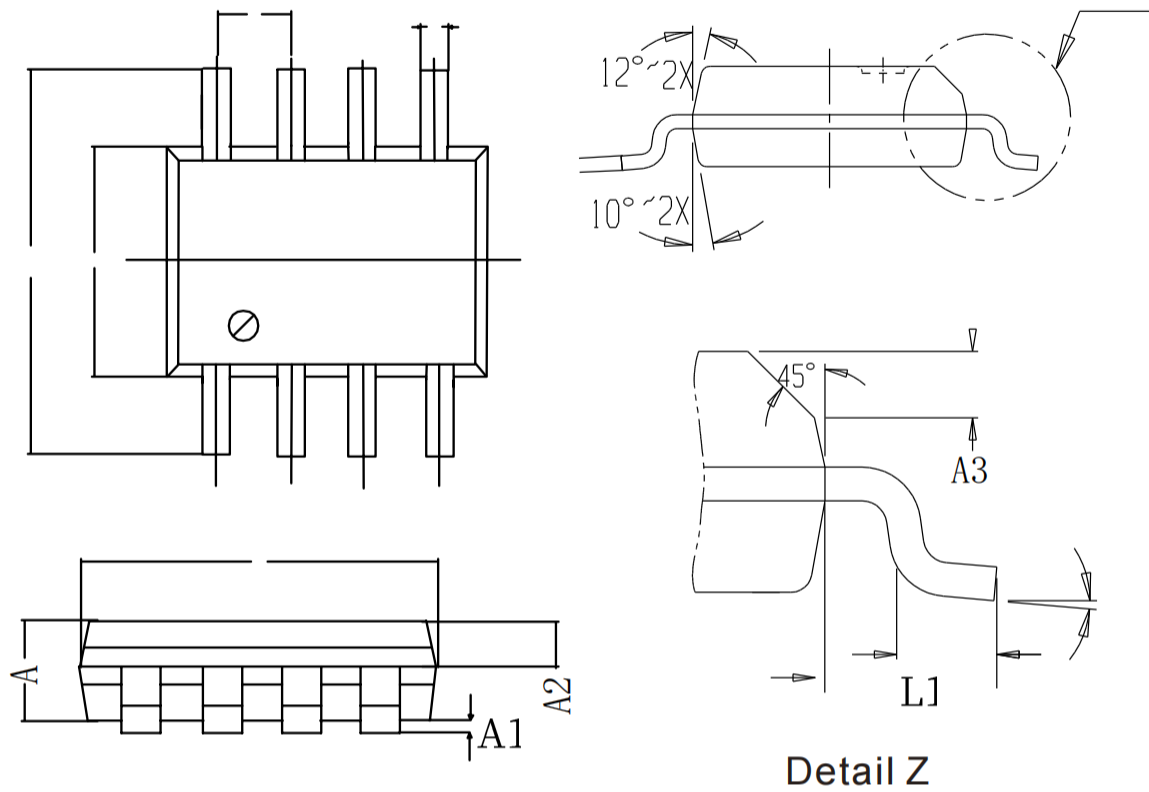
COMMON DIMENSIONS			
SYMBOL	MILLIMETER		
	MIN	MID	MAX
A	2.82	2.92	3.02
A1	0.90	0.95	1.00
A2	0.38	0.44	0.50
B	1.52	1.62	1.72
B1	2.80	2.95	3.10
B2	0.12	0.13	0.135
C	1.05	1.10	1.15
C1	0.03	0.08	0.13
C2	0.60	0.65	0.70
D	0.03	0.08	0.13
D1	0.40	0.45	0.50
D2	0.25 TYP		
D3	0.60	0.65	0.70

Package Outline And Physical Dimensions: SOT353 (SC70-5)



COMMON DIMENSIONS			
SYMBOL	MILLIMETER		
	MIN	MID	MAX
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.90	0.95	1.00
b	0.20	0.25	0.30
c	0.08	0.10	0.15
e1	1.20	1.30	1.40
D	2.00	2.10	2.20
E	1.15	1.25	1.35
E1	2.15	2.30	2.45
L	0.26	0.36	0.46
θ	0°	4°	6°
L1	0.525 REF		
e	0.65 TYP		

Package Outline And Physical Dimensions: SOP8 (SOIC8)

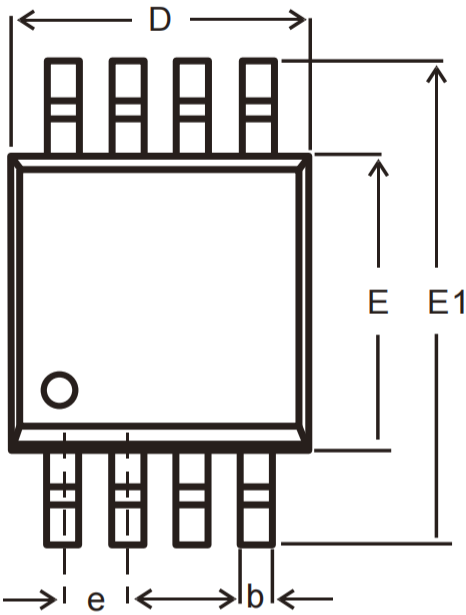


机械尺寸/mm			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	1.35	1.45	1.55
A1	0.00	0.05	0.10
A2	0.65	0.70	0.75
A3	0.35	0.40	0.45
b	0.35	0.40	0.45
c	0.18	0.20	0.22
D	4.70	4.90	5.10
e	—	1.27 TYP	—
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
L	0.40	0.60	0.80
Q	0°	—	8°
L1	1.05 REF		

Package Outline And Physical Dimensions: MSOP-8

TOPVIEW

正视图



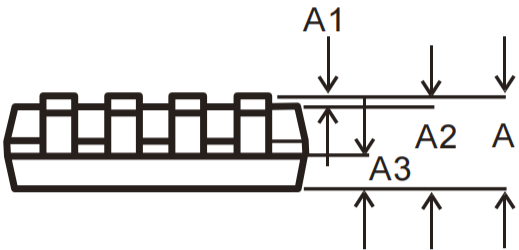
SIDE VIEW

侧视图



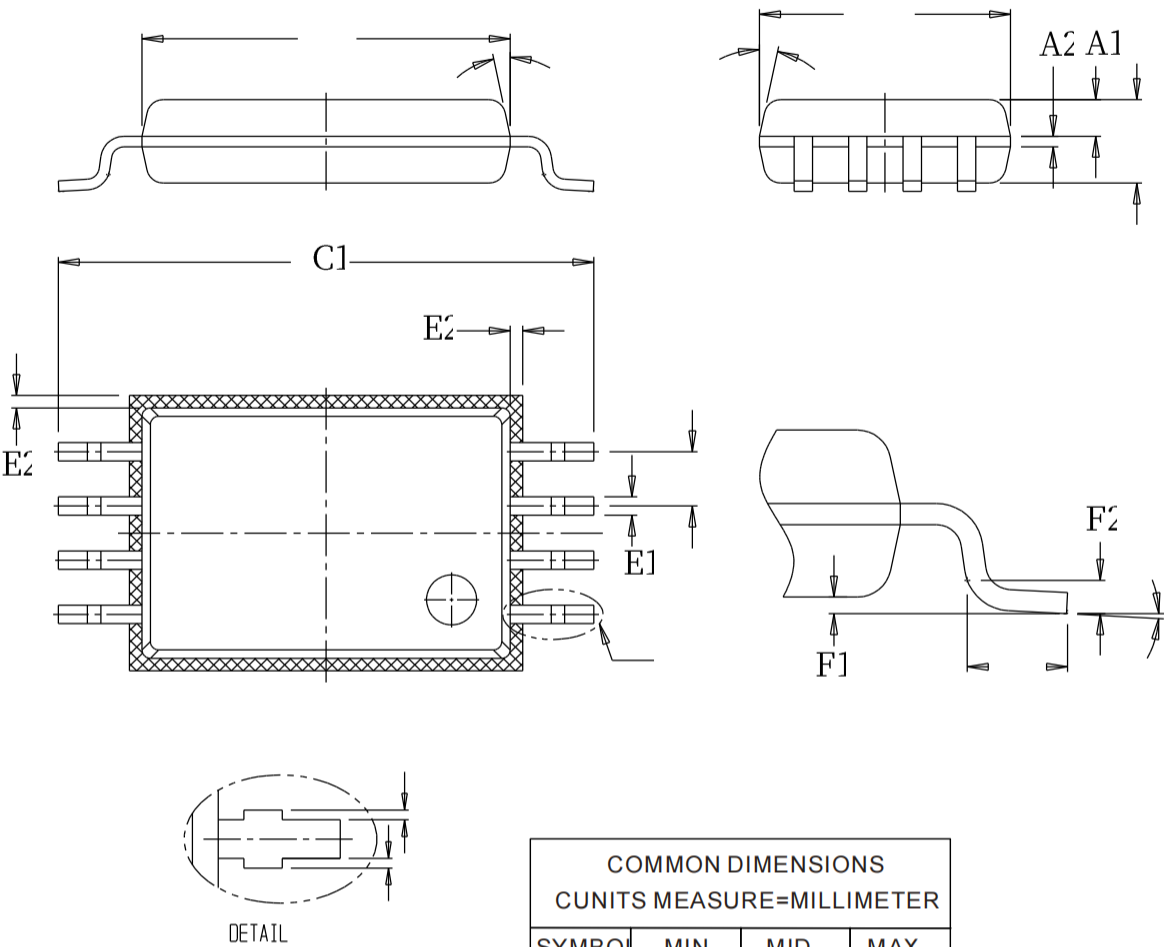
SIDE VIEW

侧视图



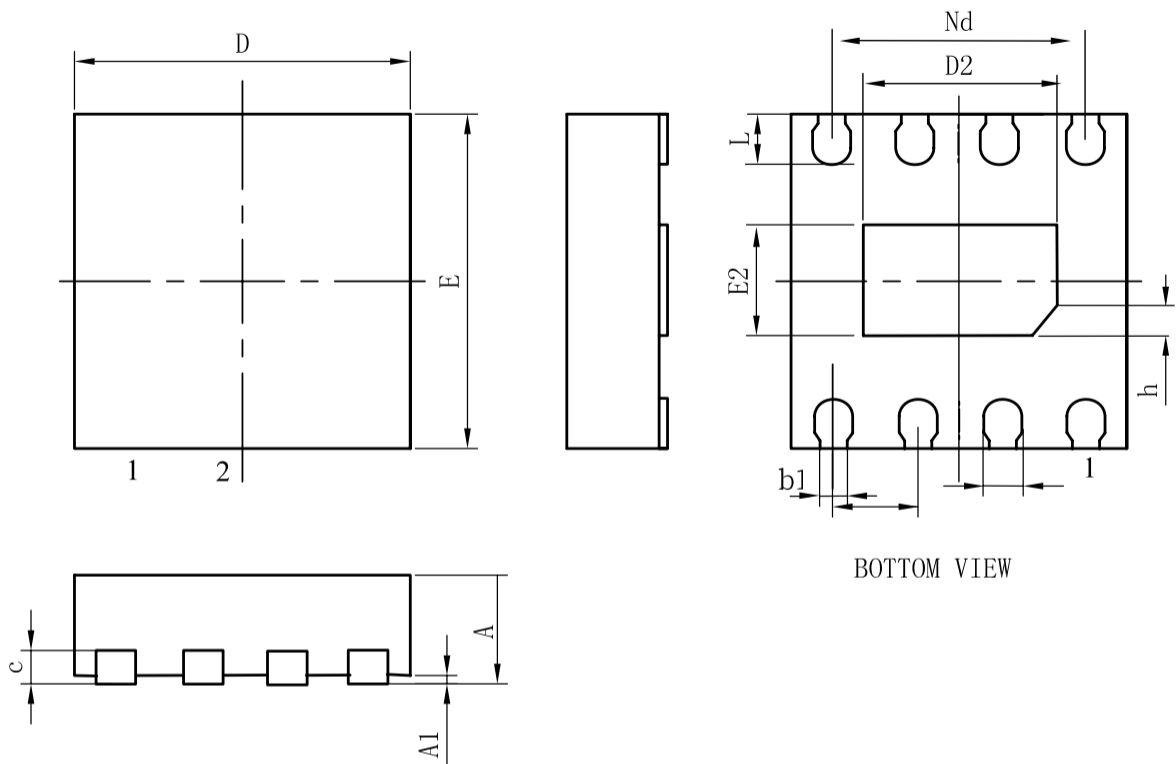
机械尺寸/mm			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	—	—	1.10
A1	0.05	—	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	—	0.36
c	0.15	—	0.19
D	2.90	3.00	3.10
E	2.90	3.00	3.10
E1	4.70	4.90	5.10
e	0.65 BSC		
L1	0.95 REF		
L	0.40	—	0.70
θ	0°	—	8°

Package Outline And Physical Dimensions: TSSOP8



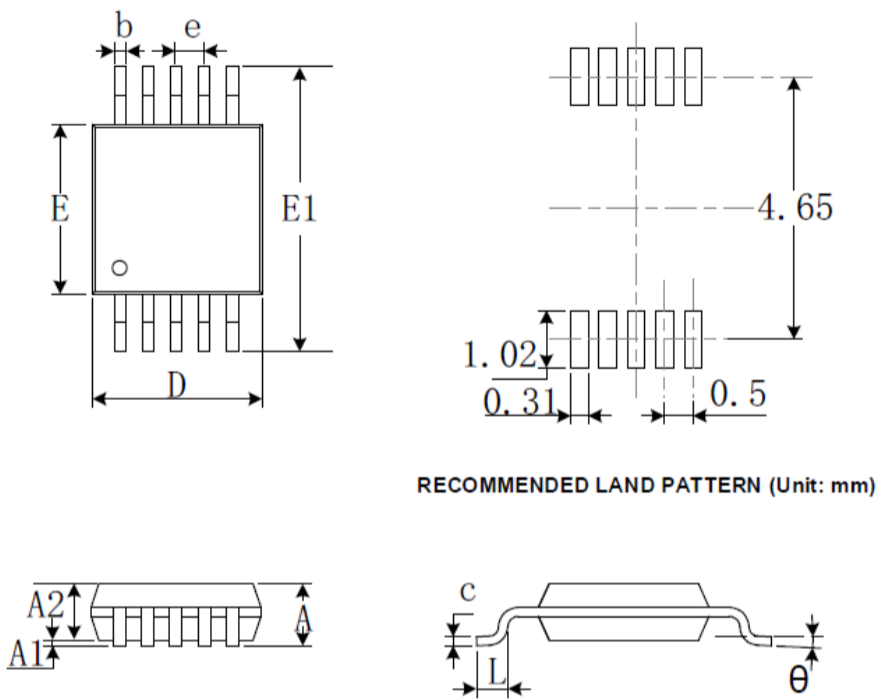
COMMON DIMENSIONS			
CUNITS MEASURE=MILLIMETER			
SYMBOL	MIN	MID	MAX
A	0.95	1.00	1.05
A1	0.39	0.44	0.49
A2	-	0.127	-
B	2.95	3.00	3.05
C	4.35	4.40	4.45
C1	6.30	6.40	6.50
E	-	0.65 TYP	-
E1	0.195	0.22	0.245
E2	-	0.12	-
F	0.5	0.60	0.7
F1	0	0.05	0.1
F2	-	0.2	-
G	-	0.075	-
I	10	12	14
J	0	3	6

Package Outline And Physical Dimensions: DFN2020×0.75-8L(TDFN -2x2-8L)



COMMON DIMENSIONS			
SYMBOL	MILLIMETER		
	MIN	MID	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.24	0.29	0.34
b1	0.13	0.18	0.23
c	0.18	0.20	0.25
D	1.95	2.00	2.05
D2	1.10	1.20	1.30
e	0.50 BSC		
Nd	1.50 BSC		
E	1.95	2.00	2.05
E2	0.60	0.70	0.80
L	0.20	0.30	0.40
h	0.15	0.20	0.25
载体尺寸	43*70		

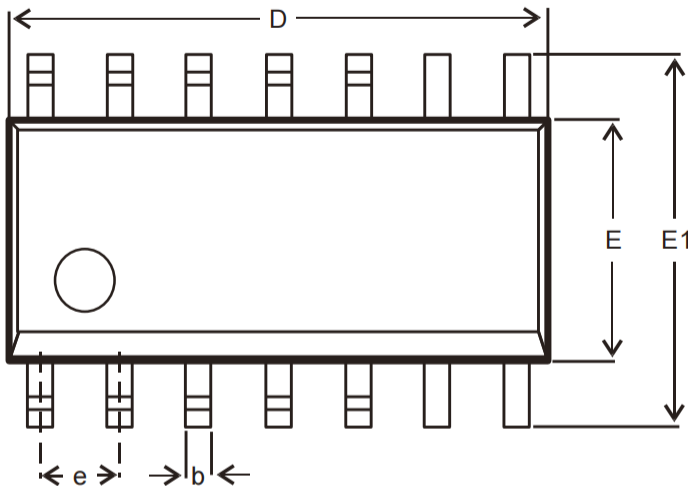
Package Outline And Physical Dimensions: MSOP-10



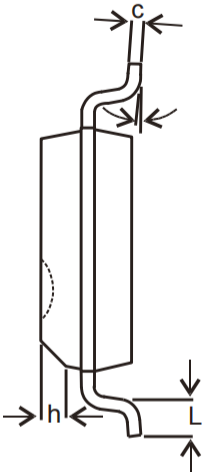
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.50(BSC)		0.020(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

Package Outline And Physical Dimensions: TSSOP-14

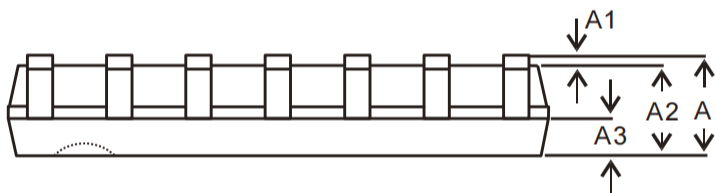
TOP VIEW
正视图



SIDE VIEW
侧视图



SIDE VIEW
侧视图

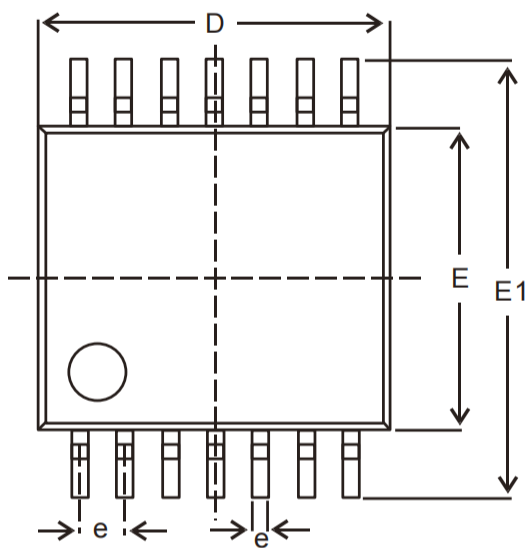


机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	—	—	1.75
A1	0.10	0.15	0.25
A2	1.35	1.45	1.55
A3	0.60	0.65	0.70
b	0.35	—	0.50
c	0.19	—	0.25
D	8.50	8.60	8.70
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	1.27 BSC		
h	0.30	—	0.50
L	0.40	—	0.80
θ	0°	—	8°

Package Outline And Physical Dimensions: TSSOP-14

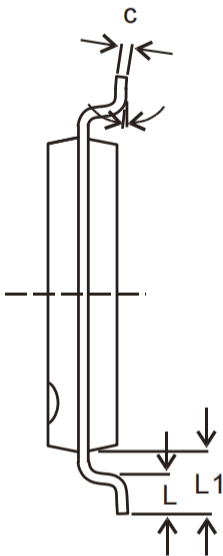
TOP VIEW

正视图



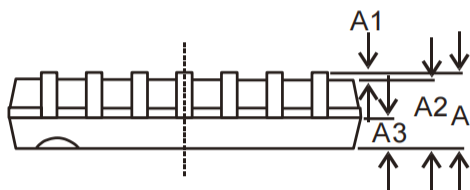
SIDE VIEW

侧视图



SIDE VIEW

侧视图



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
c	0.13	—	0.17
D	4.90	5.00	5.10
E	4.30	4.40	4.50
E1	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
θ	0°	—	8°