Description

The SWPQ202 devices are low phase noise quartz-based PLL oscillators supporting a large range of frequencies and output interface
types. These devices are designed to operate at three different power supplies and are available in multiple package sizes as well as temperature grades.

With a patented one-time program (OTP) allowing for infinite memory shelf life, the SWPQ202 devices can be programmed to generate an output frequency from 1MHz to 1250MHz with a resolution as low as 1Hz accuracy. The configuration capability of this family of devices allows for fast delivery times for both sample and large
production orders.

Pin Assignments

Note: To minimize power supply line noise, a 0.01µF bypass capacitor should be placed between V_{DD} (Pin 6) and GND (Pin 3).

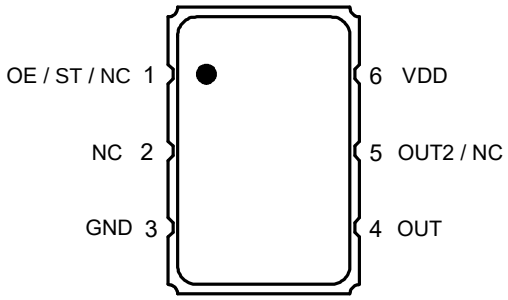


Table 1. Pin Description

Pin #	Name	Description
1	OE ST NC	Enable/Disable Standby No connect
2	NC	No connect
3	GND	Connect to ground
4	OUT1	Output
5	OUT2 NC	Output No connect
6	V_{DD}	Supply voltage

[a] Pulled high internally = output enabled.

[b] Low = output disabled.

See Ordering Information for more details.

Features

- Frequency range: 1MHz to 1250MHz
  LVCMOS：1MHz~350MHz
  HCSL： 1MHz~500MHz
  LVPECL,LVDS,CML：1MHz~1250MHz
- Output types: LVDS, LVPECL, LVCMOS, CML,HCSL
- Supply voltage options: 1.8V, 2.5V, or 3.3V
  1.8V options: LVDS, CML, HCSL
  2.5V/3.3V options: LVPECL, LVDS, CML, HCSL
- Phase jitter (12kHz to 20MHz): 1pS Max
- Package options:
  • 2.5 × 2.0 × 1.2 mm
  • 3.2 × 2.5 × 1.2 mm
  • 5.0 × 3.2 × 1.3 mm
  • 7.0 × 5.0 × 1.6mm
- Frequency stability options: ±25, ±50, or ±100ppm
- Operating temperature: -40°C to +85°C
- Operating temperature: -40°C to +105°C

Ordering Information

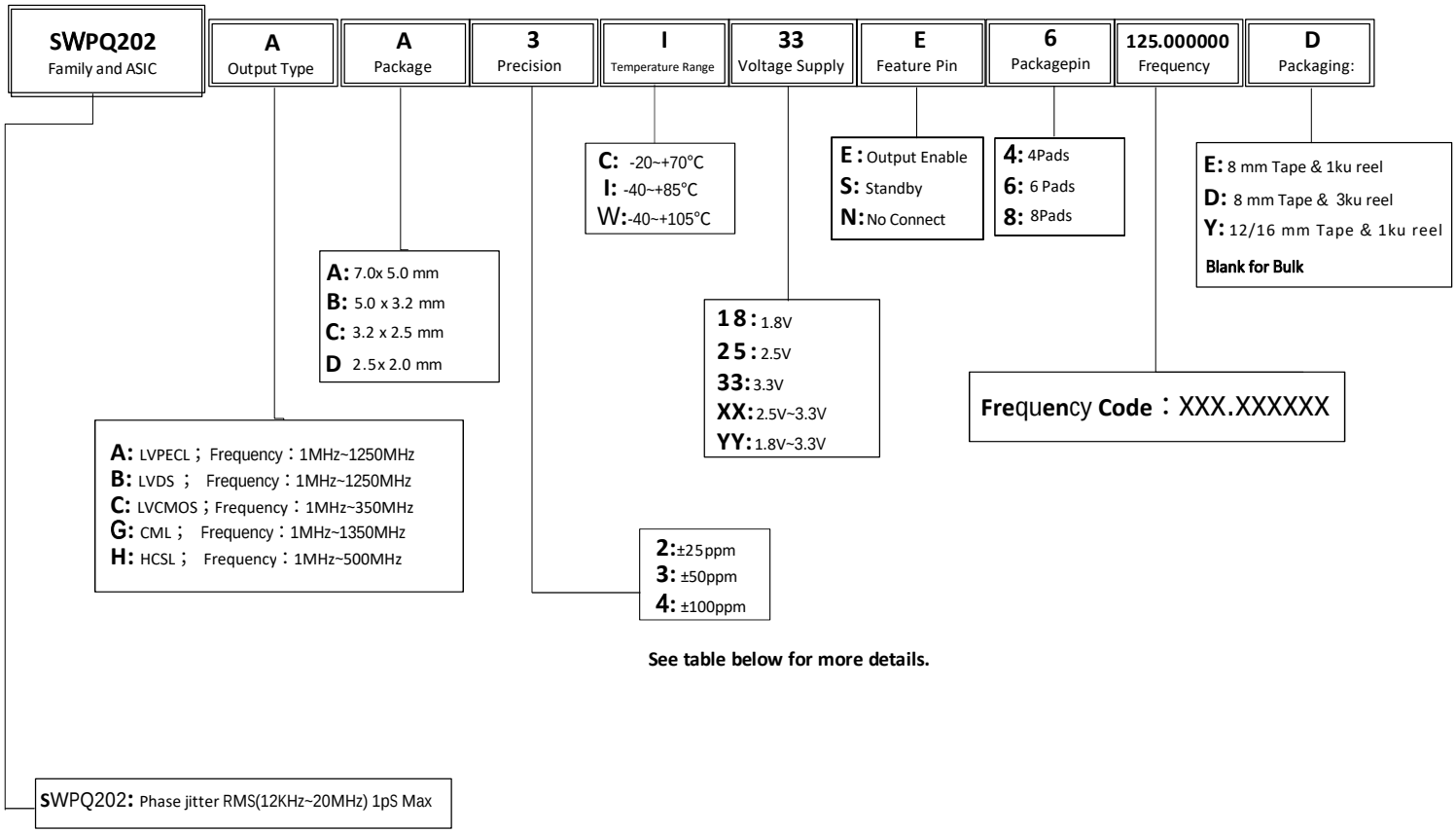


Table 2. Frequency Stability and Operating Temperature Decoder

"Precision" and "Temperature Range" Codes	Operating Temperature		Frequency Stability	
		Minimum	Maximum	Units
"2" and "C"	-20°C to +70°C	-25	+25	ppm
"2" and "V"	-40°C to +85°C	-25	+25	ppm
"3" and "V"	-40°C to +85°C	-50	+50	ppm
"4" and "V"	-40°C to +85°C	-100	+100	ppm
"3" and "W"	-40° to +105°C	-50	+50	ppm
"4" and "W"	-40° to +105°C	-100	+100	ppm

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the device. The ratings, which are standard values for Starwave commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 3. Absolute Maximum Ratings

Item	Rating			
V_{DD}	-0.5 to +5.0V			
E/D	-0.5V to V_{DD} + 0.5V			
OUT	-0.5V to V_{DD} + 0.5V			
Storage Temperature	-55°C to 125°C			
Maximum Junction Temperature	105°C			
Core Current	30mA maximum (LVCMOS 10MHz~200MHz)			
Theta J_A	JU6	75.9 °C/W	JS6	89.6 °C/W
Theta J_B		48.6°C/W		54.3 °C/W

ESD Compliance

Table 4. ESD Compliance

Human Body Model (HBM)	1000V

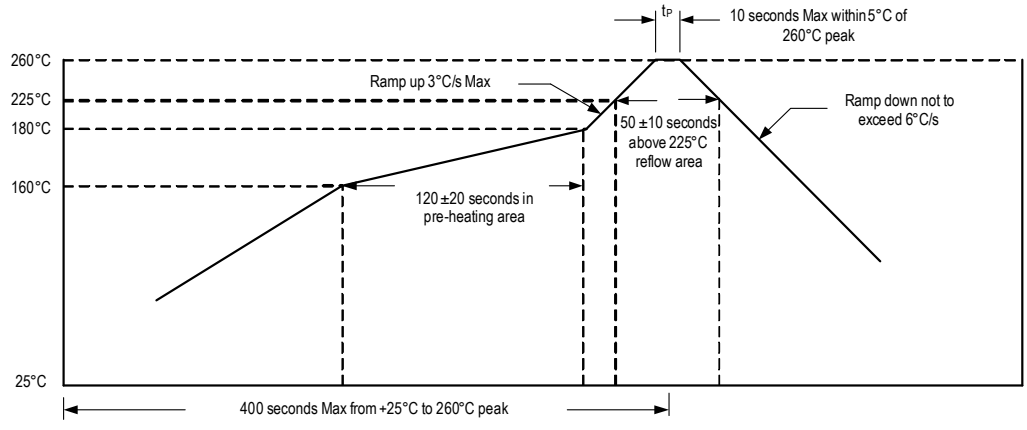
Mechanical Testing

Table 5. Mechanical Testing *

Parameter	Test Method
Mechanical Shock	Half-sine wave with 0.3ms 3000G. X, Y, Z each direction 1 time.
Mechanical Vibration	Frequency: 10 – 55MHz amplitude: 1.5mm. Frequency: 55 – 2000Hz peak value: 20G. Duration time: 4H for each X,Y,Z axis; total 12hours.
High Temp Operating Life (HTOL)	2000 hours at 125°C (under power).
Hermetic Seal	Gross leak (air leak test). Fine leak (Helium leak test) He-pressure: 6kgf/cm² 2 hours.

* MSL level does not apply.

Solder Reflow Profile



Output Waveforms

Figure 1. LVDS Output Waveforms

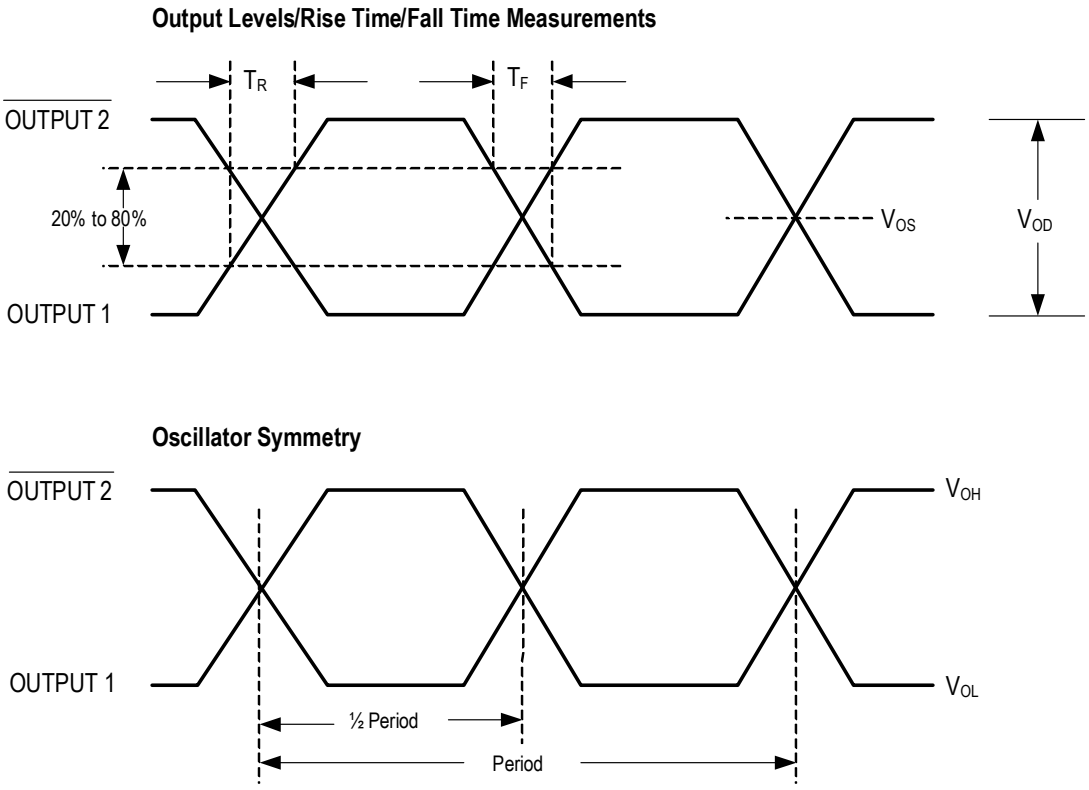


Figure 2. LVPECL Output Waveforms

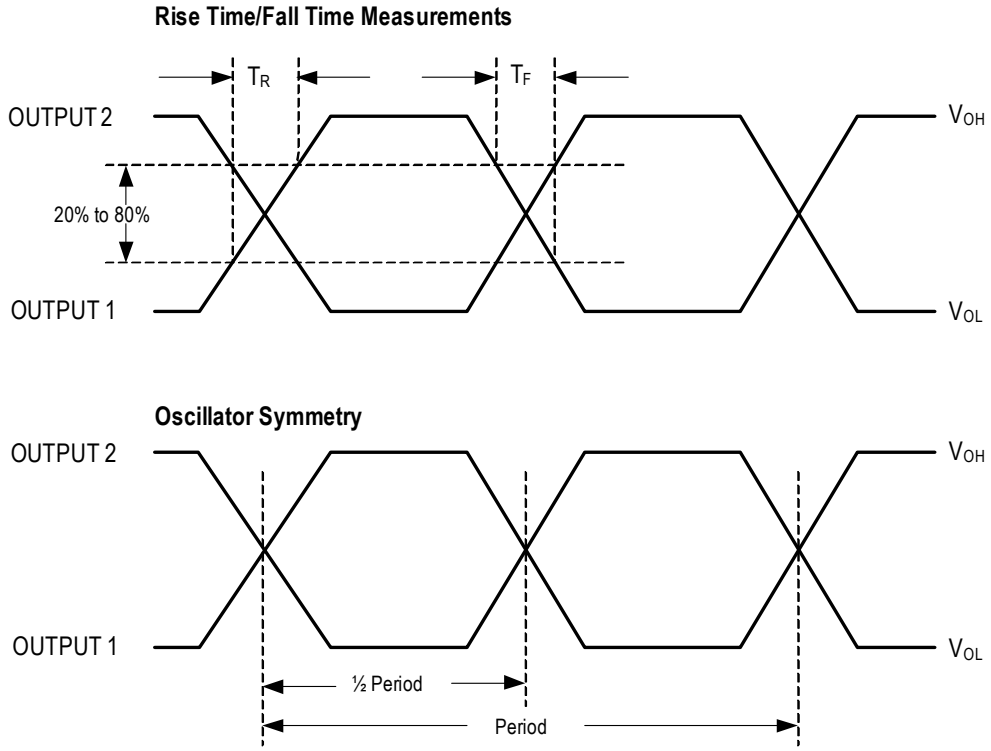
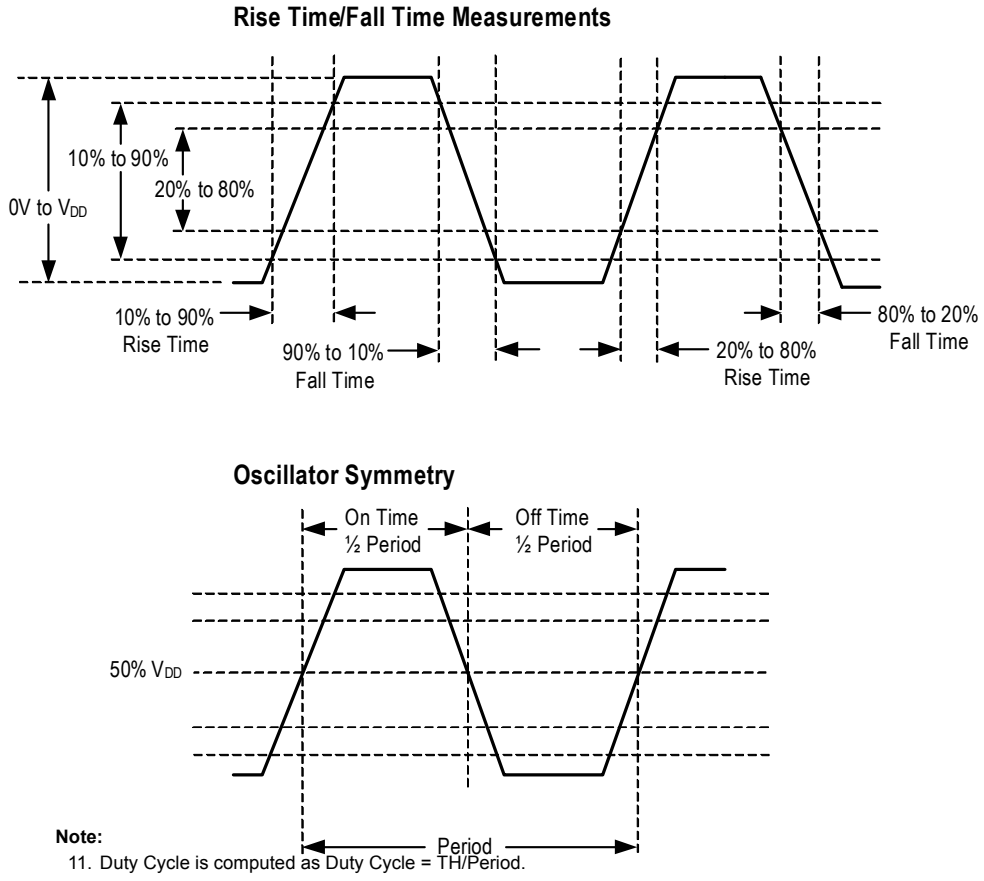


Figure 3. LVCMOS Output Waveformsms



Note:
11. Duty Cycle is computed as Duty Cycle = TH/Period.

Figure 4. HCSL Typical Termination

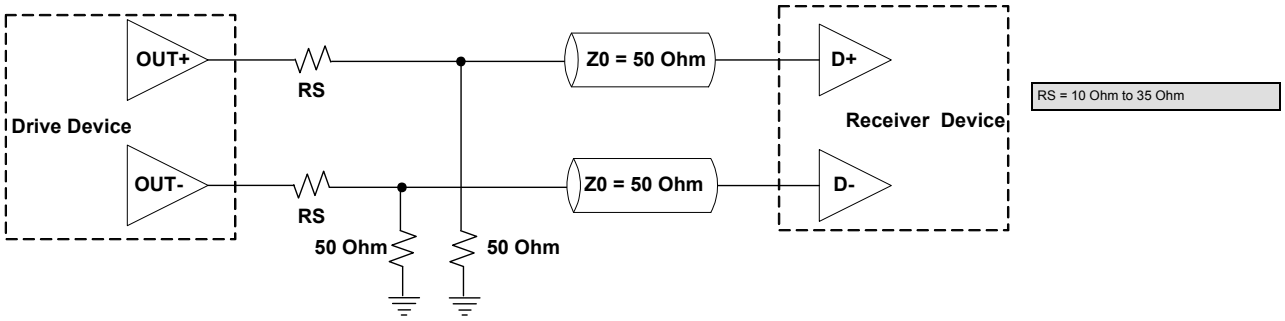


Figure 5. **CML Single Load Termination**

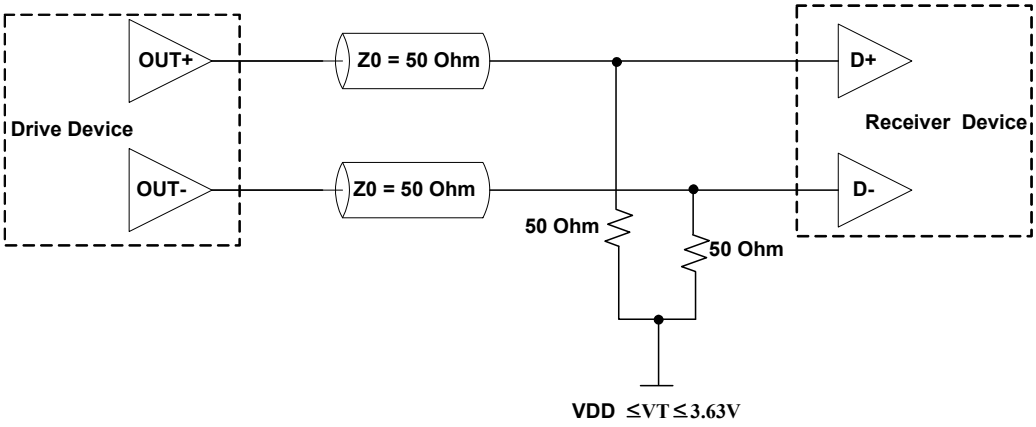
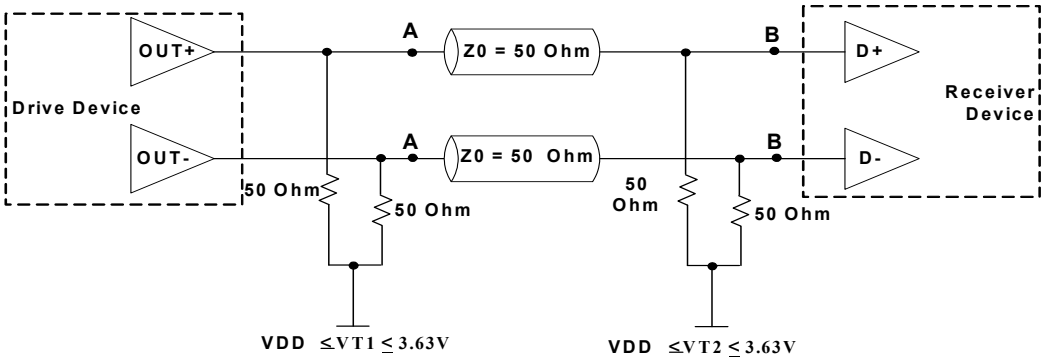
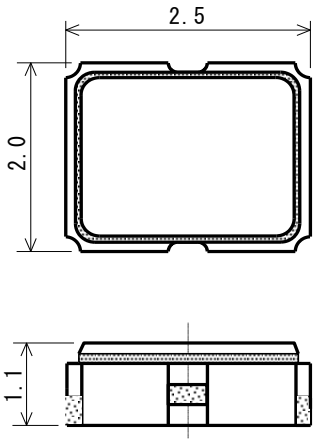


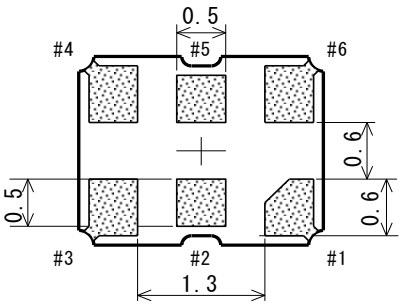
Figure 6. **CML Double Load Termination**

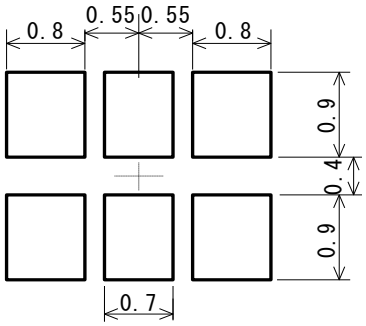


Notes:
1. For DC-coupled operation, VT1 = VT2
2. For AC coupled operation, include/insert decoupling caps at points A or B
2. For AC-coupled operation with capacitors placed at point A, VT2 sets the input common mode of Receiver Device and need not to be related to VT1

Dimensions

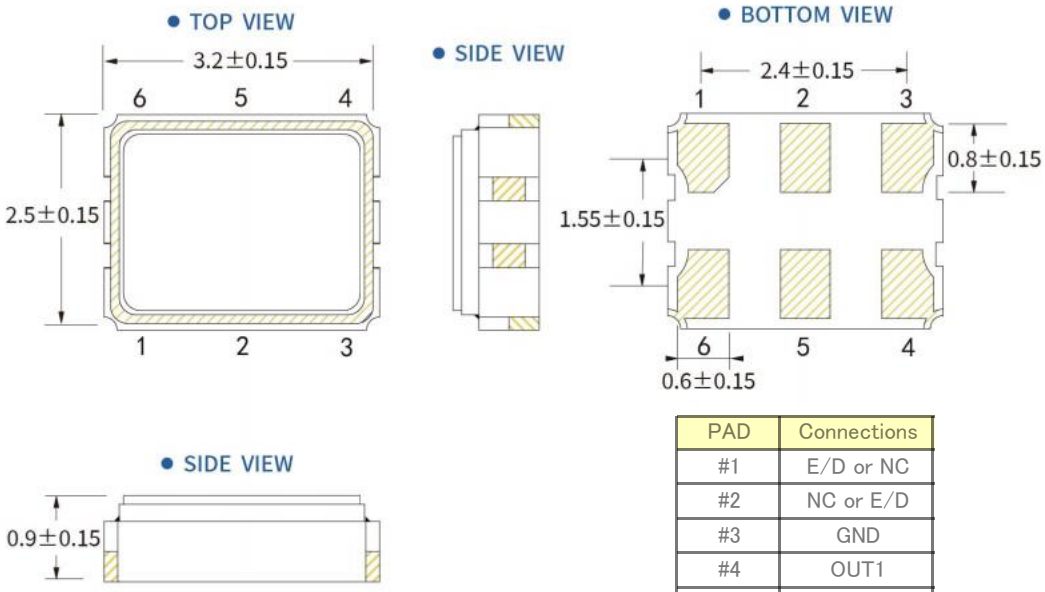






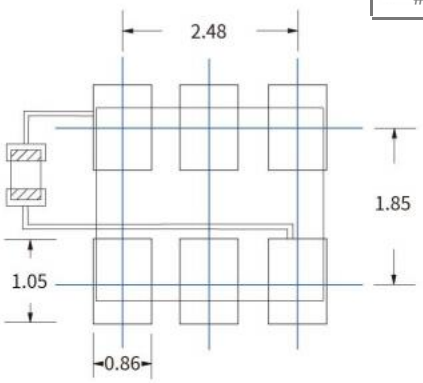
PAD	Connections
#1	E/D or NC
#2	NC or E/D
#3	GND
#4	OUT1
#5	OUT2
#6	Vcc

Dimensions



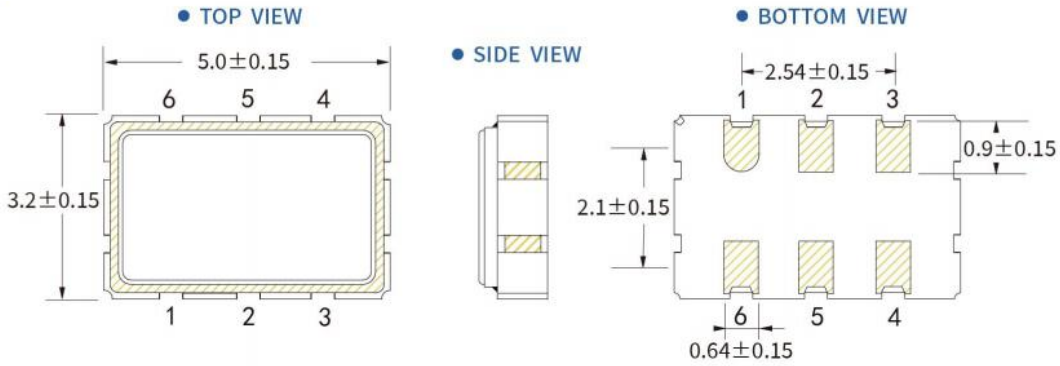
PAD	Connections
#1	E/D or NC
#2	NC or E/D
#3	GND
#4	OUT1
#5	OUT2
#6	Vcc

Solder pad layout (UNIT:mm)



To ensure optimal oscillator performance,place a by-pass capacitor of 0.1µF as close to the part as possible between Vdd and GND pads.

Dimensions



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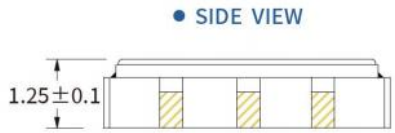
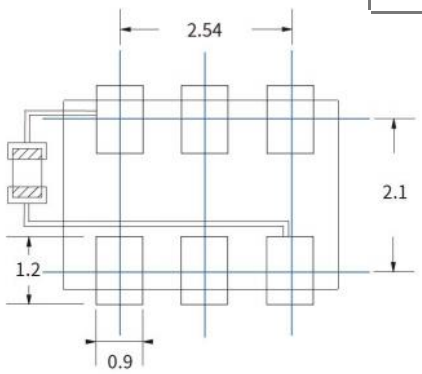


Solder pad layout (UNIT:mm)



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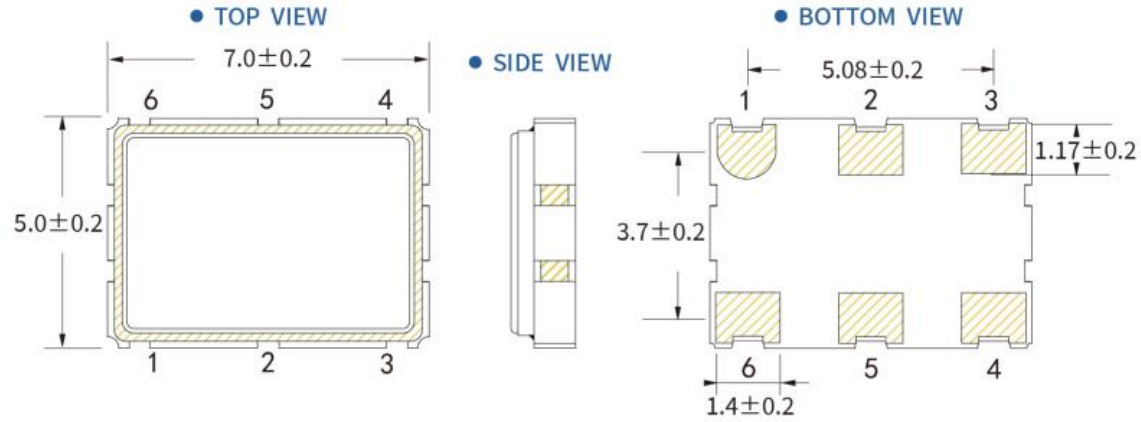

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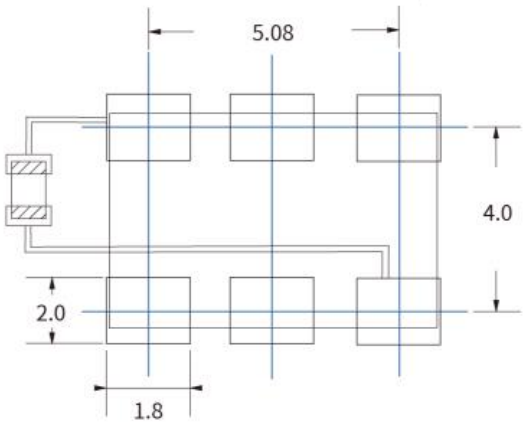
Solder pad layout (UNIT:mm)



To ensure optimal oscillator performance,place a by-pass capacitor of 0.1µF as close to the part as possible between Vdd and GND pads.

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