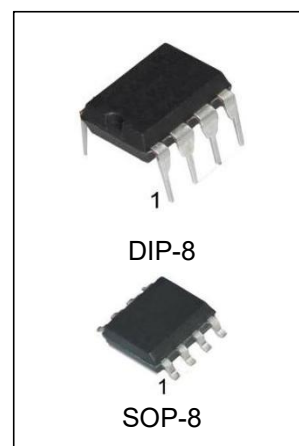


CURRENT MODE PWM CONTROLLER

FEATURES

- Optimized for off-line and DC to DC converts
- Low start up current (<0.5mA)
- Automatic feed forward compensation
- Pulse-by-Pulse current limiting
- Enhanced load response characteristics
- Under-voltage lockout with hysteresis
- Double pulse Suppression
- High current totem pole output
- Internally trimmed bandgap reference
- 500kHz operation



ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
UC2842BN	DIP-8	UC2842B,2842B	TUBE	2000pcs/Box
UC2842BM/TR	SOP-8	UC2842B,2842B	REEL	2500pcs/Reel

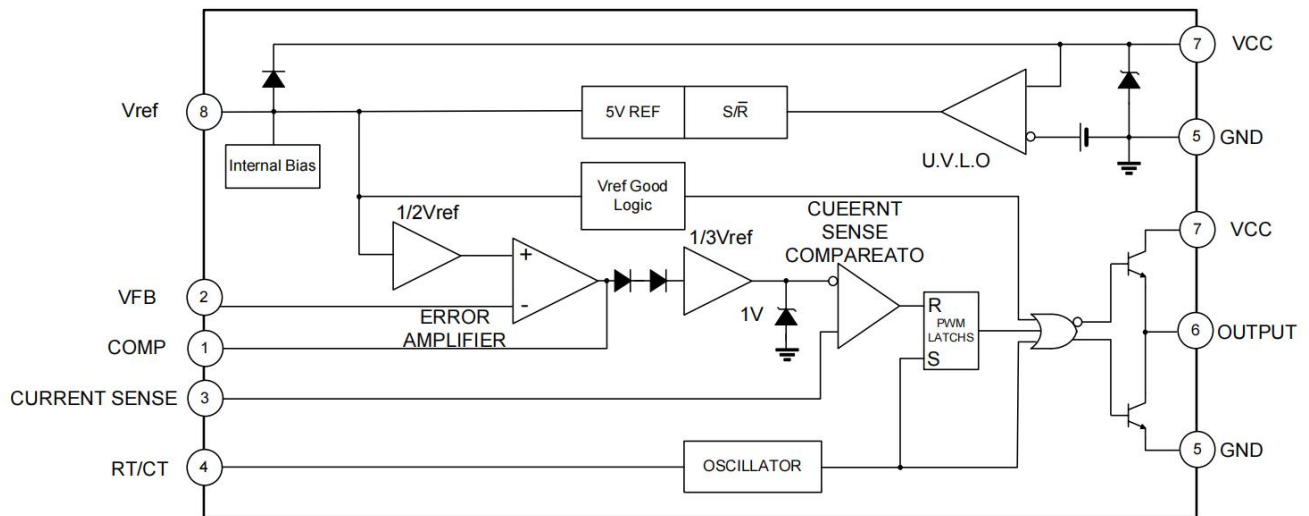
DESCRIPTION

The UC2842B provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 0.5mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N channel MOSFETs, is low in the off state.

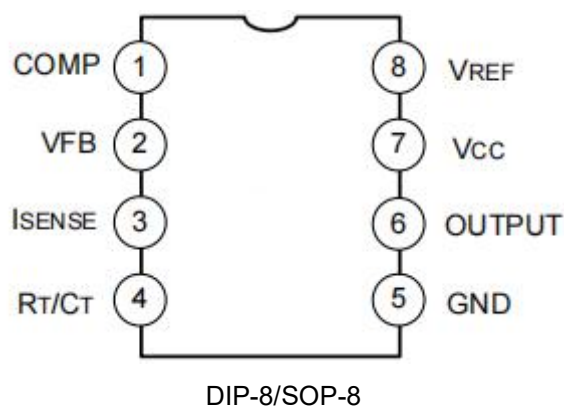
APPLICATIONS

- Power converter

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Pin Description
1	COMP	I/O	Error amplifier compensation pin
2	VFB	I	Error amplifier input
3	I _{SENSE}	I	Current sense comparator input
4	R _T / C _T	I/O	Oscillator RC input
5	GND	/	Device power supply ground terminal
6	OUTPUT	O	PWM Output
7	V _{CC}	/	Device positive voltage supply
8	V _{REF}	O	Oscillator voltage reference

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Rating	Unit
Supply Voltage	VCC	30	V
Output Current	Io	±1	A
Output Energy (capacitive Load)	W	5	μJ
Analog Inputs (pin 2,3)	VI(ANA)	-0.3 to +6.3	V
Error Amplifier Output Sink Current	ISINK(EA)	10	mA
Power Dissipation at Tamb≤25°C	PD	700	mW
Thermal Resistance, Junction to Ambient	RthJA	180.6	°C/W
Junction Temperature	TJ	150	°C
Storage Temperature	Tstg	-65~+150	°C
Lead Temperature (Soldering, 10 seconds)	TL	260	°C

Note: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured.

RECOMMENDED OPERATING CONDITION

(UNLESS OTHERWISE SPECIFIED, TA=25°C)

Characteristics	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VCC	--	--	28	V
Input Voltage	RT/CT, VFB, ISENSE	0	--	5.5	V
Supply Current	ICC	--	--	25	mA
Average Output Current	Io	--	--	200	mA
Reference Output Current	Io(ref)	--	--	-20	mA
Oscillator Frequency	fosc	--	100	500	kHz
Operating free-air temperature	Ta	-40	--	105	°C

ELECTRICAL CHARACTERISTICS

(UNLESS OTHERWISE SPECIFIED, VCC=15V, Ta=-40~105°C, RT=10KΩ, CT=3.3nF)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Reference Section						
Output voltage	VREF	Ta=25°C, IL=1mA	4.95	5.00	5.05	V
Liner regulation	ΔVREF1	VCC=12V~25V	--	6	20	mV
Load regulation	ΔVREF2	IL=1mA~20mA	--	6	25	mV
Temperature stability	TS	--	--	0.2	0.4	mV/C
Total output variation	ΔVREF3	Line, Load, Temp	4.82	--	5.18	V
Output Noise Voltage	VOSC	10Hz≤f≤10kHz, Ta=25°C	--	50	--	μV
Long-term stability	S	Ta=25°C, 1000hours	--	5	25	mV
Output short circuit current	ISC	VREF=0V, Ta=25°C	-30	-100	-180	mA
Oscillator Section						
Initial Accuracy	f	Ta=25°C	49	52	55	kHz
Voltage stability	Δf/ΔVCC	VCC=12V~25V	--	0.2	1	%
Temp stability	Δf/ΔT	Tmin≤Ta≤max	--	5	--	%
Amplitude	Vosc	Vpin 4 peak to peak	--	1.6	--	V

Error amplifier Section						
Input Voltage	V _{I(EA)}	V _{pin 1} =2.5V	2.42	2.50	2.58	V
Input Bias current	I _{BIAS}	--	--	-0.1	-2	mA
Open-loop voltage gain	AVOL	2≤V _o ≤4V	60	90	--	dB
Unity Gain Bandwidth	BW	T _a =25°C	0.7	1	--	mHz
Power supply ripple rejection ratio	PSRR	12≤V _{CC} ≤25V	60	70	--	dB
Output Sink Current	I _{sink}	V _{pin 2} =2.7V, V _{pin 1} =1.1V	2	12	--	mA
Output Source Current	I _{source}	V _{pin 2} =2.3V, V _{pin 1} =5V	-0.5	-1	--	mA
V _{out} High	V _{OH}	V _{pin 2} =2.3V, R _L =15k to GND	5	6.2	--	V
V _{out} Low	V _{OL}	V _{pin 2} =2.7V, R _L =15k to V _{REF}	--	0.8	1.1	V
Current Sense section						
Gain	GV	(note 1, 2)	2.85	3	3.15	V/V
Maximum Input signal	V _{I(MAX)}	V _{pin 1} =5V(note 1)	0.9	1	1.1	V
Power supply ripple rejection ratio	PSRR	12≤V _{CC} ≤25V	--	70	--	dB
Input Bias Current	I _{BIAS}	--	--	-2	-10	μA
Delay to Output	T _{PLH}	V _{pin 3} =0 to 2V	--	150	300	ns
Output Section						
Output low Level	V _{OL}	I _{sink} =20mA	--	0.1	0.4	V
		I _{sink} =200mA	--	1.6	2.2	V
Output High Level	V _{OH}	I _{source} =20mA	13	13.5	--	V
		I _{source} =200mA	12	13.5	--	V
Rise Time	t _R	T _a =25°C, C _L =1nF	--	50	150	ns
Fall Time	t _F	T _a =25°C, C _L =1nF	--	50	150	ns
UVLO Saturation	V _{OL(UVLO)}	V _{CC} =5V, I _{sink} =1mA	--	0.7	1.2	V
Under-Voltage Lockout Output Section						
Start Threshold	V _{TH(ST)}	--	15	16	17	V
Min.Operating Voltage After Turn On	V _{OPR(min)}	--	9	10	11	V
PWM Section						
Min. duty cycle	D _(MIN)	--	--	--	0	%
Max. duty cycle	D _(MAX)	--	94	96	100	%
Total Standby Current						
Start-up Current	I _{ST}	--	--	0.3	0.5	mA
Operating Supply Current	I _{CC(opr)}	V _{pin 2} =V _{pin 3} =0V	--	12	17	mA
V _{cc} Zener Voltage	V _Z	I _{CC} =25mA	--	34	--	V

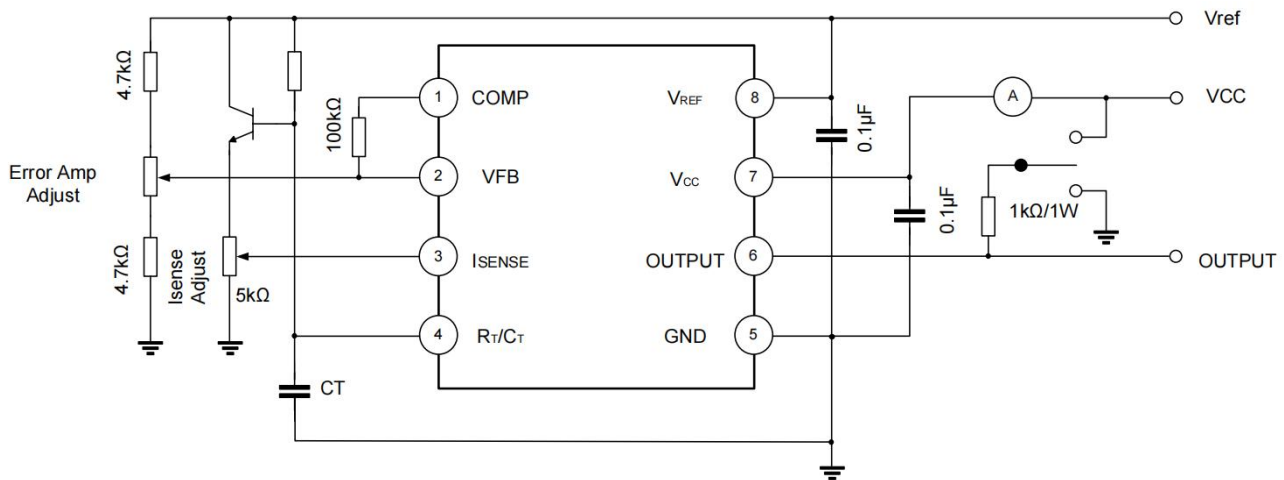
note1: Parameters measured at trip point of latch with V_{pin 2}=0.

2: Gain defined as:

$$A = \frac{\Delta V_{pin1}}{\Delta V_{pin3}}; \quad 0 \leq V_{pin3} \leq 0.8V$$

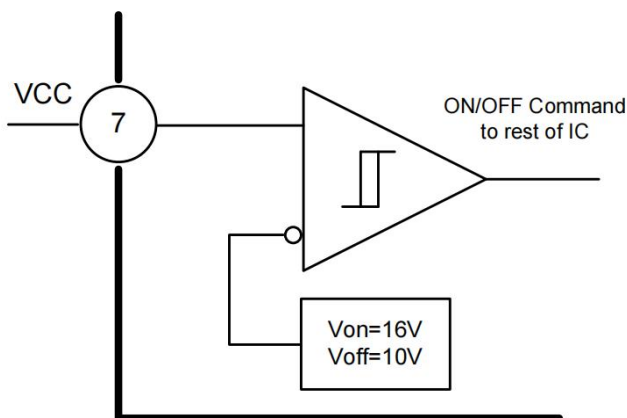
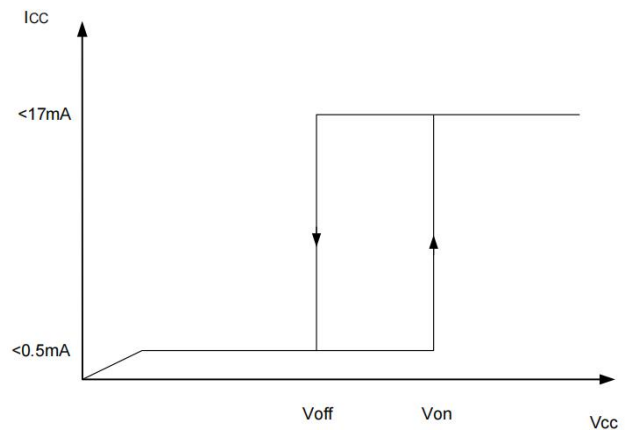
APPLICATION CIRCUIT

OPEN-LOOP LABORATORY TEST CIRCUIT



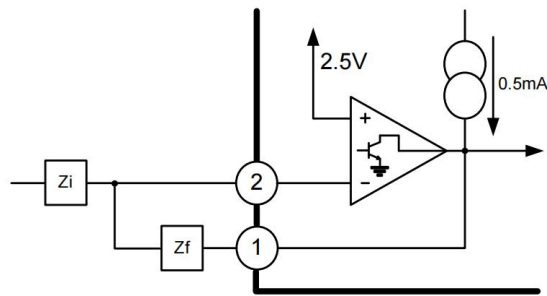
High peak current associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin5 in single point GND. The transistor and 5kΩ potentiometer are used to sample the oscillator waveform and apply an adjustable Ramp to Pin3.

UNDER-VOLTAGE LOCKOUT



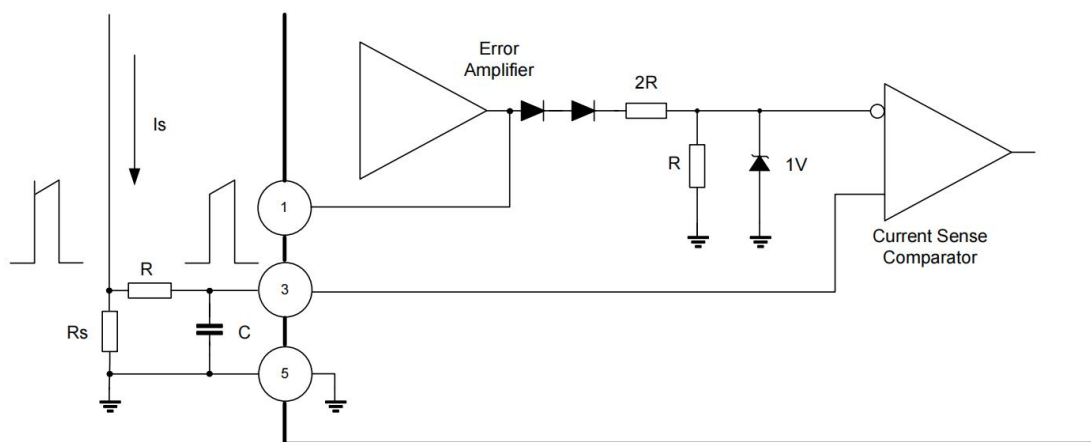
During Under-Voltage Lockout, the output driver is biased to a high impedance state. Pin 6 should be shunt to GND with a bleeder resistor to prevent activating the power switch with output leakage currents.

ERROR AMPLIFIER CONFIGURATION



Error amplifier can source or sink up to 0.5mA

CURRENT SENSE CIRCUIT

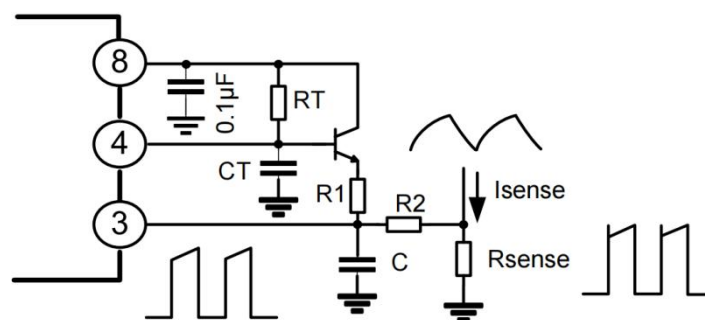


Peak current (I_s) determined by the formula:

$$I_{smax} = 1.0V/R_s.$$

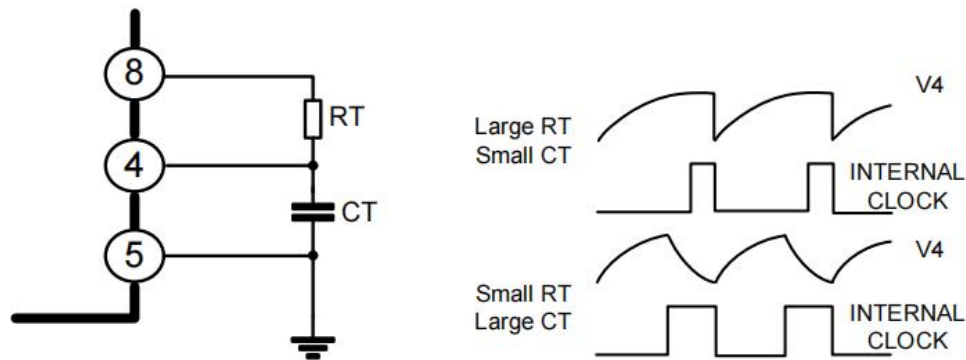
A small RC filter be required to suppress switch transients.

SLOPE COMPENSATION

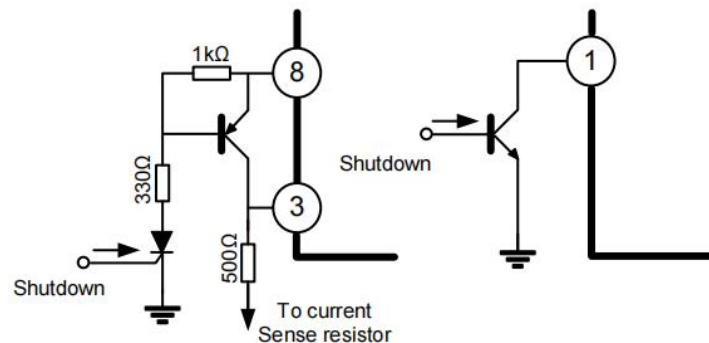


A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converts requiring duty cycles over 50%. Note that capacitor C, forms a filter with R2 to suppress the leading edge switch spikes.

OSCILLATOR SECTION



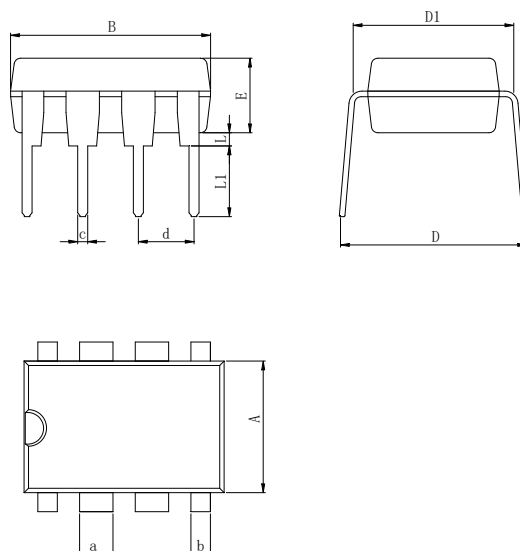
SHUTDOWN TECHNIQUES



Shutdown UC2842B can be accomplished by two methods; either raise pin 3 above 1V or pull Pin 1 below a voltage two diode drops above ground. Either method caused the output of PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which be reset by cycling V_{cc} below the lower UVLO threshold. At this point the reference turns off allowing the SCR to reset.

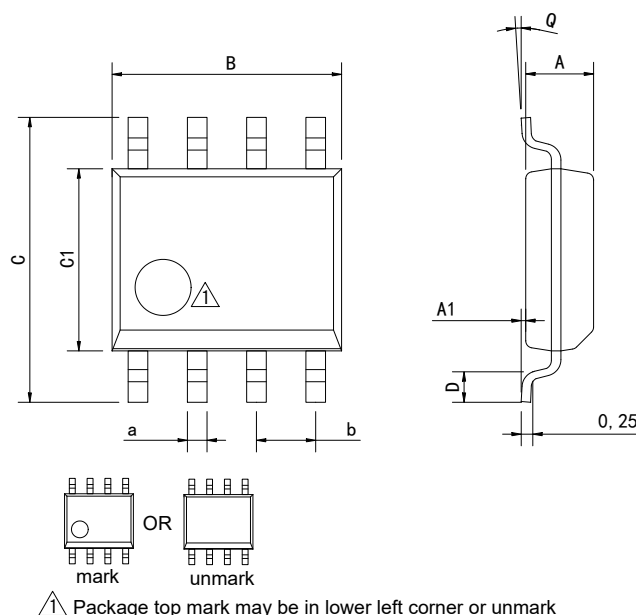
Physical Dimensions

DIP-8



Dimensions In Millimeters(DIP-8)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

SOP-8



Dimensions In Millimeters(SOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

Revision History

REVISION NUMBER	DATE	REVISION	PAGE
V1.0	2018-8	New	1-10
V1.1	2020-9	Remove the package MSOP、Update encapsulation type、	1、 3
V1.2	2024-11	Update Operating Temperature 、 Add a model marking name 、 Update Lead Temperature	3
V1.3	2025-12	Update important statements、 Update SOP-8 Dimension drawing	8、 10

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