

TK100E10NE

This material is for a technological examination material to aim at the product introduction. The change in the content of the characteristic might be accompanied at the final specification process. The latest specification will be able to be gotten in the brokerage department when the product of an equipment is designed and to get the confirmation.

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOSVIII-H)

TK100E10NE

Unit: mm

■ E-Bike/UPS/Inverter

Note : This product is designed for E-Bike / UPS / Inverter in China / India market.

- Low drain-source on-resistance : $R_{DS(ON)} = 4.3 \text{ m}\Omega$ (typ.)
- Low leakage current : $I_{DSS} = 10 \text{ }\mu\text{A}$ (max) ($V_{DS} = 100 \text{ V}$)
- Enhancement mode : $V_{th} = 2.0 \sim 4.0 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

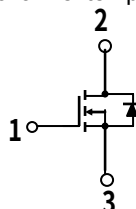
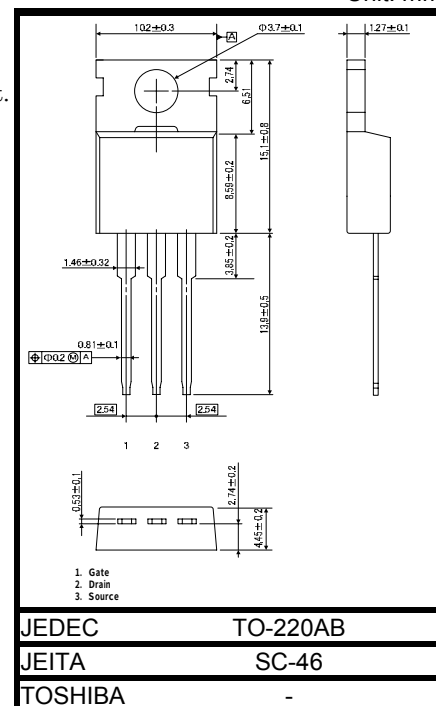
Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	100	V
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)		V_{DGR}	100	V
Gate-source voltage		V_{GSS}	± 20	V
Drain current	DC (Note 1)	I_D	100	A
	DC (Note 1,4)	I_D	90	A
	Pulse (Note 1)	I_{DP}	670	A
Drain power dissipation ($T_c = 25^\circ\text{C}$)		P_D	230	W
Single pulse avalanche energy (Note 2)		E_{AS}	65	mJ
Avalanche current		I_{AR}	50	A
Repetitive avalanche energy (Note 3)		E_{AR}	23	mJ
Peak diode recovery dv/dt (Note 5)		dv/dt	12	V/ns
Channel temperature (Note 4)		T_{ch}	175	$^\circ\text{C}$
Storage temperature range (Note 4)		T_{stg}	$-55 \sim 175$	$^\circ\text{C}$

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	0.65	$^\circ\text{C/W}$
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	83.3	$^\circ\text{C/W}$

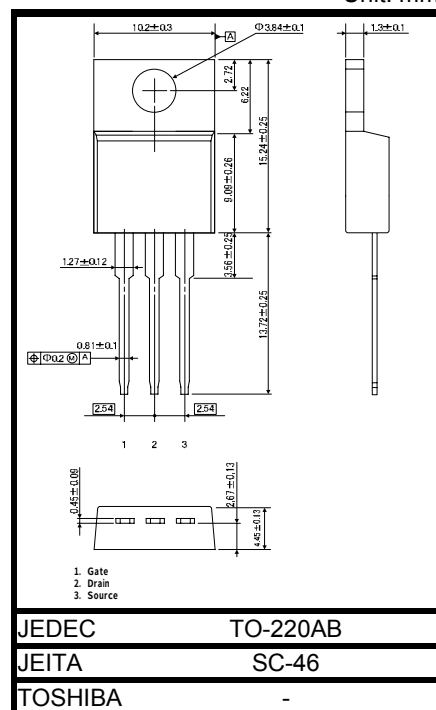
Note 1: Ensure that the channel temperature does not exceed 175°C .Note 2: $V_{DD} = 25 \text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 42 \text{ }\mu\text{H}$, $R_G = 25 \text{ }\Omega$, $I_{AR} = 50 \text{ A}$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

Note 4: $T_c = 100^\circ\text{C}$ Note 5: $I_{DR} \leq 80 \text{ A}$, $di/dt \leq 160 \text{ A}/\mu\text{s}$, $T_{ch} \leq T_{ch \text{ max.}}$,
 $V_{DS \text{ peak}} < V_{DSS}$ This transistor is an electrostatic-sensitive device.
Please handle with caution.

Weight: 1.9 g (typ.)

Unit: mm

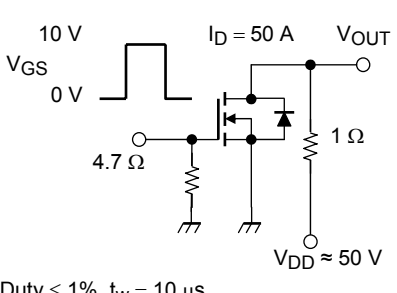


Weight: 1.9 g (typ.)

Note : Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.). Thermal Characteristics

Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 0.1	μA
Drain cut-off current		I_{DSS}	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	10	μA
Drain-source breakdown voltage	$V_{(BR)DSS}$		$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	100	—	—	V
	$V_{(BR)DSX}$		$I_D = 10 \text{ mA}, V_{GS} = -20 \text{ V (Note 5)}$	65	—	—	V
Gate threshold voltage		V_{th}	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$	2.0	—	4.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = 10 \text{ V}, I_D = 50 \text{ A}$	—	4.3	5.1	$\text{m}\Omega$
Input capacitance		C_{iss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	5590	—	pF
Reverse transfer capacitance		C_{rss}		—	350	—	
Output capacitance		C_{oss}		—	2680	—	
Switching time	Rise time	t_r		—	18	—	ns
	Turn-on time	t_{on}		—	44	—	
	Fall time	t_f		—	27	—	
	Turn-off time	t_{off}		—	86	—	
Total gate charge (Gate-source plus gate-drain)		Q_g	$V_{DD} \approx 80 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 100 \text{ A}$	—	83	—	nC
Gate-source charge		Q_{gs}		—	63	—	
Gate-drain ("miller") charge		Q_{gd}		—	20	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

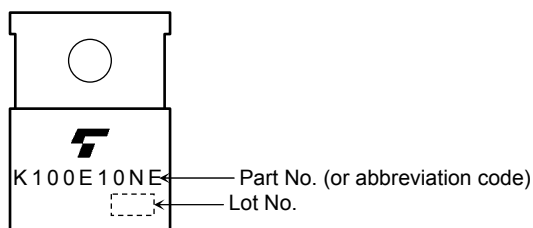
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	100	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	670	A
Forward voltage (diode)	V_{DSF}	$I_{DR} = 100 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	-1.5	V
Reverse recovery time (Note 6)	t_{rr}	$I_{DR} = 100 \text{ A}, V_{GS} = 0 \text{ V}$	—	88	—	ns
Reverse recovery charge (Note 6)	Q_{rr}	$dI_{DR}/dt = 50 \text{ A}/\mu\text{s}$	—	93	—	nC

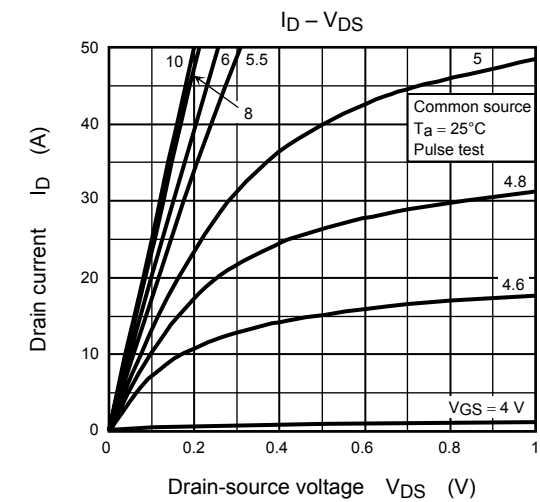
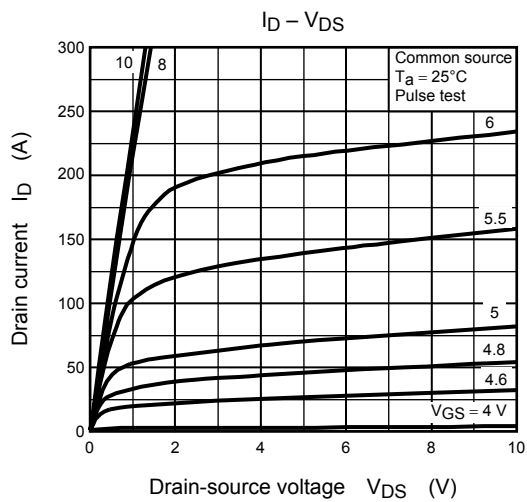
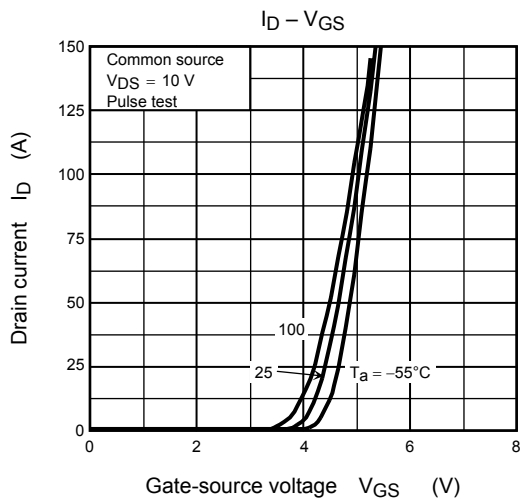
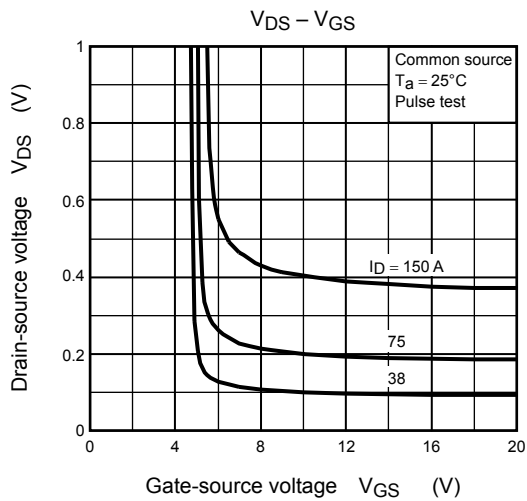
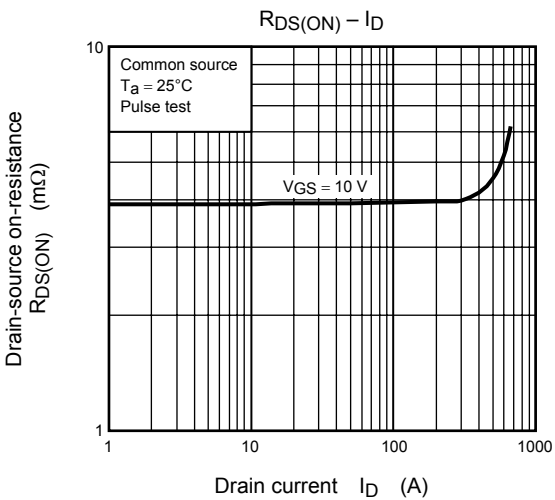
Note 5: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode.

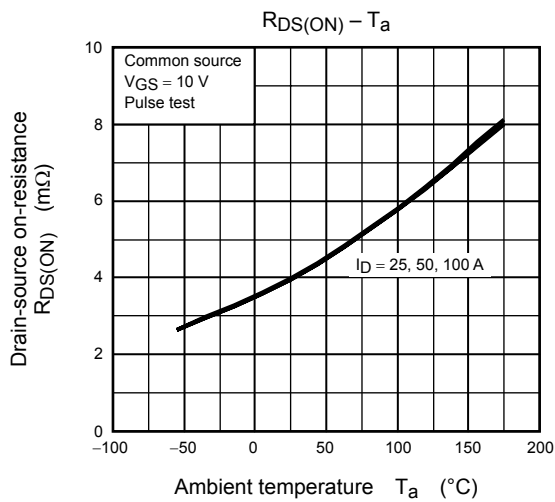
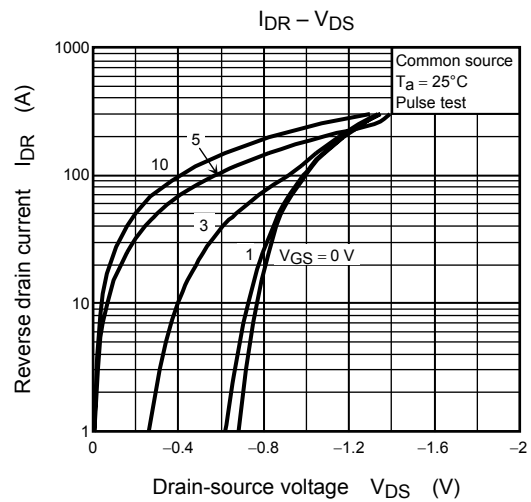
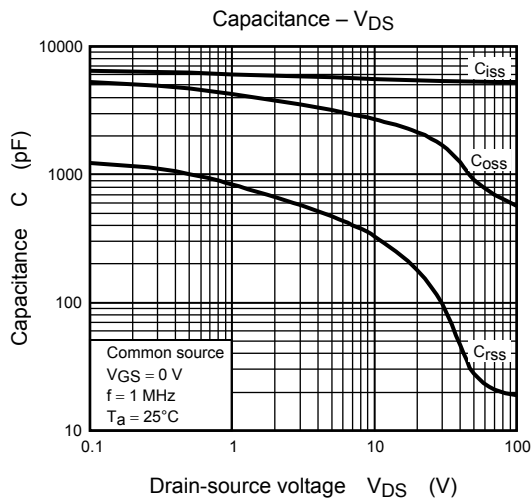
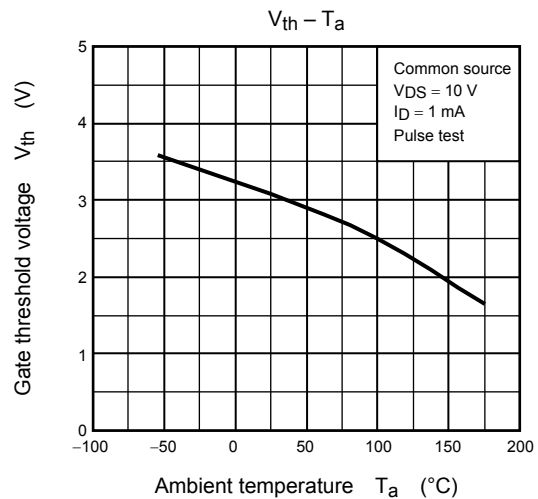
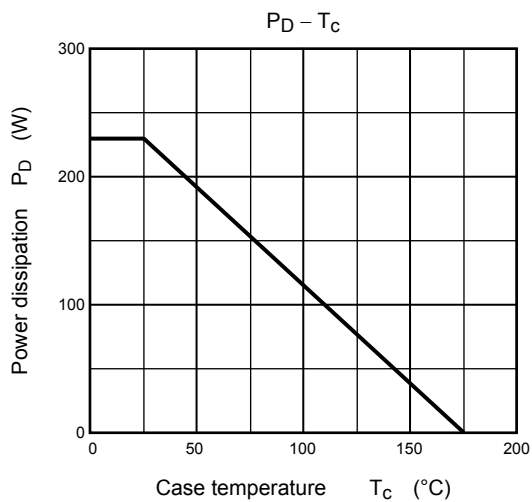
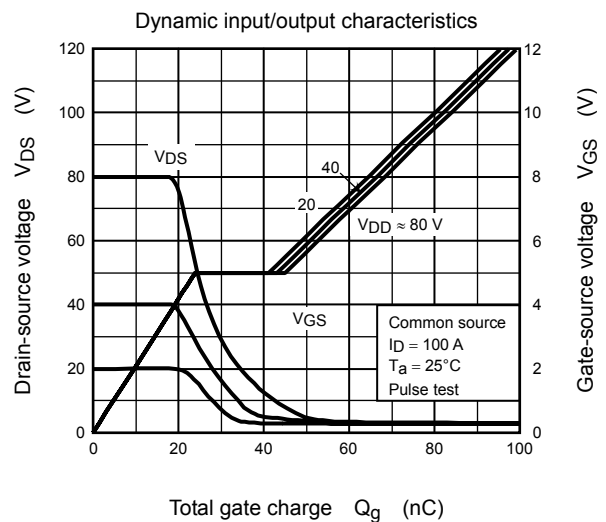
Note that the drain-source breakdown voltage is lowered in this mode.

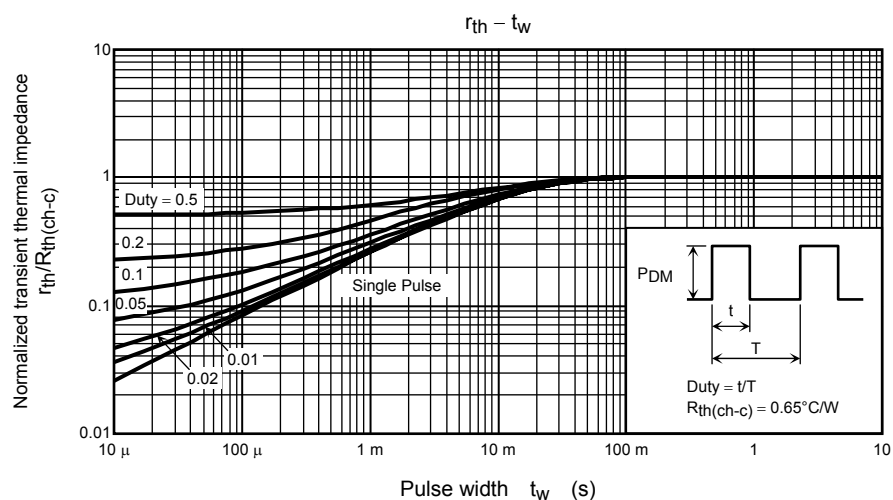
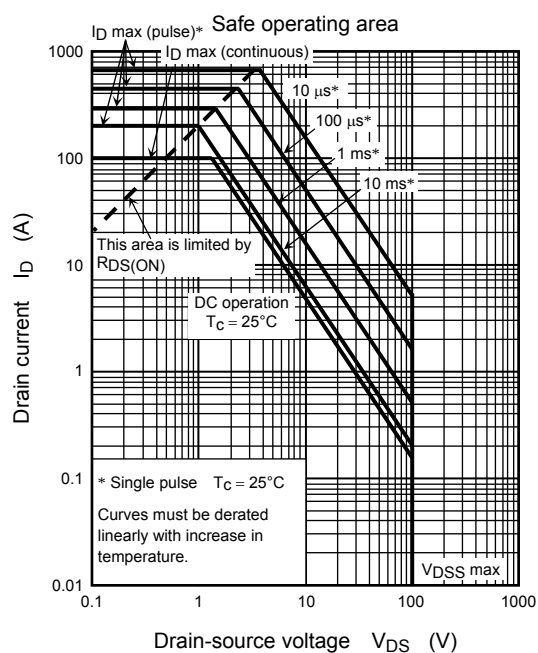
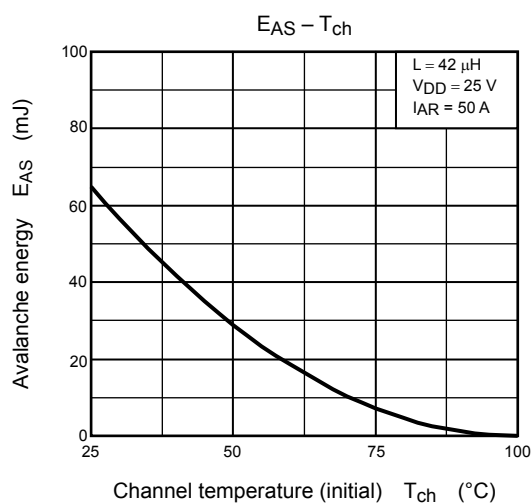
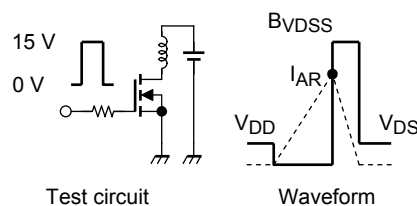
Note 6: Ensure that V_{DS} peak does not exceed V_{DSS} .

Marking









$$R_G = 25 \, \Omega$$

$$V_{DD} = 25 \, \text{V}, L = 42 \, \mu\text{H}$$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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