Features

General

- 2-output programmable clock generator
- High jitter performance
- Working temperature: -40°C ~ 85°C
- Power supply: 1.8V to 3.3V
- Low power consumption
  - <100mW (1.8V with 100MHz LP-HCSL outputs)
- Input reference source option
  - SYKG1021E: external crystal or clock input
  - SYKG1021Q5: internal crystal

Input Reference Clock

- Single input source
  - Crystal input source
    - Internal crystal: 50MHz
    - External crystal: 8MHz ~ 50MHz
  - Clock input source
    - Frequency range: 1.22MHz ~ 250MHz
    - Acceptable input duty cycle: 40 ~ 60%

Output Clock

- 2 differential-pair outputs
- Output frequency range: 1MHz ~ 333.33MHz
- SYNK-developed LP-HCSL for high jitter performance and low power
- Support LVPECL and CML logic with easy AC coupling
- 1 LVCMOS reference clock outputs
- Support all three PCIe clocking architectures
  - Common Clocked (CC)
  - Independent Reference without spread spectrum (SRnS)
  - Independent Reference with spread spectrum (SRIS)
- Optional individual SSC setting for all output clocks; feedback fractional divider used by SSC for better jitter performance
- Programmable output impedance: 85Ω/100Ω or off Control

Control

- Three control modes selectable at power-on stage: I2C mode, OTP mode, PIN mode
- Output clock dynamical control by multi-function pins
- Support up to 4 On-chip OTP configurations
- Four programmable I2C addresses: D0, D2, D4, D6

Package

- 3.0mm x 3.0mm x 1.1mm, 0.5mm pitch, 16-pin LGA
- Package MSL: Level-2-260C

Key Specifications

- 250fs RMS 12kHz ~ 20MHz typical phase jitter at 100MHz
- 230fs RMS 12kHz ~ 20MHz typical phase jitter at 156.25MHz
- FFB PCIe Gen5 jitter (CC) typical 30fs RMS
- FOD PCIe Gen5 jitter (CC) typical 98fs RMS
- FFB PCIe Gen6 jitter (CC) typical 20fs RMS
- FOD PCIe Gen6 jitter (CC) typical 66fs RMS

Applications

- High-performance Computing (HPC)
- Storage, like SSD
- Ethernet
- Fiber Optic Modules
- NVLink

General Description

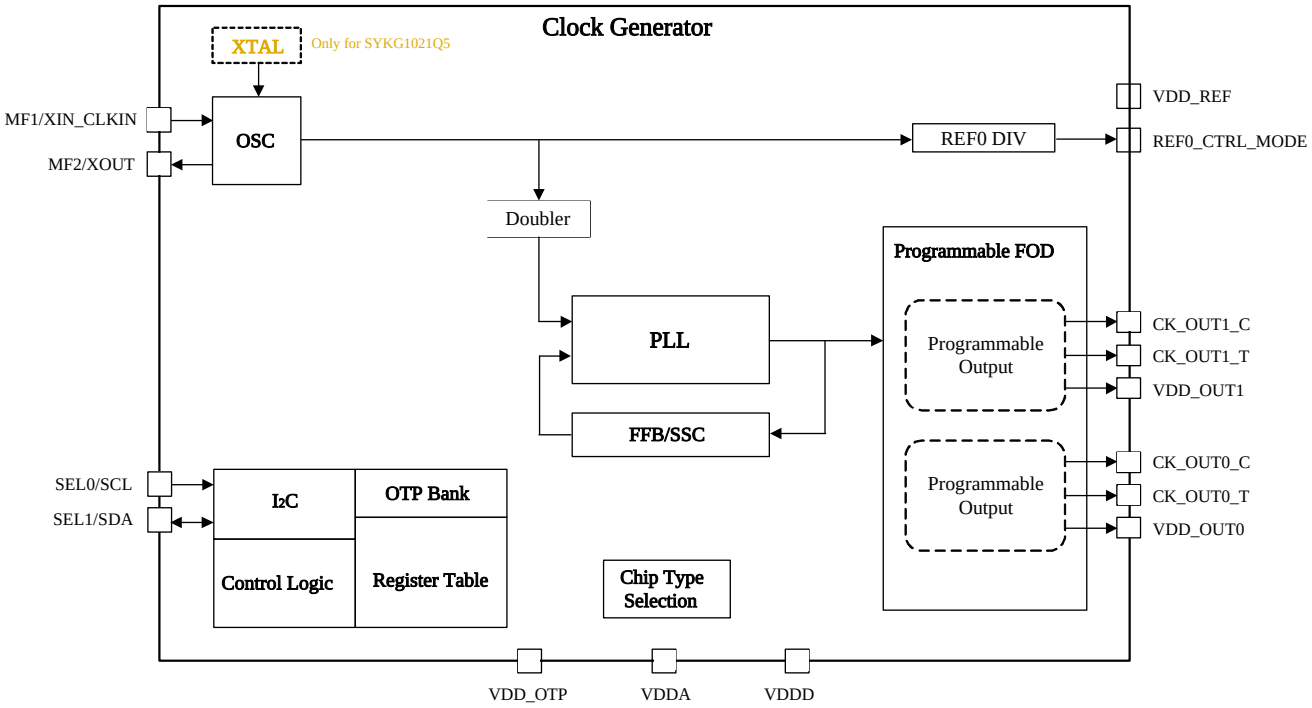
SYKG1021E/Q5 is a Clock Generator with one input reference clock, two programmable output pairs plus one LVCMOS reference outputs.

The chip utilizes SYNK's advanced IO technology to generate a wide range of frequencies with excellent jitter performance for low phase noise spread-spectrum applications such as PCIe. It can source multiple 100MHz PCIe clock outputs. All differential clock outputs are compliant to PCIe Gen1/2/3/4/5/6 common clock and separate reference clock architecture specifications.

This chip supports the initialization through on-chip One-Time Programmable (OTP) configurations. These chip configuration can be partly or fully modified in working state according to the current control mode decided by a strapping pin at power-up stage, which easily realizes software selection of the desired configuration. Four programmable I2C addresses are available, allowing easy I2C access to multiple components.

Functional Block Diagram

Figure 1. SYKG1021E/Q5 Block Diagram



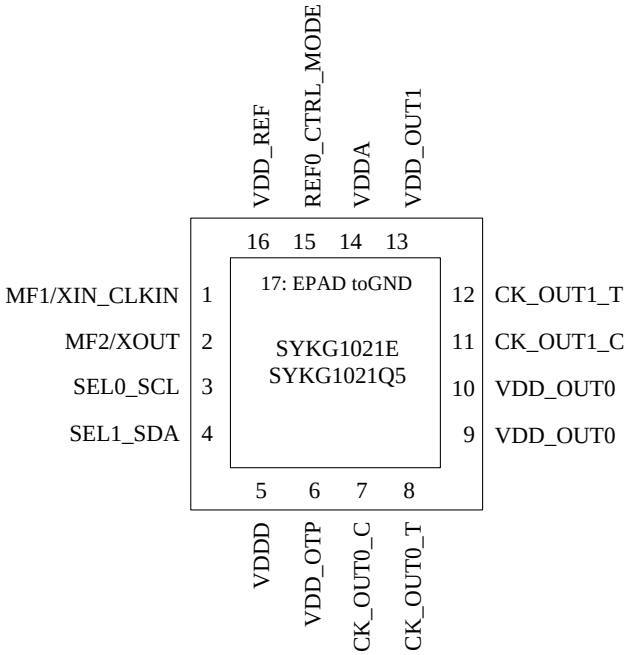
Notes:

1. FFB: Fraction Feedback Divider
   FOD: Fraction Output Divider
   IN DIV: Input Divider
   OTP: One-Time Programmable
   PLL: Phase Locked Loop
   SSC: Spread Spectrum Clocking
   XTAL: Crystal

1 Pin Information

1.1 Pin Assignment

Figure 2. 16-LGA Pin Assignment, 3.0mm x 3.0mm x 1.1mm, 0.5mm Pitch (Top view)



1.2 Pin Description

Table 1. Pin Description (16-LGA) (Sheet 1 of 2)

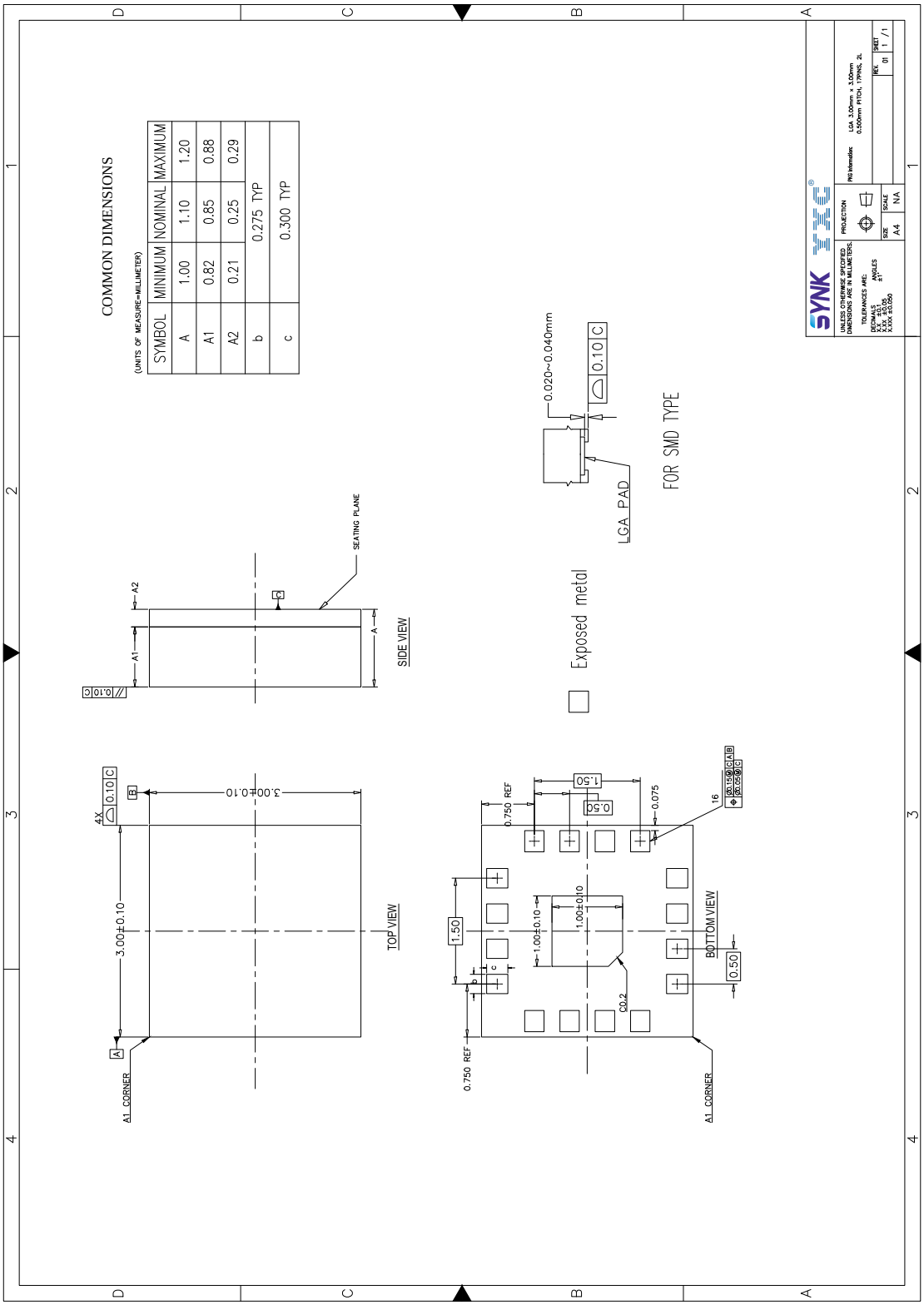
Pin NO.	Pin Name	Type	Description
1	MF1/XIN_CLKIN	Input	Crystal input or reference clock input or multi-function pin.
2	MF2/XOUT	Input/Output	Crystal output or multi-function pin.
3	SEL0_SCL	Input	Tri-state logic clock pin with 120kΩ internal pull-up and pull-down. Be used as LSB of control mode selection or I2C SCL.
4	SEL1_SDA	Input/Output	Tri-state logic datapin with 120kΩ internal pull-up and pull-down.Be used as MSB of control mode selection or I2C SDA.
5	VDDD	Power	Digitalpower.Connectto1.8V,2.5V,3.3V.
6	VDD_OTP	Power	Voltage for OTP programming, 1.8V±10%. For Read operation, this pin can be connected to VDDD if VDDD is lower than 2.5V. This pin must be tied to ground or floating if the VDDD is greater than 2.5V. It is recommended to connect VDD_OTP to ground or leave VDD_OTP floating, no matter what level VDDD is.
7	CK_OUT0_C	Output	Complementary Output Clock0.

Table 1. Pin Description (16-LGA) (Sheet 2 of 2)

PinNO.	PinName	Type	Description
8	CK_OUT0_T	Output	Output Clock0.
9	VDD_OUT0	Power	Power supply for Output Clock0.
10	VDD_OUT0	Power	Power supply for Output Clock0.
11	CK_OUT1_C	Output	Complementary Output Clock1.
12	CK_OUT1_T	Output	Output Clock1.
13	VDD_OUT1	Power	Power supply for Output Clock1.
14	VDDA	Power	Analog power.Connect to same voltage as V_{DDD} with suitable filtering.
15	REF0_CTRL_MODE	StrappingPin	Chip configuration model selection and LVCMOS clock output. Tri-state logic in put pin. At power-up, the state of this pin is latched to select the functionality of several hardware pins. After power-up, this pin acts as one LVCMOS reference output with the output frequency same as input reference or scale down to 1/64 at most.
16	VDD_REF	Power	Power supply for REF output and the internal XOUT. Nominal voltages are 1.8V, 2.5V and 3.3V.
17	EPAD	GND	Connect to ground.

2 Mechanical Package Data

Figure 3. 16-LGA Package Outline (3.0mm x 3.0mm x 1.1mm, 0.5mm Pitch)



3 Ordering Information

Part Number	Package	Temperature	Crystal	Packing
SYKG1021E-XX-T	3mm x 3mm x 1.1mm, 0.5mm pitch 16-LGA; MSL Level-2-260C	-40~+85°C	External	Tape & Reel