Features

- 3 input reference clocks
  - Two differential clock pair up to 3.1GHz, accepting single-ended clock source up to 350MHz
  - One crystal input, accepting 8MHz to 50MHz crystal or single-ended clock source
- 4 output clocks:
  - Two power banks with 2 differential outputs each, supporting LVPECL, LVDS and LP-HCSL
  - One independent LVCMOS output clock
- Frequency range:
  - LVCMOS: DC to 350MHz
  - LVDS: DC to 3.1GHz
  - LVPECL: DC to 3.1GHz
  - LP-HCSL: DC to 1GHz
- Excellent PSRR :
  - LVDS: -74dBC @156.25Mhz
  - LVPECL: -67dBC @156.25Mhz
  - LPHCSL: -76dBC @156.25Mhz
- Ultra-low latency and skew
- Additive Jitter:
  - 34 fs RMS (12kHz to 20MHz) typical @LP-HCSL 156.25MHz
  - 10 fs RMS typical @ PCIe Gen5 jitter (CC)
- Three independently configurable 1.8V-3.3Vpower supplies for:
  - Core
  - Differential outputs
  - Single-ended outputs
- Pin-based control for flexible input reference selection and output enable/disable
- Glitch-free switchover supported in the "G" version
- Working temperature: -40°C to +85°C
- Package: 32-pin WQFN

1.SYKB*****: No glitch-free switchover.
2.SYKB*****G: Includes glitch-free switchover.
3.F: Supports LVPECL, LVDS, and LP-HCSL differential clock outputs.
4.Unless otherwise stated, the terms "clock buffer" and "buffer" refer to the entire series.

General Description

SYKB23F04(G)[1,2,3,4] is a type of high-performance clock fanout buffer operating at up to 3.1GHz with 4 outputs. The buffer is designed for low-jitter, high-frequency clock/data distribution and level translation.

The buffer supports clock input selection from either two differential clock pairs or one crystal input, distributing the selected clock to two output banks, each with 2 differential outputs, along with a dedicated LVCMOS output. Both differential output banks can be configured as LPPECL,LVDS,LP-HCSL or disabled

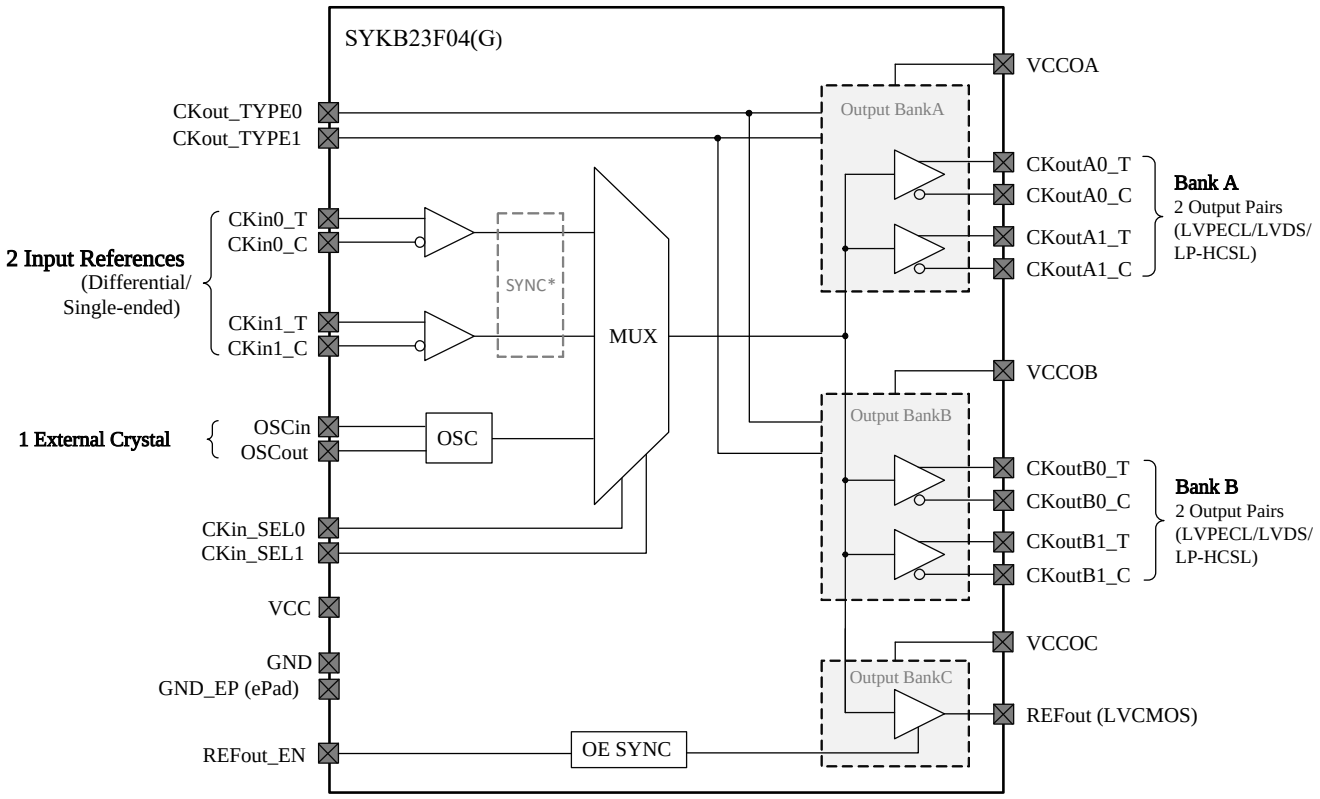
Operating with a core supply of 1.8V-3.3V and three independent output supplies of 1.8V-3.3V, the clock buffer provides flexible control via logic pins for input reference clock selection and output enable/disable functions.

The buffer can be paired with SYNK Technology’ s SYKG010xx clock generator to deliver a robust clock tree solution. With broad input and output frequency ranges, optimized power management, and reduced propagation delay, the buffer operates across a wide temperature range, making it an ideal choice for demanding applications.

Applications

- PCIe® 1.0 to 6.0 and NVLink
- Clock distribution and level translation for ADCs, DACs, SATA/SAS, SONET/SDH, multi-gigabit Ethernet, and Fibre Channel line cards
- Servers, storage systems, switches, routers, and display panels
- Reference clock distribution for BBU and RRU applications

Functional Block Diagram



Note: Only the "G" (includes glitch-free switchover) version supports the synchronization function.

Ordering Information

Part Number	Package	Operating Temperature
SYKB23F04	32-pin WQFN, 5.0mm x 5.0mm x 0.75mm	-40°C to +85°C