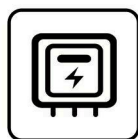


TDSEMIC

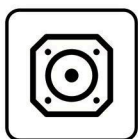
拓電半導體

自主封測 品質把控 售後保障

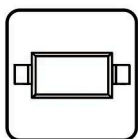
WEB | WWW.TDSEMIC.COM



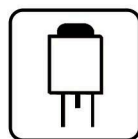
電源管理



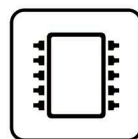
顯示驅動



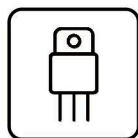
二三極管



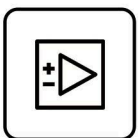
LDO穩壓器



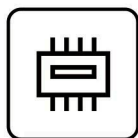
觸摸芯片



MOS管



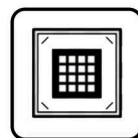
運算放大器



存儲芯片



MCU



串口通信

TD110N100

產品規格說明書

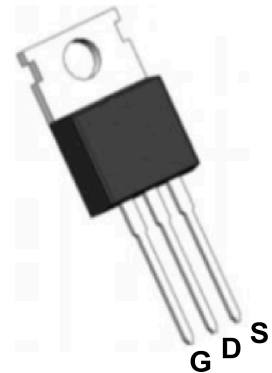
100V N-Channel Enhancement Mode Power MOSFET TD110N100 · TO-220

Features

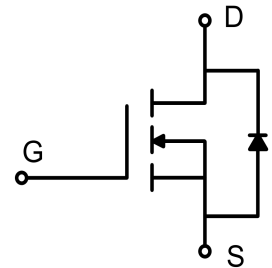
- $V_{DS} = 100V$, $I_D = 120A$
- $R_{DS(on)} < 5\text{ m}\Omega$ @ $V_{GS} = 10V$
- Green Device Available
- Low Gate Charge
- 100% EAS Guaranteed

Applications

- Power Management Switches
- DC/DC Converter
- Industrial and Motor Drive Applications



TO-220



Absolute Maximum Ratings

Parameter	Conditions	Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ¹	$T_C = 25^\circ\text{C}$	I_D	120	A
	$T_C = 100^\circ\text{C}$		73.4	
Pulsed Drain Current ²		I_{DM}	464	A
Single Pulse Avalanche Energy ³		E_{AS}	205	mJ
Total Power Dissipation ⁴	$T_C = 25^\circ\text{C}$	P_D	162	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient ¹	$R_{\theta JA}$	58	$^\circ\text{C/W}$
Thermal Resistance from Junction-to-Case ¹	$R_{\theta JC}$	0.77	$^\circ\text{C/W}$

Electrical Characteristics $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100	—	—	V
Gate-body Leakage current	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V	—	—	±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	T _J = 25℃, V _{DS} = 100V, V _{GS} = 0V	—	—	1	μA
		T _J = 100℃, V _{DS} = 100V, V _{GS} = 0V	—	—	100	
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2.2	2.9	3.6	V
Drain-Source on-Resistance ²	R _{DS(on)}	V _{GS} = 10V, I _D = 20A	—	4.6	6	mΩ
		V _{GS} = 8.0V, I _D = 15A	—	4.9	6.5	
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} = 50V, V _{GS} = 0V, f = 1MHz	—	4400	—	pF
Output Capacitance	C _{oss}		—	645	—	
Reverse Transfer Capacitance	C _{rss}		—	20	—	
Switching Characteristics						
Gate Resistance	R _g	V _{GS} = 0V, V _{DS} = 0V, f = 1MHz	—	1.6	—	Ω
Total Gate Charge	Q _g	V _{GS} = 10V, V _{DS} = 50V, I _D = 20A	—	75	—	nC
Gate-Source Charge	Q _{gs}		—	17	—	
Gate-Drain Charge	Q _{gd}		—	13	—	
Turn-on Delay Time	t _{d(on)}	V _{GS} = 10V, V _{DS} = 50V, R _G = 3Ω, I _D = 20A	—	15.4	—	ns
Rise Time	t _r		—	13	—	
Turn-off Delay Time	t _{d(off)}		—	34	—	
Fall Time	t _f		—	6.2	—	
Drain-Source Body Diode Characteristics						
Diode Forward Voltage ²	V _{SD}	I _F = 20A, V _{GS} = 0V	—	—	1.2	V
Continuous Source Current ^{1,5}	I _S	V _G = V _D = 0V, Force Current	—	—	120	A
Body Diode Reverse Recovery Time	t _{rr}	I _F = 20A, dI/dt = 100A/μs	—	55	—	ns
Body Diode Reverse Recovery Charge	Q _{rr}		—	101	—	nC

Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating. The test condition is $V_{DD} = 50V, V_{GS} = 10V, L = 0.4mH, I_{AS} = 32A$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

Typical Characteristics

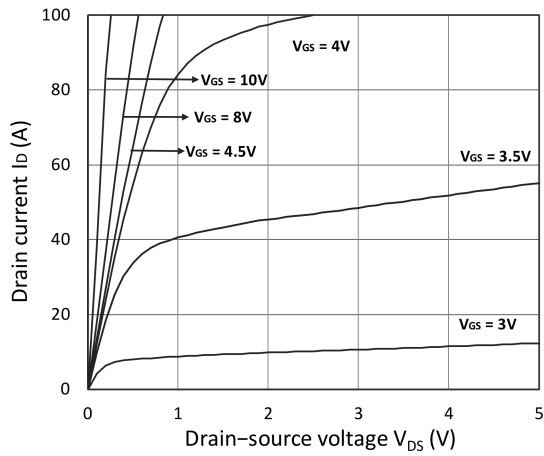


Figure 1. Output Characteristics

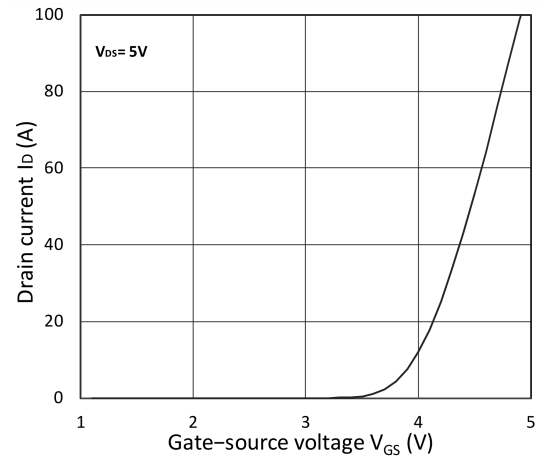


Figure 2. Transfer Characteristics

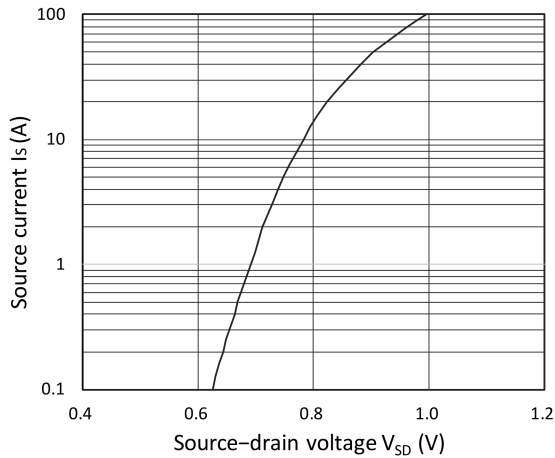


Figure 3. Forward Characteristics of Reverse

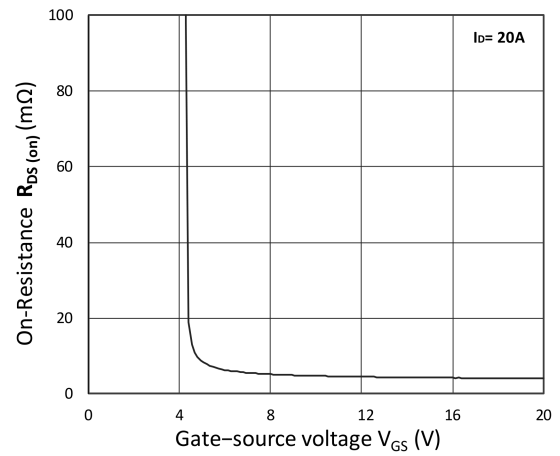


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

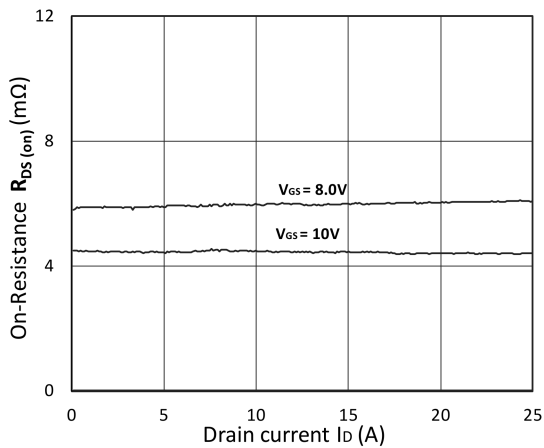


Figure 5. $R_{DS(ON)}$ vs. I_D

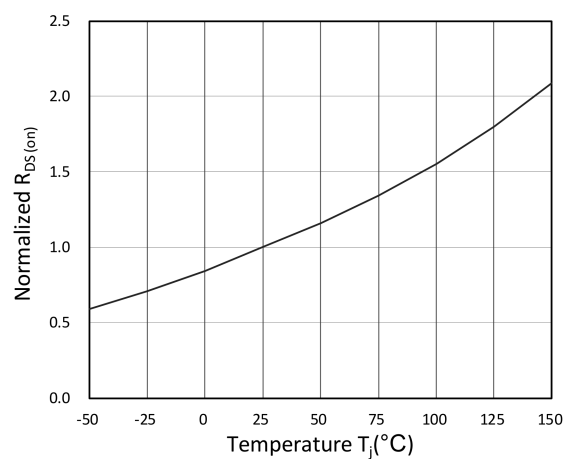


Figure 6. Normalized $R_{DS(ON)}$ vs. Temperature

Typical Characteristics (continued)

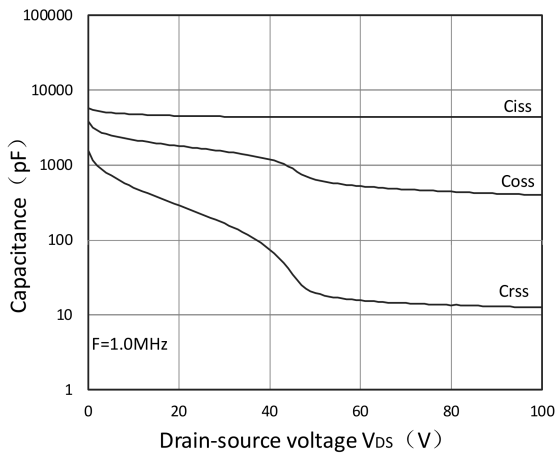


Figure 7. Capacitance Characteristics

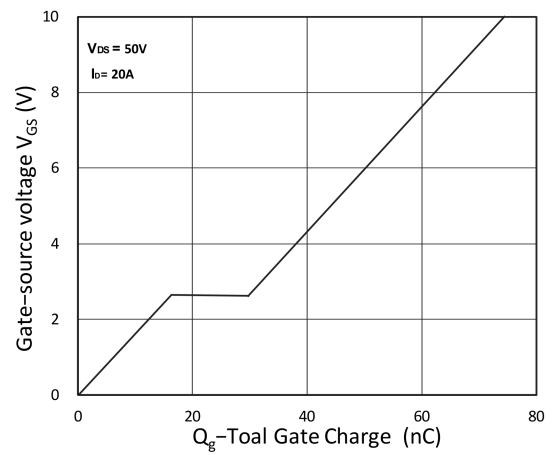


Figure 8. Gate Charge Characteristics

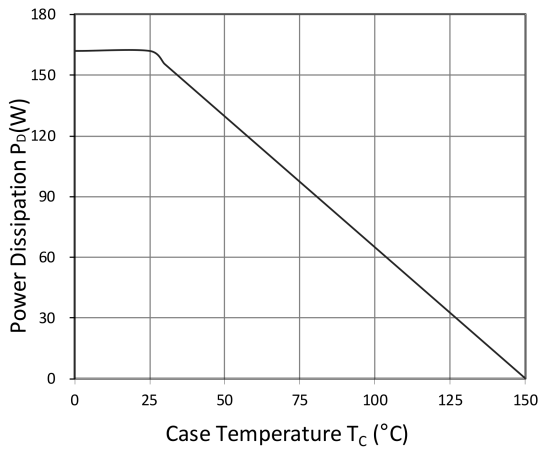


Figure 9. Power Dissipation

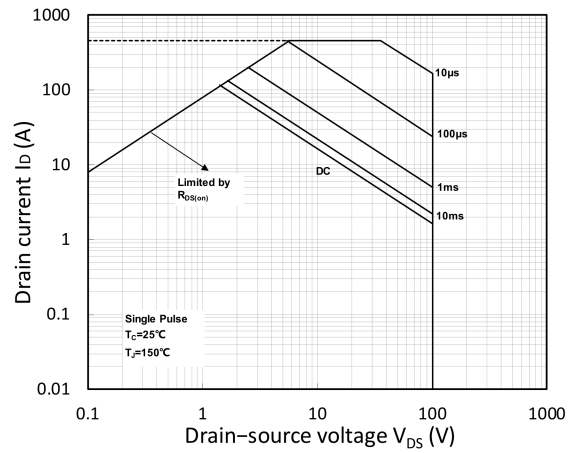


Figure 10. Safe Operating Area

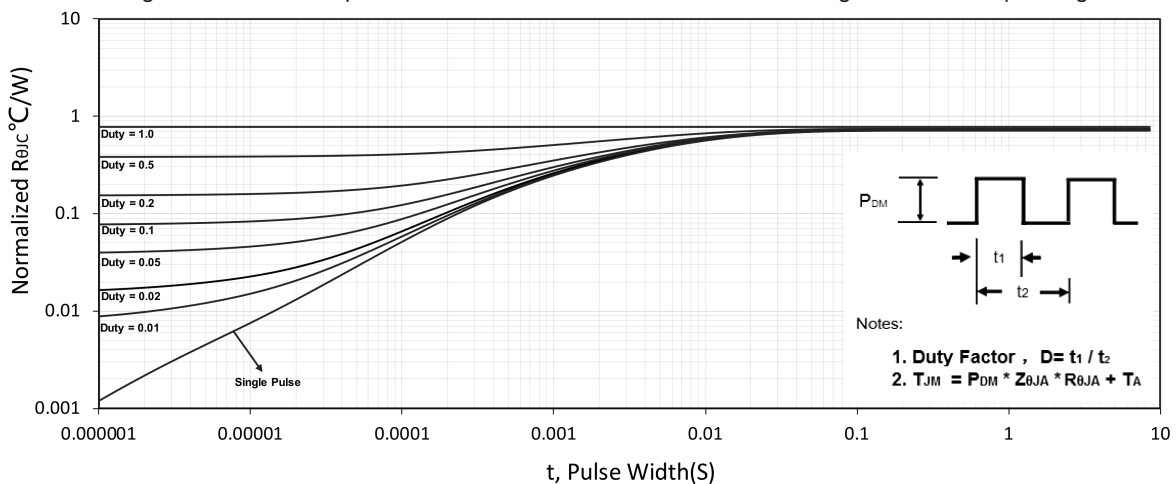


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

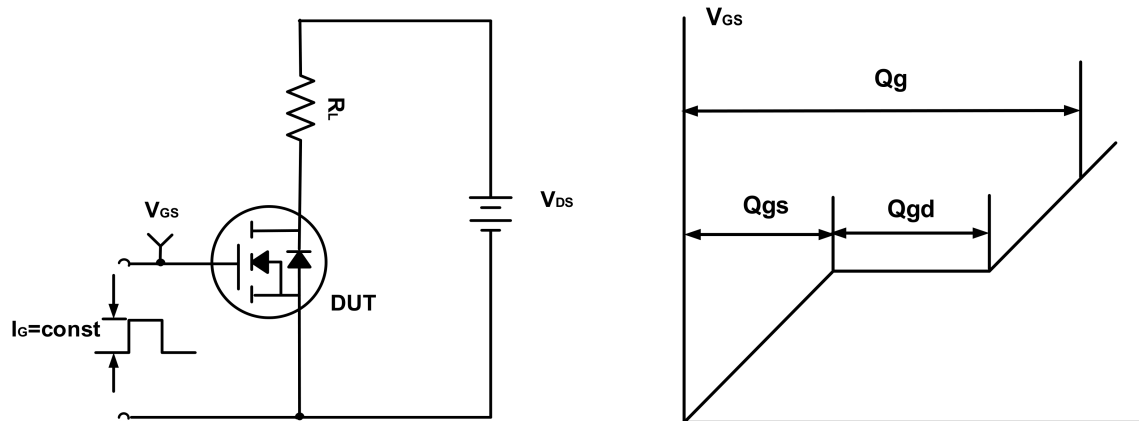


Figure A. Gate Charge Test Circuit & Waveforms

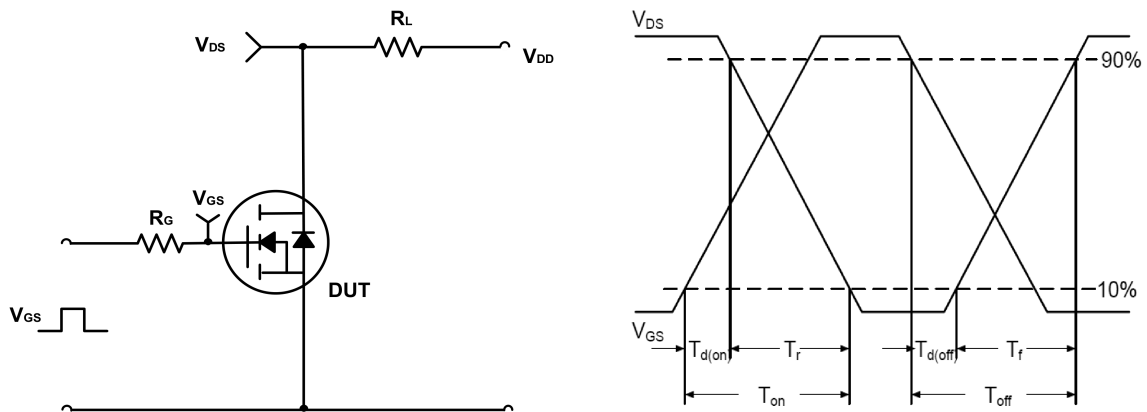


Figure B. Switching Test Circuit & Waveforms

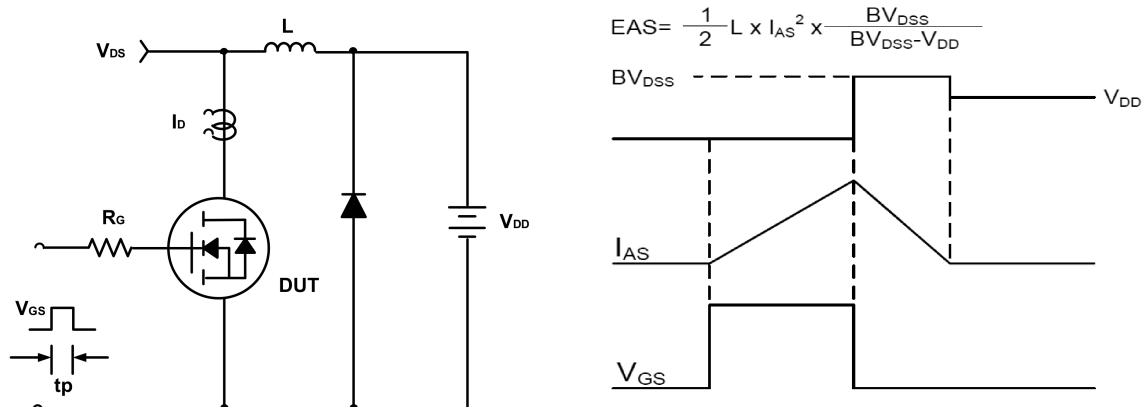
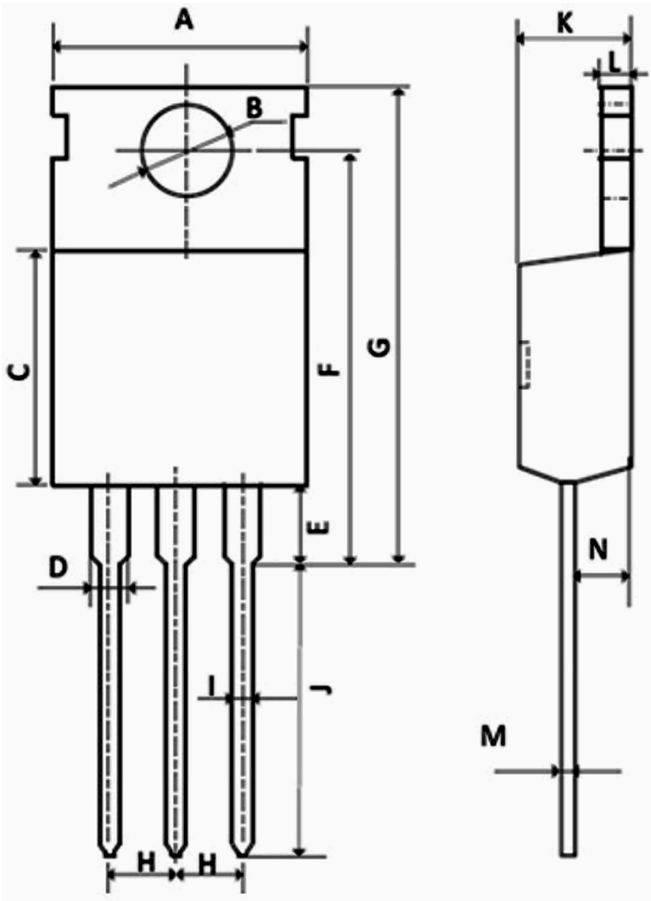


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Package Outline TO-220

Mechanical Dimensions for TO-220



COMMON DIMENSIONS

SYMBOL	MM		SYMBOL	MM	
	MIN	MAX		MIN	MAX
A	9.70	10.30	H	2.54REF	
B	3.40	3.80	I	0.70	0.95
C	8.80	9.40	J	9.35	11.00
D	1.17	1.47	K	4.30	4.77
E	2.60	3.50	L	1.20	1.45
F	15.10	16.70	M	0.40	0.65
G	19.55MAX		N	2.20	2.60