Features

General

- 4-output programmable clock generator
- High jitter performance, low-phase-noise PLL
- Working temperature: -40°C ~ 85°C
- Power supply: 1.8V to 3.3V

Input Reference Clock

- Redundant input sources with manual switching
  - Crystal input source
    - External crystal: 8MHz ~ 40MHz
  - Clock input source
    - CLKIN/CLKINB: 1MHz ~ 350MHz, AC-coupled
    - XIN/REF single-ended: 1MHz ~ 200MHz
- Glitch-free switching between the two inputs

Output Clock

- 4 general-purpose output pairs, independently configurable
  - Differential: LVPECL, LVDS or HCSL
  - Single-ended: 2 × LVCMOS
- 4 output frequency range
  - LVCMOS: 1kHz ~ 250MHz
  - Differential: 1kHz ~ 300MHz (integer and fractional divider)
  - Differential: 300 ~ 800MHz (integer divider only)
- 1 LVCMOS reference clock outputs
- Individual programmable SSC per divider, 30kHz ~ 63kHz triangular modulation
- Programmable output phase offset 0 ~ 360°, 1/128 VCO period step
- I/O supply (VDDOx) per output pair:
  - LVDS and LVCMOS: 1.8V, 2.5V or 3.3V
  - HCSL and LVPECL: 2.5V or 3.3V
- Programmable LVCMOS output slew rate,4 levels

Control

- SD/OE pin programmable as output enable or power-down
- Support up to 4 On-chip OTP configurations
- I2C addresses: 0xD0 or 0xD4

Package

- 4.0mm x 4.0mm x 0.9mm, 0.5mm pitch, 24-pin VFQFPN

Key Specifications

- <0.4ps RMS typical phase jitter at the output
- 0.2ps RMS 12kHz ~ 20MHz typical phase jitter ,differential output
- PCIe Gen5 jitter (CC, SSC off) typical 0.02ps RMS
- PCIe Gen6 jitter (CC, SSC off) typical 0.015ps RMS
- PCIe Gen3/4 jitter (CC, SSC -0.5%) typical 0.45ps RMS
- Jcy-cy: 5ps on LVCMOS, 25ps differential (typ)

Applications

- Ethernet switches/routers, MSAN/DSLAM/PON
- SSC disabled: PCIe 1.0/2.0/3.0/4.0/5.0/6.0
- SSC enabled: PCIe 1.0/2.0/3.0/4.0
- Broadcast video/audio clocks
- Multifunction printers
- Processor and FPGA clocks
- Fibre Channel, Storage Area Network

General Description

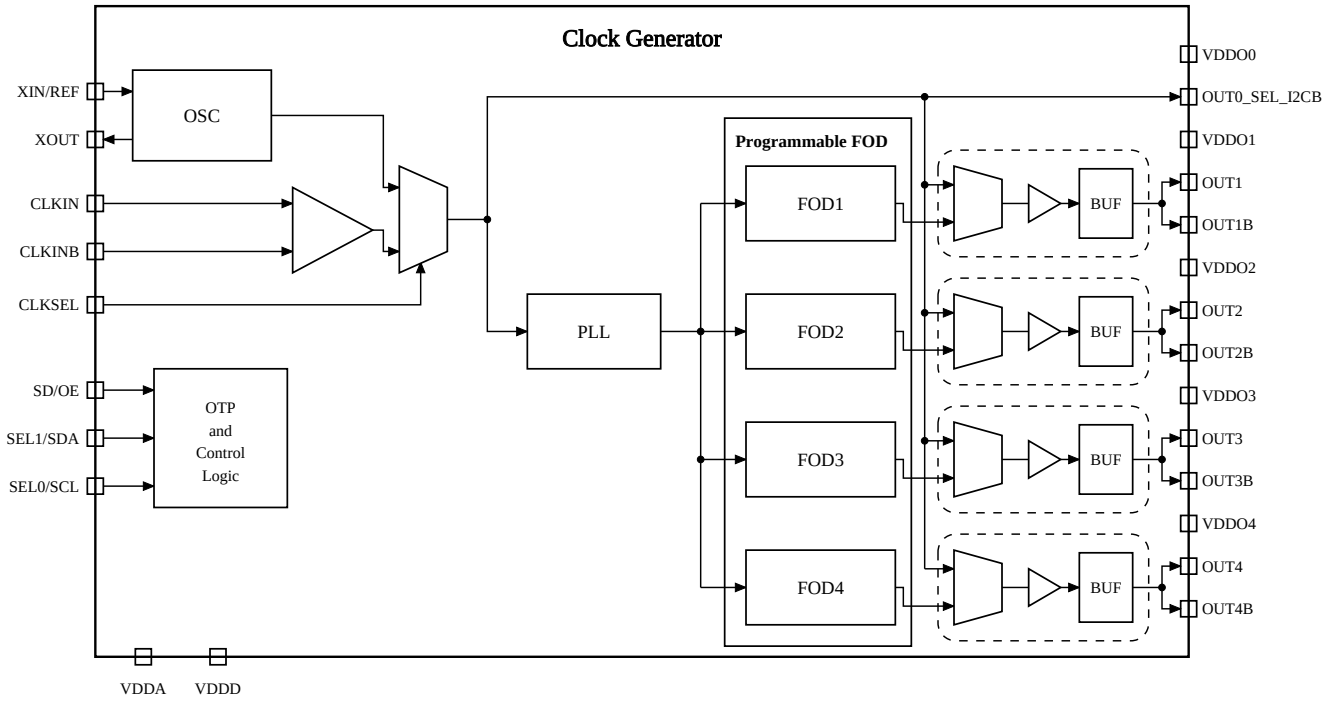
The SYKG6965 is a programmable clock generator suitable for high-performance consumer electronics, networking, industrial, computing and data communications applications. Configuration information can be stored in on-chip one-time programmable (OTP) memory or modified through the I2C interface. All output frequencies are generated from a single reference clock.

The reference clock can be derived from either of two redundant inputs, and a glitch-free manual switching function allows selection of one of them during normal operation. Four general-purpose output pairs can be configured independently as LVPECL, LVDS or HCSL differential outputs, or as two LVCMOS outputs, with I/O supplies mixed between 1.8V (LVDS and LVCMOS), 2.5V and 3.3V.

Two selection pins give access to up to four configurations through GPIO or a bootstrap circuit, and either of two I2C addresses can be selected.

Functional Block Diagram

Figure 1. SYKG6965 Block Diagram



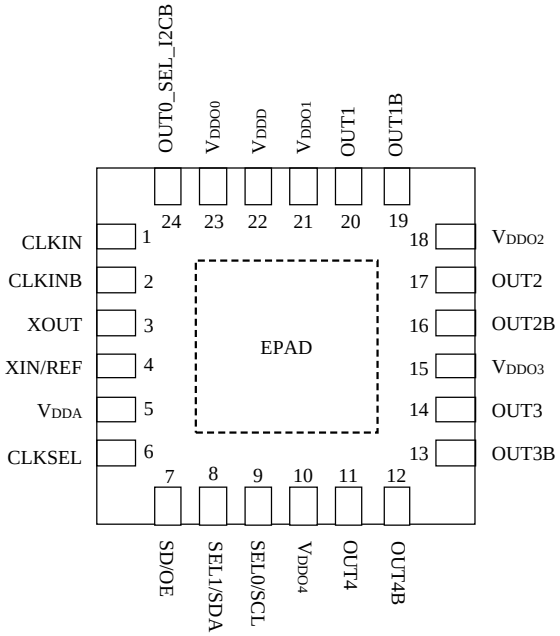
Notes:

1. FOD: Fraction Output Divider
   OTP: One-Time Programmable
   PLL: Phase Locked Loop
   SSC: Spread Spectrum Clocking

1 Pin Information

1.1 Pin Assignment

Figure 2. 24-VFQFPN Pin Assignment, 4.0mm x 4.0mm x 0.9mm, 0.5mm Pitch (Top view)



4 × 4 mm 24-VFQFPN

1.2 Pin Description

Table 1. Pin Description (24-VFQFPN) (Sheet 1 of 2)

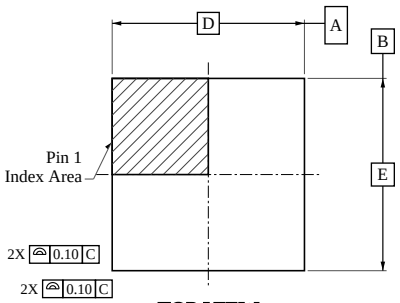
Pin NO.	Pin Name	Type	Description
1	CLKIN	Input	AC-coupled differential clock input.
2	CLKINB	Input	AC-coupled complementary differential clock input.
3	XOUT	Output	Crystal oscillator interface output.
4	XIN/REF	Input	Crystal oscillator interface input, or single-ended LVCMOS clock input. The input voltage must not exceed 1.2V.
5	VDDA	Power	Analog power supply. Connect to 1.8V ~ 3.3V. VDDA and VDDD should be set to the same voltage.
6	CLKSEL	Input	Input clock selection (internal pull-down). 0 = XIN/REF, XOUT (default); 1 = CLKIN, CLKINB.
7	SD/OE	Input	Output enable (OE) or chip power-down (SD) (internal pull-down).
8	SEL1/SDA	Input	Configuration selection pin, or I2C SDA input selected by OUT0_SEL_I2CB. Internal weak pull-up and pull-down.
9	SEL0/SCL	Input	Configuration selection pin, or I2C SCL input selected by OUT0_SEL_I2CB. Internal weak pull-up and pull-down.

Table 1. Pin Description (24-VFQFPN) (Sheet 2 of 2)

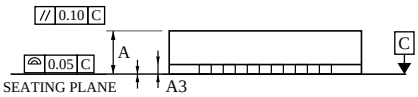
Pin NO.	Pin Name	Type	Description
10	VDDO4	Power	Output power supply for OUT4/OUT4B. Connect to 1.8V ~ 3.3V.
11	OUT4	Output	Output clock 4.
12	OUT4B	Output	Complementary output clock 4.
13	OUT3B	Output	Complementary output clock 3.
14	OUT3	Output	Output clock 3.
15	VDDO3	Power	Output power supply for OUT3/OUT3B. Connect to 1.8V ~ 3.3V.
16	OUT2B	Output	Complementary output clock 2.
17	OUT2	Output	Output clock 2.
18	VDDO2	Power	Output power supply for OUT2/OUT2B. Connect to 1.8V ~ 3.3V.
19	OUT1B	Output	Complementary output clock 1.
20	OUT1	Output	Output clock 1.
21	VDDO1	Power	Output power supply for OUT1/OUT1B. Connect to 1.8V ~ 3.3V.
22	VDDD	Power	Digital power supply. Connect to 1.8V ~ 3.3V. VDDA and VDDD should be set to the same voltage.
23	VDDO0	Power	Power supply for OUT0_SEL_I2CB; sets the OUT0 output level. Connect to 1.8V ~ 3.3V.
24	OUT0_SEL_I2CB	Input/Output	Latch input and LVCMOS reference output. At power-up, 10kΩ pull-up → pins 8/9 are SEL1/SEL0; pull-down or floating → pins 8/9 are SDA/SCL. After power-up this pin acts as one LVCMOS reference output.
25	GND	GND	Exposed pad (EPAD). Connect to ground.

2 Mechanical Package Data

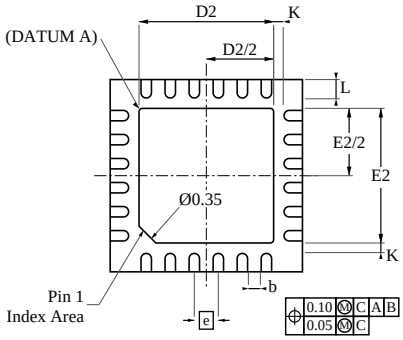
Figure 3. 24-VFQFPN Package Outline (4.0mm x 4.0mm x 0.9mm, 0.5mm Pitch)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
K		0.20	
D		4.00 BSC	
E		4.00 BSC	
D2	2.70	2.80	2.90
E2	2.70	2.80	2.90
e		0.50 BSC	
L	0.30	0.40	0.50
b	0.18	0.25	0.30

NOTES :

1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M - 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.

3 Ordering Information

Part Number	Package	Temperature	Crystal	Packing
SYKG6965-XX	4.0mm x 4.0mm x 0.9mm, 0.5mm pitch 24-VFQFPN	-40~+85°C	External	Tape & Reel