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# TPCAT809 Series

## 3-Pin Microprocessor Reset Circuits

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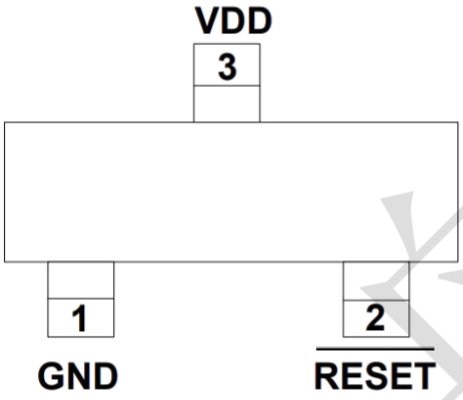
## Features

- Typical Quiescent Current of 3μA
- No External Components
- $V_{CC}$ Transient Immunity
- Correct Logic Output Guaranteed to $V_{CC}$=1.0V
- Push-Pull Low Active Reset Output
- Packages SOT323

## Applications

- Computers
- Embedded Systems
- Battery-Powered Equipments
- Intelligent Instruments
- CPU and Logic Circuit Reset
- Power Fail Detectors
- Automotive

## Pin Definition




SOT323

## Ordering Information

TPCAT809JSDI-GT3

**RESET VOLTAGE:**

L=4.63V
M=4.38V
J=4.00V
T=3.08V
S=2.93V
R=2.63V
Z=2.32V

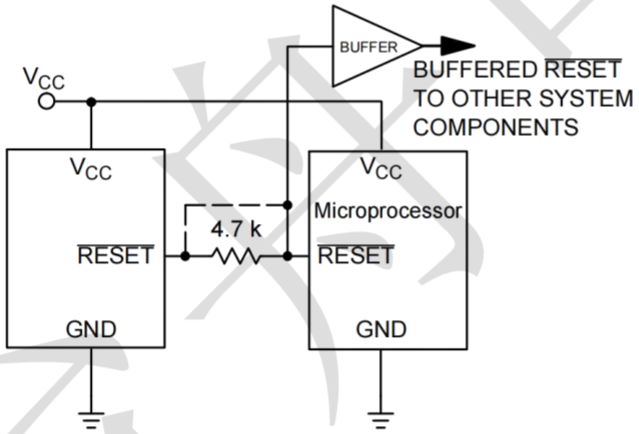
## PIN CONFIGURATION

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | GND | Ground |
| 2 | $\overline{\text{RESET}}$ | $\overline{\text{RESET}}$ output remains low while VCC is below the reset voltage threshold, and for a reset timeout period after VCC rises above reset threshold |
| 3 | VCC | Supply Voltage . |

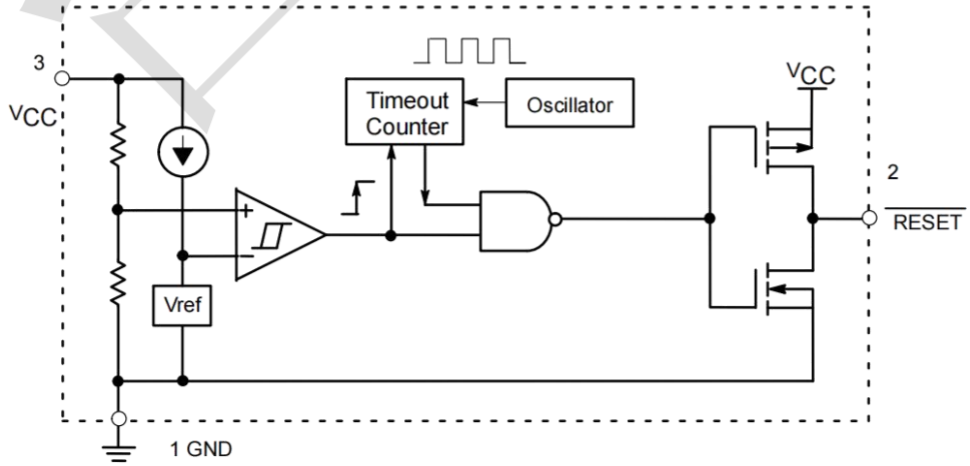
## Absolute Maximum Ratings (Note 1)

| Symbol | Parameter | Value | UNIT |
|---|---|---|---|
| VCC | Any pin with respect to ground | -0.3 to +6.0 | V |
| ICC | Input Current, VCC | 20 | mA |
| IO | Output Current,$\overline{\text{RESET}}$ | 20 | mA |
| | Rate of Rise, VCC | 100 | V/μs |
| PD | Continuous Power Dissipation | 250 | mW |
| TA | Operating Temperature Range | -40 to +85 | ℃ |
| TSTG | Storage Temperature Range | -65 to +105 | ℃ |
| $R_{\theta JC}$ | Thermal Resistance from Junction to Case | 110 | ºC/W |
| $R_{\theta JA}$ | Thermal Resistance from Junction to Ambient | 250 | ºC/W |

## TYPICAL APPLICATIN CIRCUIT




## FUNCTIONAL BLOCK DIAGRAM




**Series Complementary Active−Low Output**

## Electrical Characteristics

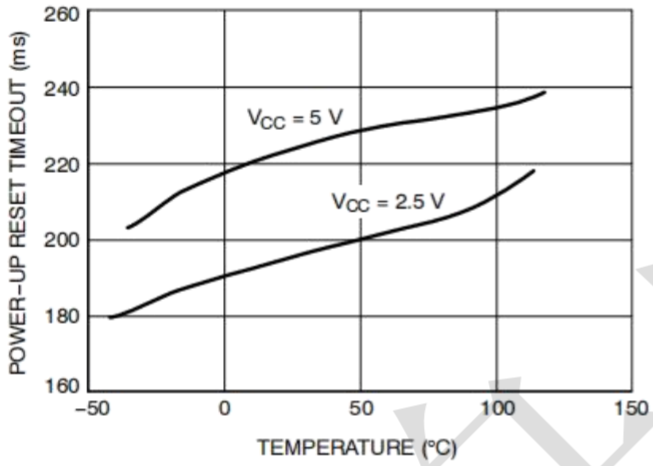
(VCC=full range, TA=-40°C to +85°C, unless otherwise noted. Typical values are at TA=+25°C, VCC=5V for L/M/J versions, VCC=3.3V for T/S versions, VCC=3V for R version, and VCC=2.5V for Z version. ) Note1

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | $V_{CC}$ Range | $T_A$=0°C to +70°C | | 1.0 | | 5.5 | V |
| $I_{CC}$ | Supply Current | $V_{CC}$<5.5V, L/M/J | | | 3 | 5 | μA |
| | | $V_{CC}$<3.6V, R/S/T/Z | | | 3 | 5 | |
| $V_{TH}$ | Reset Threshold | L | $T_A$=+25°C | 4.49 | 4.63 | 4.72 | V |
| | | | $T_A$=-40°C to +85°C | 4.44 | | 4.76 | |
| | | M | $T_A$=+25°C | 4.29 | 4.38 | 4.51 | |
| | | | $T_A$=-40°C to +85°C | 4.25 | | 4.55 | |
| | | J | $T_A$=+25°C | 3.90 | 4.00 | 4.10 | |
| | | | $T_A$=-40°C to +85°C | 3.86 | | 4.14 | |
| | | T | $T_A$=+25°C | 3.02 | 3.08 | 3.18 | |
| | | | $T_A$=-40°C to +85°C | 2.99 | | 3.21 | |
| | | S | $T_A$=+25°C | 2.83 | 2.93 | 2.97 | |
| | | | $T_A$=-40°C to +85°C | 2.80 | | 3.00 | |
| | | R | $T_A$=+25°C | 2.54 | 2.63 | 2.67 | |
| | | | $T_A$=-40°C to +85°C | 2.51 | | 2.69 | |
| | | Z | $T_A$=+25°C | 2.24 | 2.32 | 2.36 | |
| | | | $T_A$=-40°C to +85°C | 2.22 | | 2.38 | |
| Reset Threshold Tempco | | | | | 30 | | ppm/°C |
| $V_{CC}$ to Reset Delay | | $V_{CC}$=$V_{TH}$ to ($V_{TH}$–100mV) | | | 10 | | μs |
| Reset Active Timeout Period | | $T_A$=-40°C to +85°C | | 140 | 240 | 360 | ms |
| $V_{OL}$ | RESET Output Voltage Low (Push-Pull Active Low) | $V_{CC}$=$V_{TH}$ min, $I_{SINK}$=1.2mA,S/T/Z | | | | 0.3 | V |
| | | $V_{CC}$=$V_{TH}$ min, $I_{SINK}$=3.2mA,J/L/M | | | | 0.4 | |
| | | $V_{CC}$≤1.0V, $I_{SINK}$=50μA | | | | 0.3 | |
| $V_{OH}$ | RESET Output Voltage High (Push-Pull Active Low) | $V_{CC}$>$V_{TH}$ max, $I_{SOURCE}$=500μA, S/T/Z | | 0.8$V_{CC}$ | | | V |
| | | $V_{CC}$>$V_{TH}$ max, $I_{SOURCE}$=800μA, J/L/M | | $V_{CC}$–1.5 | | | |

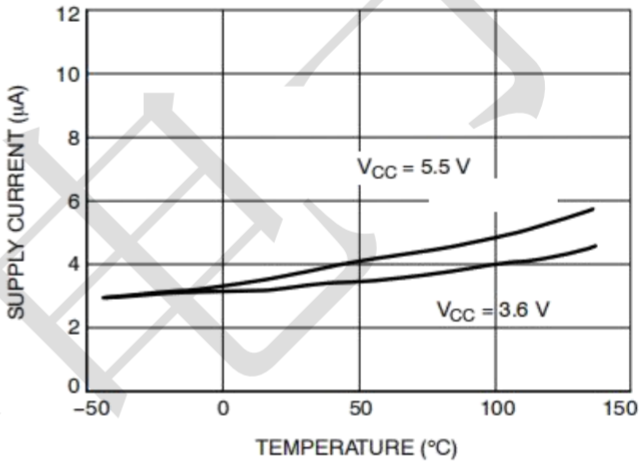
Note 1: Production testing done at TA=+25°C; limits over temperature guaranteed by design only.

## Typical Operating Characteristics

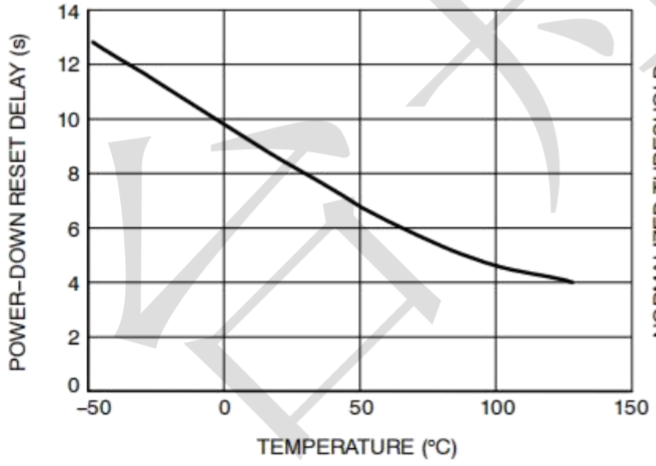
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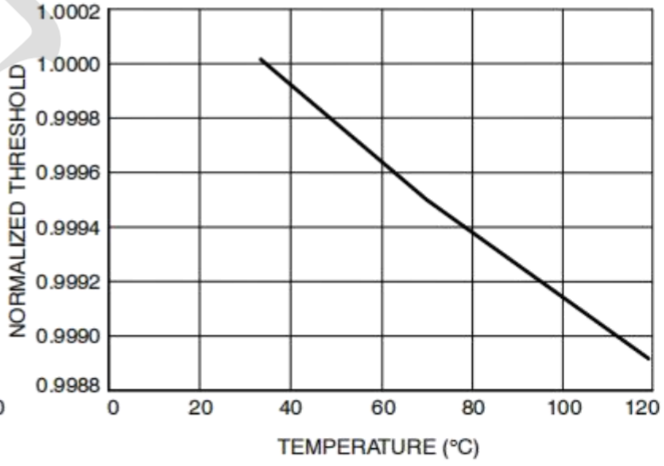

**Power−Up Reset Timeout vs. Temperature**




**Supply Current vs. Temperature (No Load, )**



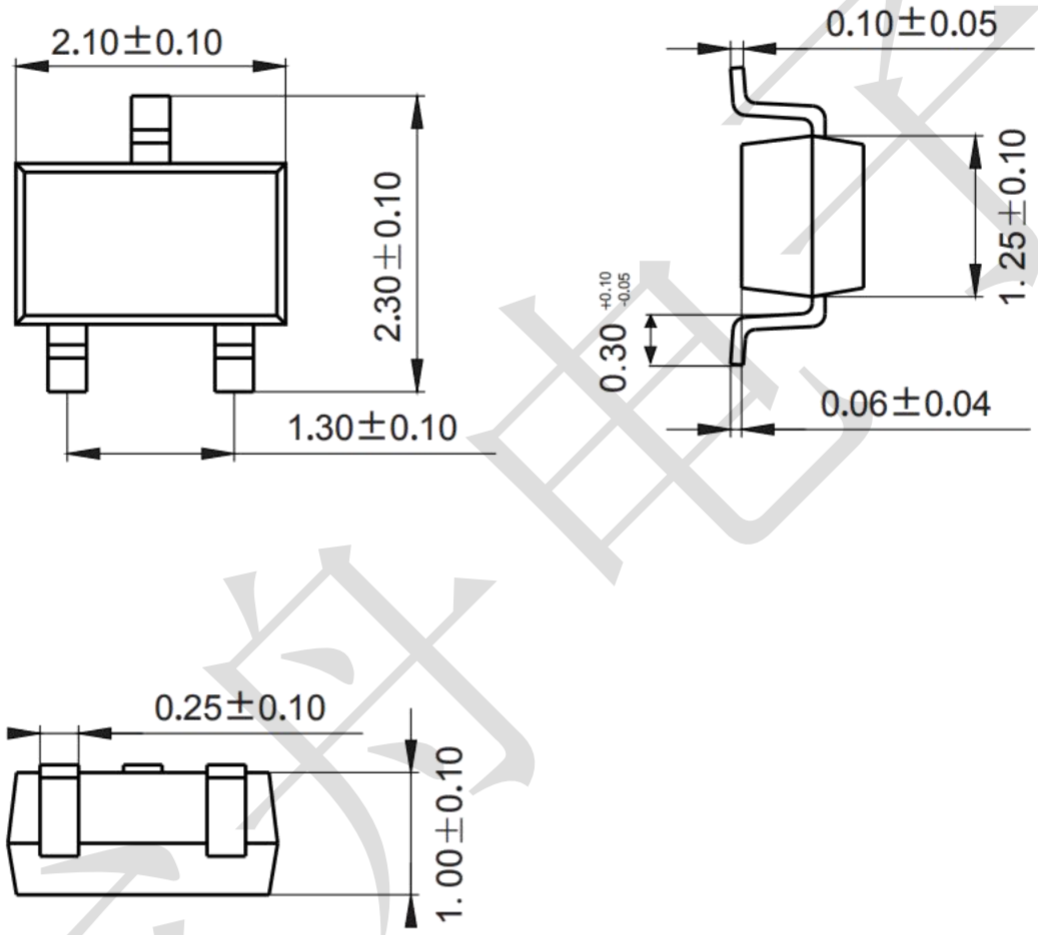

**Power−Down Reset Delay vs. Temperature**




**Normalized Reset Threshold vs. Temperature**

## Package Outline Dimensions (unit: mm)

**SOT323**




## Mounting Pad Layout (unit: mm)

