LXS0102HKEX-TP

2-Bit Bidirectional Voltage-Level Translator

GENERAL DESCRIPTION

This two-bit non-inverting translator is a bidirectional voltage-level translator and can be used to establish digital switching compatibility between mixed-voltage systems. It uses two separate configurable power-supply rails, with the A ports supporting operating voltages from 1.65V to 5.5V while it tracks the VCCA supply, and the B ports supporting operating voltages from 2.3V to 5.5V while it tracks the VCCB supply. This allows the support of both lower and higher logic signal levels while providing bidirectional translation capabilities between any of the 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

When the output-enable (OE) input is low, all I/Os are placed in the high-impedance state, which significantly reduces the power-supply quiescent current consumption. OE has an internal pull-down current source, as long as VCCA is powered.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

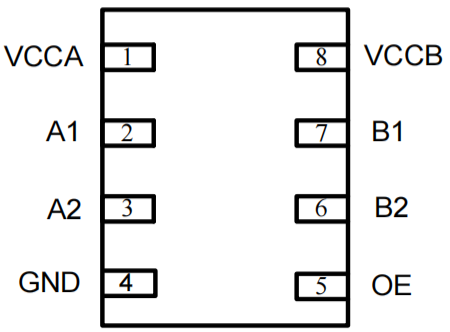
FEATURES

- No Direction-Control Signal Needed
- Data Rates
  24Mbps (Push-Pull)
  2Mbps (Open-Drain)
- 1.65V to 5.5V on A Ports and 2.3V to 5.5V on B Ports (VCCA ≤ VCCB)
- VCC Isolation: If Either VCC is at GND, Both Ports are in the High-Impedance State
- No Power-Supply Sequencing Required, Either VCCA or VCCB can be Ramped First
- I_{OFF}: Supports Partial-Power-Down Mode Operation
- Available in XTDFN1.4X1.0-8L package.

APPLICATIONS

I2C BUS
Portable POS Systems
Smart Card Readers
Cell-Phones
GPS
Portable Communication Devices

PIN CONFIGURATION (Top View)



XTDFN1.4X1.0-8L

PIN DESCRIPTION

PIN		NAME	FUNCTION
SOT	DFN/QFN		
1	8	V_{CCB}	B-Port Supply Voltage. 2.3V≤V_{CCB}≤5.5V.
2	7	B1	Input/Output B. Referenced to V_{CCB}.
3	6	B2	Input/Output B. Referenced to V_{CCB}.
4	5	OE	Output Enable (Active High). Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
5	4	GND	Ground.
6	3	A2	Input/Output A. Referenced to V_{CCA}.
7	2	A1	Input/Output A. Referenced to V_{CCA}.
8	1	V_{CCA}	A-Port Supply Voltage. 1.65V≤V_{CCA}≤5.5V and V_{CCA}≤V_{CCB}.

ABSOLUTE MAXIMUM RATINGS

V_{CCA}, Supply Voltage Range..... -0.3V to 6V

V_{CCB}, Supply Voltage Range..... -0.3V to 6V

V_I, A Port, B Port, OE Input Voltage Range (2)..... -0.3V to 6V

V_O, Voltage Range Applied to Any Output in the High- Impedance or Power-Off State (2)

A Port..... -0.3V to 6V

B Port..... -0.3V to 6V

V_O, Voltage Range Applied to Any Output in the High or Low State (2) (3)

A Port..... -0.3V to V_{CCA} + 0.3V

B Port..... -0.3V to V_{CCB} + 0.3V

I_{IK}, Input Clamp Current (VI < 0) ..... -50mA

I_{OK}, Output Clamp Current (VO < 0) ..... -50mA

I_O, Continuous Output Current..... ±50mA

Continuous Current through VCCA, VCCB, or GND..... ±100mA

Operating Temperature Range..... -40℃ to +85℃

Junction Temperature..... 150℃

Storage Temperature Range..... -65℃ to +150℃

Lead Temperature (Soldering, 10sec)..... 260℃

ESD

HBM B Port.....8KV

HBM Other Pin.....4KV

NOTE:

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute Maximum rating conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
3. The value of VCCA and VCCB are provided in the recommended operating conditions table.

ELECTRICAL CHARACTERISTICS

(V_{CCA} = 1.65V to 5.5V, V_{CCB} = 2.3V to 5.5V, typical values are at T_A = +25℃, unless otherwise noted)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
RECOMMENDED OPERATING CONDITIONS (1) (2)							
Supply Voltage (3)	V_{CCA}			1.65		5.5	V
	V_{CCB}			2.3		5.5	
High-Level Input Voltage (V_{IH})	A Port I/Os	V_{CCA} = 1.65V to 1.95V, V_{CCB} = 2.3V to 5.5V		V_{CCI} - 0.2		V_{CCI}	V
		V_{CCA} = 2.3V to 5.5V, V_{CCB} = 2.3V to 5.5V		V_{CCI} - 0.4		V_{CCI}	
	B Port I/Os			V_{CCI} - 0.4		V_{CCI}	
	OE Input			V_{CCA}×0.8		5.5	
Low-Level Input Voltage (V_{IL})	A Port I/Os			0		0.15	V
	B Port I/Os			0		0.15	
	OE Input			0		V_{CCA}×0.25	
Input Transition Rise or Fall Rate (Δt/ΔV)		A Port I/Os Push-Pull Driving				10	ns/V
		B Port I/Os Push-Pull Driving				10	
		Control Input				10	
ELECTRICAL CHARACTERISTICS							
A Port High Level Output Voltage (V_{OHA})		I_{OH} = -20μA, V_{IB} ≥V_{CCB} - 0.4V		V_{CCA}×0.7			V
A Port Low Level Output Voltage (V_{OLA})		I_{OL} = 1mA, V_{IB} ≤ 0.15V				0.4	
B Port High Level Output Voltage (V_{OHB})		I_{OH} = -20μA, V_{IA} ≥V_{CCA} - 0.4V		V_{CCB}×0.7			
B Port Low Level Output Voltage (V_{OLB})		I_{OL} = 1mA, V_{IA} ≤ 0.15V				0.4	
Input Leakage Current (I_I)	OE				0.5		μA
Power Off Leakage Current (I_{OFF})	A Port	V_{CCA} = 0V, V_{CCB} = 0V to 5.5V			0.1		
	B Port	V_{CCA} = 0V to 5.5V, V_{CCB} = 0V			0.1		
3-State Output Leakage (I_{OZ})	A or B Port	OE = 0V			0.1		
Quiescent Supply Current (I_{CCA})		V_I = V_O = OPEN, I_O = 0	V_{CCA} = 1.65V to V_{CCB}, V_{CCB} = 2.3V to 5.5V		0.1		μA
			V_{CCA} =5.5V, V_{CCB} = 0V		0.1		
			V_{CCA} = 0V, V_{CCB} = 5.5V		0.1		
Quiescent Supply Current (I_{CCB})		V_I = V_O = OPEN, I_O = 0	V_{CCA} = 1.65V to V_{CCB}, V_{CCB} = 2.3V to 5.5V		7		μA
			V_{CCA} =5.5V, V_{CCB} = 0V		0.1		
			V_{CCA} = 0V, V_{CCB} = 5.5V		0.1		
Quiescent Supply Current (I_{CCA} + I_{CCB})		V_I = V_O = OPEN, I_O = 0	V_{CCA} = 1.65V to V_{CCB}, V_{CCB} = 2.3V to 5.5V		7.1		μA

ELECTRICAL CHARACTERISTICS

(V_{CCA} = 1.65V to 5.5V, V_{CCB} = 2.3V to 5.5V, typical values are at T_A = +25℃, unless otherwise noted)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Supply Current (I_{CCZA})	$V_I = V_{CCI}$, I_O = 0, OE = GND	V_{CCA} = 1.65V to V_{CCB}, V_{CCB} = 2.3V to 5.5V		0.1		μA
		V_{CCA} =5.5V, V_{CCB} = 0V		0.1		
		V_{CCA} = 0V, V_{CCB} = 5.5V		0.1		
Quiescent Supply Current (I_{CCZB})	$V_I = V_{CCI}$, I_O = 0, OE = GND	V_{CCA} = 1.65V to V_{CCB}, V_{CCB} = 2.3V to 5.5V		0.1		μA
		V_{CCA} =5.5V, V_{CCB} = 0V		0.1		
		V_{CCA} = 0V, V_{CCB} = 5.5V		0.1		
OE Input Capacitance (C_I)	V_{CCA} = 3.3V, V_{CCB} = 3.3V			3.6		pF
Input/Output Capacitance A Port (C_{IO})	V_{CCA} = 3.3V, V_{CCB} = 3.3V			5.4		pF
Input/Output Capacitance B Port (C_{IO})				6.3		

NOTES:

1. V_{CCI} is the V_{CC} associated with the input port.
2. V_{CCO} is the V_{CC} associated with the output port.
3. V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 5.5V.

TIMING REQUIREMENTS

(typical values are at T_A = +25℃, unless otherwise noted)

			V_{CCB} = 2.5V	V_{CCB} = 3.3V	V_{CCB} = 5V	UNITS
			TYP	TYP	TYP	
(T_A = +25℃, V_{CCA} = 1.8V, unless otherwise noted.)						
Data Rate	Push-Pull Driving		21	22	24	Mbps
	Open-Drain Driving		2	2	2	
Pulse Duration (t_W)	Push-Pull Driving	Data Inputs	47	45	41	ns
	Open-Drain Driving		500	500	500	
(T_A = +25℃, V_{CCA} = 2.5V, unless otherwise noted.)						
Data Rate	Push-Pull Driving		20	22	24	Mbps
	Open-Drain Driving		2	2	2	
Pulse Duration (t_W)	Push-Pull Driving	Data Inputs	50	45	41	ns
	Open-Drain Driving		500	500	500	
(T_A = +25℃, V_{CCA} = 3.3V, unless otherwise noted.)						
Data Rate	Push-Pull Driving			23	24	Mbps
	Open-Drain Driving			2	2	
Pulse Duration (t_W)	Push-Pull Driving	Data Inputs		43	41	ns
	Open-Drain Driving			500	500	
(T_A = +25℃, V_{CCA} = 5V, unless otherwise noted.)						
Data Rate	Push-Pull Driving				24	Mbps
	Open-Drain Driving				2	
Pulse Duration (t_W)	Push-Pull Driving	Data Inputs			41	ns
	Open-Drain Driving				500	

SWITCHING CHARACTERISTICS

(V_{CCA} = 1.8V, typical values are at T_A = +25℃, unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 2.5V	V_{CCB} = 3.3V	V_{CCB} = 5V	UNITS
t_{PHL}	A	B	Push-Pull Driving	2.4	3.0	4.3	ns
			Open-Drain Driving	26.0	26.3	26.7	
t_{PLH}			Push-Pull Driving	4.0	3.6	3.5	
			Open-Drain Driving	175	145	110	
t_{PHL}	B	A	Push-Pull Driving	2.0	1.9	2.1	ns
			Open-Drain Driving	26.0	26.1	26.2	
t_{PLH}			Push-Pull Driving	1.7	1.5	1.4	
			Open-Drain Driving	133	69	51	
t_{EN} (t_{PZH} & t_{PZL})	OE	A or B		17	15	14	ns
t_{DIS} (t_{PHZ} & t_{PLZ})	OE	A or B		614	616	626	
t_{rA}	A Port Rise Time		Push-Pull Driving	6.6	5.8	5.4	ns
			Open-Drain Driving	89	31	10	
t_{rB}	B Port Rise Time		Push-Pull Driving	5.6	4.6	3.9	ns
			Open-Drain Driving	128	98	58	
t_{fA}	A Port Fall Time		Push-Pull Driving	2.9	2.7	2.6	ns
			Open-Drain Driving	1.9	1.7	1.6	
t_{fB}	B Port Fall Time		Push-Pull Driving	4.6	5.9	8.0	ns
			Open-Drain Driving	2.2	2.3	2.9	
$t_{sk(0)}$	Channel-to-Channel Skew			0.5	0.5	0.5	ns
Data Rate			Push-Pull Driving	21	22	24	Mbps
			Open-Drain Driving	2	2	2	

SWITCHING CHARACTERISTICS

(V_{CCA} = 2.5V, typical values are at T_A = +25℃, unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 2.5V	V_{CCB} = 3.3V	V_{CCB} = 5V	UNITS
t_{PHL}	A	B	Push-Pull Driving	2.7	3.3	4.8	ns
			Open-Drain Driving	26.2	26.4	26.7	
t_{PLH}			Push-Pull Driving	2.6	2.4	2.3	
			Open-Drain Driving	169	144	110	
t_{PHL}	B	A	Push-Pull Driving	2.4	2.3	2.4	ns
			Open-Drain Driving	26.3	26.4	26.5	
t_{PLH}			Push-Pull Driving	2.0	1.9	1.8	
			Open-Drain Driving	165	118	55	
t_{EN} (t_{PZH} & t_{PZL})	OE	A or B		14	13	12	ns
t_{DIS} (t_{PHZ} & t_{PLZ})	OE	A or B		630	635	640	
t_{rA}	A Port Rise Time		Push-Pull Driving	3.2	2.8	2.6	ns
			Open-Drain Driving	120	70	10	
t_{rB}	B Port Rise Time		Push-Pull Driving	4.5	3.4	2.6	ns
			Open-Drain Driving	122	96	62	
t_{fA}	A Port Fall Time		Push-Pull Driving	4.9	5.0	4.8	ns
			Open-Drain Driving	2.0	1.9	1.7	
t_{fB}	B Port Fall Time		Push-Pull Driving	4.8	6.1	8.3	ns
			Open-Drain Driving	1.9	2.1	2.7	
$t_{sk(0)}$	Channel-to-Channel Skew			0.5	0.5	0.5	ns
Data Rate			Push-Pull Driving	20	22	24	Mbps
			Open-Drain Driving	2	2	2	

SWITCHING CHARACTERISTICS

(V_{CCA} = 3.3V, typical values are at T_A = +25℃, unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 3.3V	V_{CCB} = 5V	UNITS
t_{PHL}	A	B	Push-Pull Driving	3.5	4.9	ns
			Open-Drain Driving	26.3	26.7	
t_{PLH}			Push-Pull Driving	2.2	2.0	
			Open-Drain Driving	133	104	
t_{PHL}	B	A	Push-Pull Driving	3.0	3.2	ns
			Open-Drain Driving	26.6	26.8	
t_{PLH}			Push-Pull Driving	1.8	1.7	
			Open-Drain Driving	132	83	
t_{EN} (t_{PZH} & t_{PZL})	OE	A or B		12	11	ns
t_{DIS} (t_{PHZ} & t_{PLZ})	OE	A or B		630	635	
t_{rA}	A Port Rise Time		Push-Pull Driving	2.2	2.0	ns
			Open-Drain Driving	87	36	
t_{rB}	B Port Rise Time		Push-Pull Driving	2.9	2.3	ns
			Open-Drain Driving	87	56	
t_{fA}	A Port Fall Time		Push-Pull Driving	6.2	5.8	ns
			Open-Drain Driving	2.3	2.0	
t_{fB}	B Port Fall Time		Push-Pull Driving	6.5	8.2	ns
			Open-Drain Driving	2.0	2.5	
$t_{sk(0)}$	Channel-to-Channel Skew			0.5	0.5	ns
Data Rate			Push-Pull Driving	23	24	Mbps
			Open-Drain Driving	2	2	

SWITCHING CHARACTERISTICS

(V_{CCA} = 5.0V, typical values are at T_A = +25℃, unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CCB} = 5V	UNITS
t_{PHL}	A	B	Push-Pull Driving	5.4	ns
			Open-Drain Driving	26.7	
t_{PLH}			Push-Pull Driving	1.9	
			Open-Drain Driving	120	
t_{PHL}	B	A	Push-Pull Driving	5.6	ns
			Open-Drain Driving	27.3	
t_{PLH}			Push-Pull Driving	1.7	
			Open-Drain Driving	126	
t_{EN} (t_{PZH} & t_{PZL})	OE	A or B		10	ns
t_{DIS} (t_{PHZ} & t_{PLZ})	OE	A or B		636	
t_{rA}	A Port Rise Time		Push-Pull Driving	1.8	ns
			Open-Drain Driving	79	
t_{rB}	B Port Rise Time		Push-Pull Driving	2.2	ns
			Open-Drain Driving	73	
t_{fA}	A Port Fall Time		Push-Pull Driving	8.7	ns
			Open-Drain Driving	2.7	
t_{fB}	B Port Fall Time		Push-Pull Driving	8.6	ns
			Open-Drain Driving	2.4	
$t_{sk(0)}$	Channel-to-Channel Skew			0.5	ns
Data Rate			Push-Pull Driving	24	Mbps
			Open-Drain Driving	2	

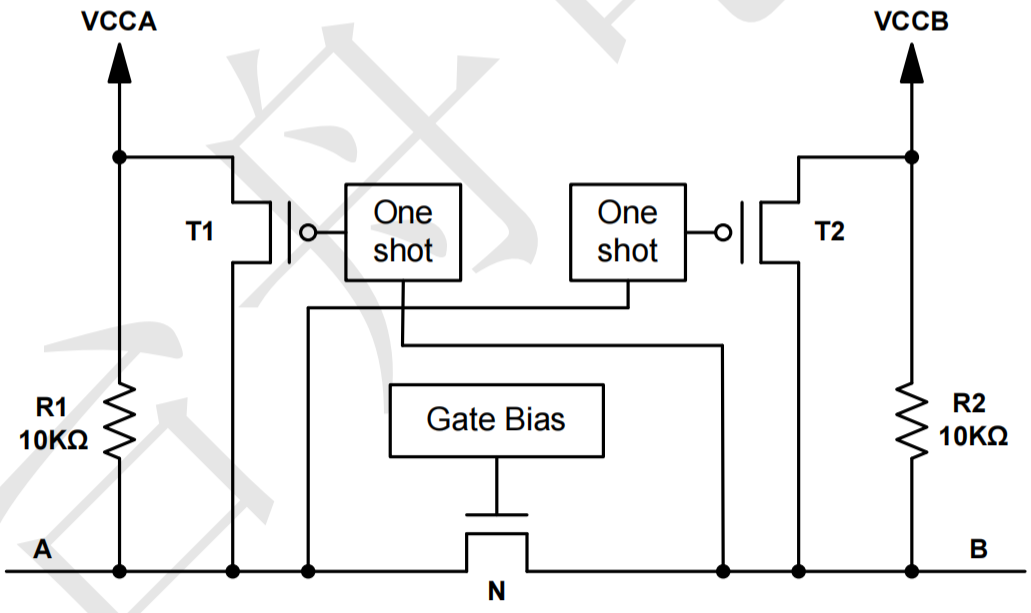
APPLICATION INFORMATION

The can be used to bridge the digital-switching compatibility gap between two voltage nodes to successfully interface logic threshold levels found in electronic systems. It should be used in a point-to-point topology for interfacing devices or systems operating at different interface voltages with one another. Its primary target application use is for interfacing with open-drain drivers on the data I/Os such as I2C or 1-wire, where the data is bidirectional and no control signal is available. The can also be used in applications where a push-pull driver is connected to the data I/Os

Block Diagram

The architecture (see Figure 1) is an auto-direction-sensing based translator that does not require a direction-control signal to control the direction of data flow from A to B or from B to A.

These two bidirectional channels independently determine the direction of data flow without a direction-control signal. Each I/O pin can be automatically reconfigured as either an input or an output, which is how this auto-direction feature is realized.



Block Diagram of TXS0102DDFR-TP **I/O Cell**

The employs two key circuits to enable this voltage translation: An N-channel pass-gate transistor topology that ties the A port to the B port. Output one-shot (O.S.) edge-rate accelerator circuitry to detect and accelerate rising edges on the A or B ports.

Input Driver Requirements

The fall time (t_{fA}, t_{fB}) of a signal depends on the output impedance of the external device driving the data I/Os of the . Similarly, the t_{PHL} and data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and data rates in the datasheet assume that the output impedance of the external driver is less than 50Ω.

Power Up

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first.

Output Load Considerations

We recommend careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 30ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

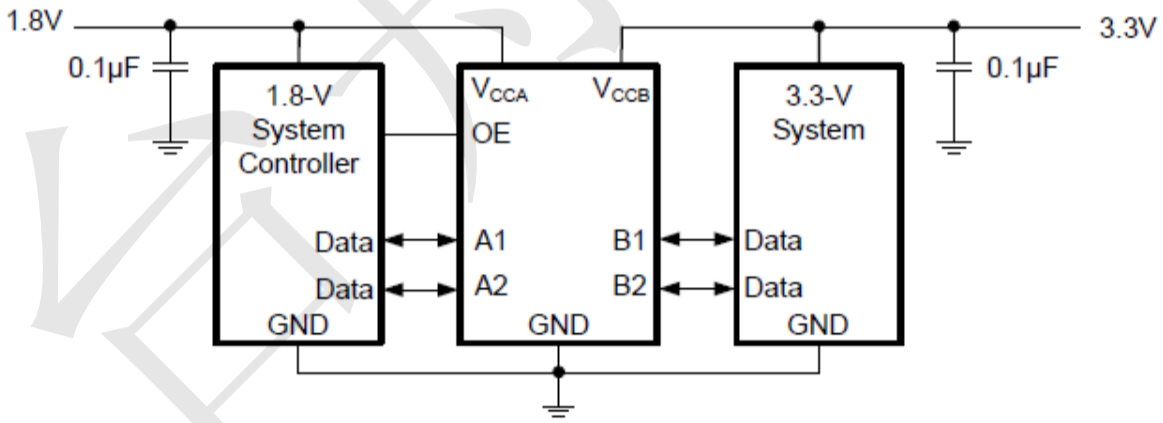
Enable and Disable

The has an OE input that is used to disable the device by setting OE low, which places all I/Os in the Hi-Z state. OE has an internal pull-down current source, as long as V_{CCA} is powered. The disable time (t_{DIS}) indicates the delay between the time when OE goes low and when the outputs are disabled (Hi-Z). The enable time (t_{EN}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

Pull-up or Pull-down Resistors on I/O Lines

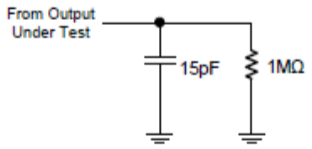
Each A port I/O has an internal 10kΩ pull-up resistor to V_{CCA}, and each B port I/O has an internal 10kΩ pull-up resistor to V_{CCB}. If a smaller value of pull-up resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10kΩ resistors). Adding lower value pull-up resistors will effect V_{OL} levels, however. The internal pull-ups of the are disabled when the OE pin is low.

Typical Application Circuit

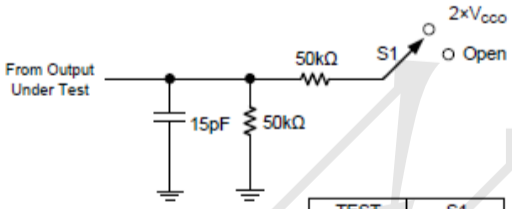


Typical Application Circuit

Test Circuits

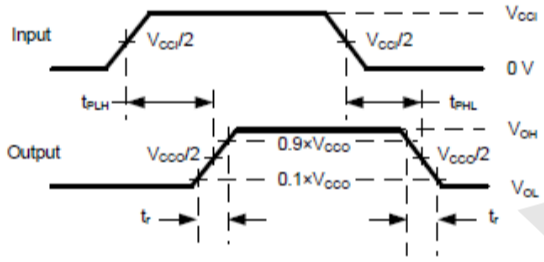


LOAD CIRCUIT FOR MAX DATA RATE, PULSE DURATION PROPAGATION DELAY OUTPUT RISE AND FALL TIME MEASUREMENT

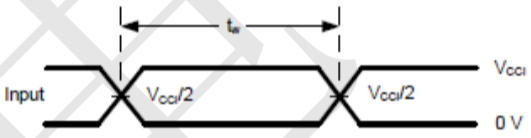


LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT

TEST	S1
t_{PZL}/t_{PLZ} t_{PHZ}/t_{PZH}	$2\times V_{CCO}$ Open



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



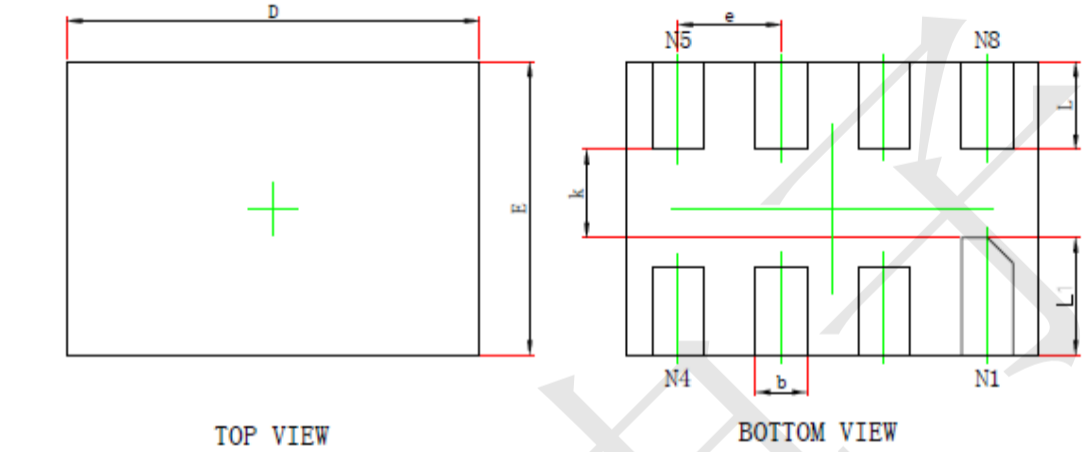
VOLTAGE WAVEFORMS PULSE DURATION

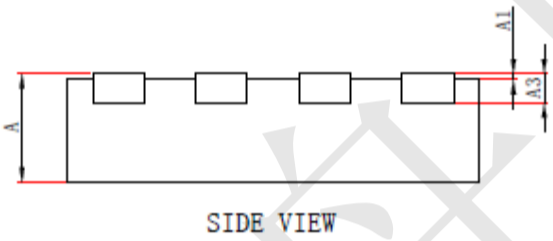
A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR≤10MHz, Z_O=50Ω,dv/dt≥1V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. V_{CCI} is the V_{CC} associated with the input port.
F. V_{CCO} is the V_{CC} associated with the output port.
G. All parameters and waveforms are not applicable to all devices.

Load Circuits and Voltage Waveforms

Outline Drawing

XTDFN1.4X1.0-8L





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.340	0.400	0.013	0.016
A1	0.000	0.050	0.000	0.002
A3	0.100REF.		0.004REF.	
D	1.350	1.450	0.053	0.057
E	0.950	1.050	0.037	0.041
D1	——	——	——	——
E1	——	——	——	——
k	0.200MIN.		0.008MIN.	
b	0.150	0.200	0.006	0.008
e	0.350TYP.		0.014TYP.	
L	0.250	0.350	0.010	0.014
L1	0.350	0.450	0.014	0.018