74AHC2G00DP-TP

Dual 2-Input Positive-NAND Gate

Features

- Designed for 2.0V to 5.5V V_{CC} Operation
- Over-voltage Tolerant Inputs Accept Voltages to 5.5V
- ±8mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
- These Devices are Pb-Free and RoHS Compliant
- ESD Protection Complies with JESD22 Standard
  -- HBM: ±2000V Pass (JEDEC JS-001)
  -- CDM: ±1000V Pass (JEDEC JS-002)
- Latch-up Performance Exceeds ±100mA per JEDEC JESD78F
- Part No. and Package Information

General Description

The 74AHC2G00DP-TP is a dual 2-input positive -NAND gate operating from a 2.0V to 5.5V supply. This device is fabricated with advanced CMOS technology to achieve ultra-high speed with high output drive.

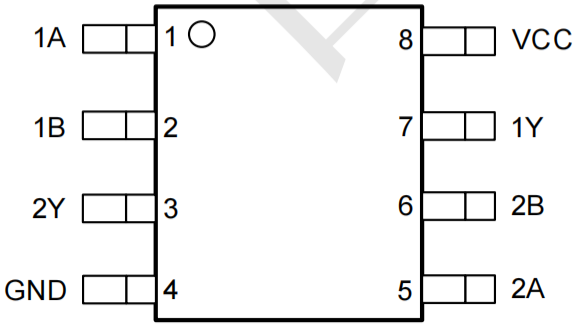
Block Diagram



Ordering Information

ORDER NUMBER	PACKAGE DESCRIPTION	PACKAGE OPTION
74AHC2G00DP-TP	MSOP8	Tape and Reel,3000

Pin Configuration



MSOP8

Functional Table

Input		Output
xA	xB	xY
L	L	H
L	H	H
H	L	H
H	H	L

Pin Function

Pin No.	Pin Name	Function
1	1A	Channel 1, Input A
2	1B	Channel 1, Input B
3	2Y	Channel 2, Output Y
4	GND	Ground
5	2A	Channel 2, Input A
6	2B	Channel 2, Input B
7	1Y	Channel 1, Output Y
8	VCC	Supply Voltage

Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage (VCC Pin)		-0.5 to 7.0	V
I_{IK}	DC Input Diode Current, V_I < GND		-20	mA
V_I	DC Input Voltage (1)		-0.5 ≤ V_I ≤ 7.0	V
I_{OK}	DC Output Diode Current, V_O < GND		±20	mA
V_O	DC Output Voltage Output in Higher or Low State		-0.5 to V_{CC} + 0.5	V
I_O	DC Output Sink Current, V_O = 0V to V_{CC}		±25	mA
I_{CC}	DC Supply Current per Supply Pin		50	mA
I_{GND}	DC Ground Current per Supply Pin		-50	mA
T_J	Max Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-65 to 150	°C
V_{ESD}	ESD Classification	Human Body Model (2)	±2000	V
		Charged Device Model (3)	±1000	
I_{LU}	Max Latch Up Current Above V_{CC} and GND at 125°C (4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: I_O absolute maximum rating must be observed.

Note2: HBM tested per JEDEC JS-001;

Note3: CDM tested per JEDEC JS-002;

Note4: Latch up Current Maximum Rating tested per JEDEC JESD78F.

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage Operating		2.0	5.5	V
V_I	DC Input Voltage		0	V_{CC}	V
V_O	DC Output Voltage (High or Low State)		0	V_{CC}	V
T_A	Operating Temperature Range		-40	125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V ± 0.3V		100	ns/V
		V_{CC} = 5.0V ± 0.5V		20	

Electrical Characteristics

DC Electrical Characteristics

Symbol	Parameter	Condition	V_{CC}(V)	T_A = 25 °C			-40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		2.0	1.5			1.5		V
			3.0	2.1			2.1		
			5.5	3.85			3.85		
V_{IL}	Low-Level Input Voltage		2.0			0.5		0.5	V
			3.0			0.9		0.9	
			5.5			1.65		1.65	
V_{OH}	High-Level Output Voltage	I_{OH} = -50uA	2~4.5	V_{CC} - 0.1	V_{CC}		V_{CC} - 0.1		V
		I_{OH} = -4mA	3	2.58			2.4		
		I_{OH} = -8mA	4.5	3.94			3.7		
V_{OL}	Low-Level Output Voltage	I_{OL} = 50uA	2~5.5			0.1		0.1	V
		I_{OL} = 4mA	3			0.36		0.55	
		I_{OL} = 8mA	4.5			0.36		0.55	
I_I	Input Leakage Current	V_I = 5.5V or GND	0~5.5			0.1		2.0	μA
I_{CC}	Quiescent Supply Current	V_I = 5.5V or GND	5.5			10		40	μA

AC Electrical Characteristics

$t_r = t_f$ = 3ns, R_L = 1kΩ

Symbol	Parameter	Condition	V_{CC}(V)	T_A = 25°C			-40°C ≤ T_A ≤ 125°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay (Figure3 and 4)	C_L = 15pF	3~3.6		4.6	6	1.0	8	ns
		C_L = 50pF	3~3.6		5.3	6.9	1.0	8.6	
		C_L = 15pF	4.5~5.5		3.4	4.4	1.0	6.1	
		C_L = 50pF	4.5~5.5		3.9	5.1	1.0	6.5	

Capacitance Characteristics

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.5V, V_I = 0V or V_{CC}	5	pF
C_{PD}	Power Dissipation Capacitance (5)	10MHz, V_{CC} = 3.3V, V_I = 0V or V_{CC}	25	pF

Note5: C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

AC Test Circuit

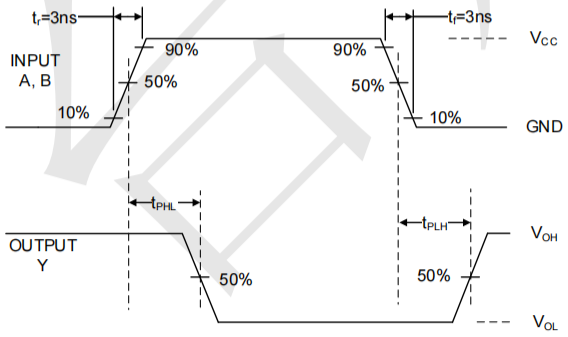


Figure3. Switching Waveform

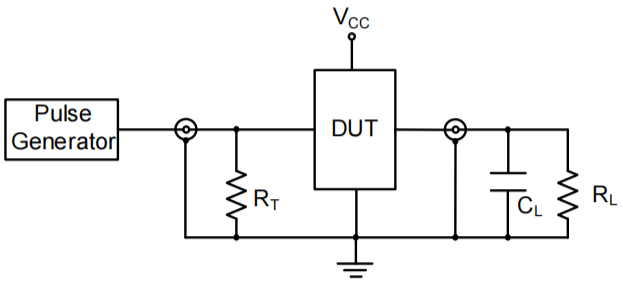
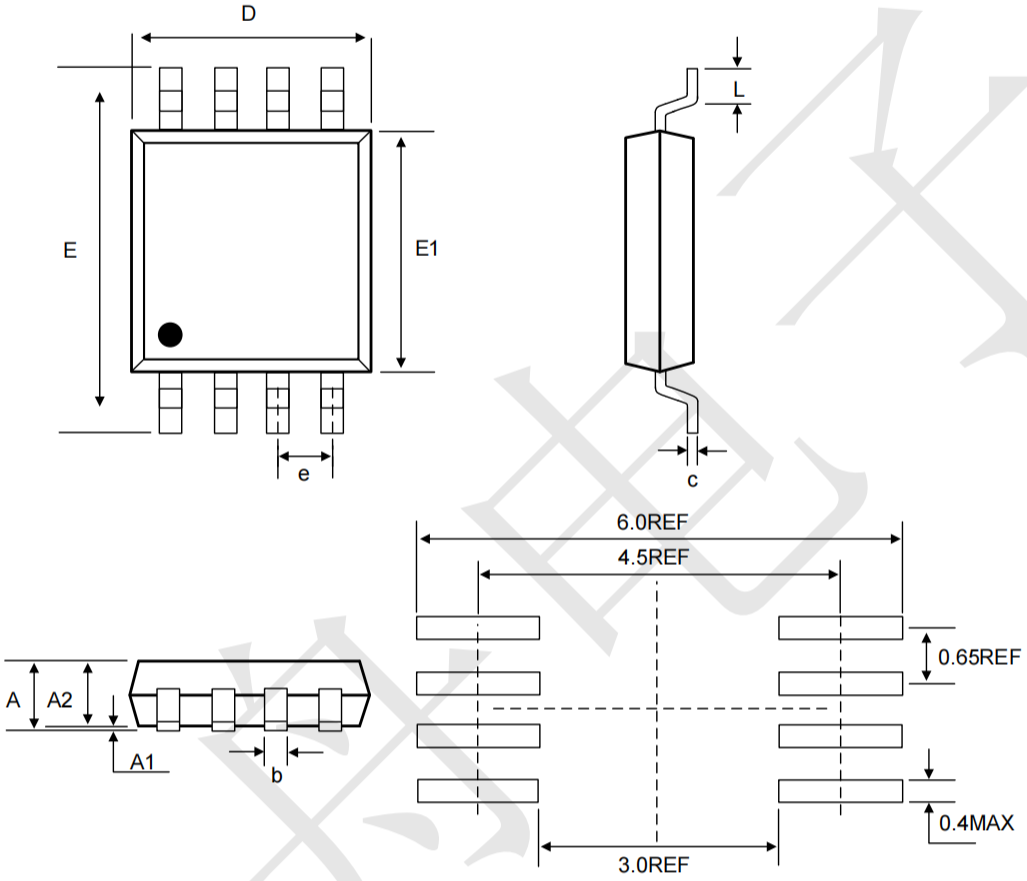


Figure4. Test Circuit

Package Dimension

MSOP8(3.0mm × 3.0mm)



COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	-	0.15
A2	0.75	0.85	0.95
b	0.22	0.30	0.38
c	0.08	0.1	0.20
D	2.90	3.00	3.10
E	3.90	-	5.10
E1	2.90	3.00	3.10
e	0.65BSC		
L	0.33	-	0.7