LPDDR4X Datasheet

BWMZEX32H2A-16G-X

Released

Ver.2.0

Oct.2022

DAT-CES-0129-A

深圳佰维存储科技股份有限公司
BIWIN STORAGE TECHNOLOGY CO.,LTD.

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Revision History

Version	Date	Description
1.0	July.2022	First Release
2.0	Oct.2022	IDD Parameters Update

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1. Features

•Ultra-low-voltage core and I/O power supplies

– VDD1 = 1.70–1.95V; 1.80V nominal

– VDD2 = 1.06–1.17V; 1.10V nominal

– VDDQ = 0.57–0.65V; 0.60Vnominal
or VDDQ = 1.06–1.17V; 1.10V nominal

•Frequency range

–1866–10 MHz (data rate range: 3733–20 Mb/s/ pin)

•16n prefetch DDR architecture

•8 internal banks per channel for concurrent operation

•Single-data-rate CMD/ADR entry

•Bidirectional/differential data strobe per byte lane

•Programmable READ and WRITE latencies (RL/WL)

•Programmable and on-the-fly burst lengths (BL = 16, 32)

•Directed per-bank refresh for concurrent bank operation and ease of command scheduling

•Up to 7.5 GB/s per die

•On-chip temperature sensor to control self refresh rate

•Partial-array self refresh (PASR)

•Selectable output drive strength (DS)

•Clock-stop capability

•RoHS-compliant, “green” packaging

•Programmable VSS (ODT) termination

Options

• VDD1/VDD2/VDDQ: 1.80V/1.10V/0.60V or 1.10V

• Array configuration

– 512Meg x 32 (2channelsx16I/O)

• Device configuration

– 2 die in package

• FBGA “green” package

– 200-ball FBGA (10mm x 14.5mm)

• Speed grade, cycle time

– 535ps@RL=32/36

• Operating temperature range

– –25°C to +85°C

Clock Rate (MHz)	Data Rate (Mb/s/pin)	RL	WL
1866	3733	32/36	16/30

Table 1 Key Timing Parameters

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2. Product Information

Part ID	Capacity	Size	Package
BWMZEX32H2A-16G-X	16Gb	10mm*14.5mm*0.9mm	FBGA200

		512M32 (16Gb/package)
Die organization in the package	Channel A, rank 0	x16 mode × 1 die
	Channel B, rank 0	x16 mode × 1 die
	Channel A, rank 1	-
	Channel B, rank 1	-
Density per die		8Gb
Density per channel		8Gb
Configuration		64Mb × 16 DQ× 8 banks
Number of channels (per die)		1
Number of banks (per channel)		8
Array prefetch (bits, per channel)		256
Number of rows (per channel)		65,536
Number of columns (fetch boundaries)		64
Page size (bytes)		2048
Channel density (bits per channel)		8,589,934,592
Total density (bits per die)		8,589,934,592
Bank address		BA[2:0]
×16	Row address	R[15:0]
	Column address	C[9:0]
Burst starting address boundary		64bit

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Note: 1. Refer to Package Block Diagram section in Product Specification and SDRAM Addressing section in General LPDDR4X specification.

2.1 MR0, MR[6:5], MR8, MR13, MR24 Definition

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0			**Single-ended mode**			**RFM support**	**Latency mode**	**REF**
	OP[0] = 1b: Only modified refresh mode supported OP[1] = 0b: Device supports normal latency OP[2] = 0b: Device supports TRR OP[5] = 1b: Device supports single-ended mode							
MR3						**PPRP[3]**		
	OP[2] = 0b: PPR protection disabled (default) 1b: PPR protection enabled							
MR5	**Manufacturer ID**							
	1111 1111b							
MR6	**Revision ID1**							
	1000 0111b							
MR8	**I/O width**		**Density**					
	OP[7:6] = 00b: x16/channel		OP[5:2] = 0100b: 8Gb single-channel die					
MR13						**VRO**		
	OP[2] = 0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6							
MR24	**TRR mode**				**Unlimited MAC**	**MAC value**		
	OP[3:0] = 1000b: Unlimited MAC OP[7] = 0b: Disable (default) 1b: Reserved							
MR25	**PPR resources[4]**							
	Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0
	0b: PPR resource is not available 1b: PPR resource is available							

Table 2 Mode Register Definition

Notes:
1. The contents of Product Specific Mode Register definition will reflect information specific to each die in these packages.
2. Other bits not defined above and other mode registers are referred to Mode Register Assignments and Definitions section.
3. When not using PPR function, PPR protection should be enabled to prevent unintended PPR entry.(MR3 OP[2]=1b).
4. Before using PPR function, confirm the availability of PPR resource by reading MR25.

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2.2 Part Numbering

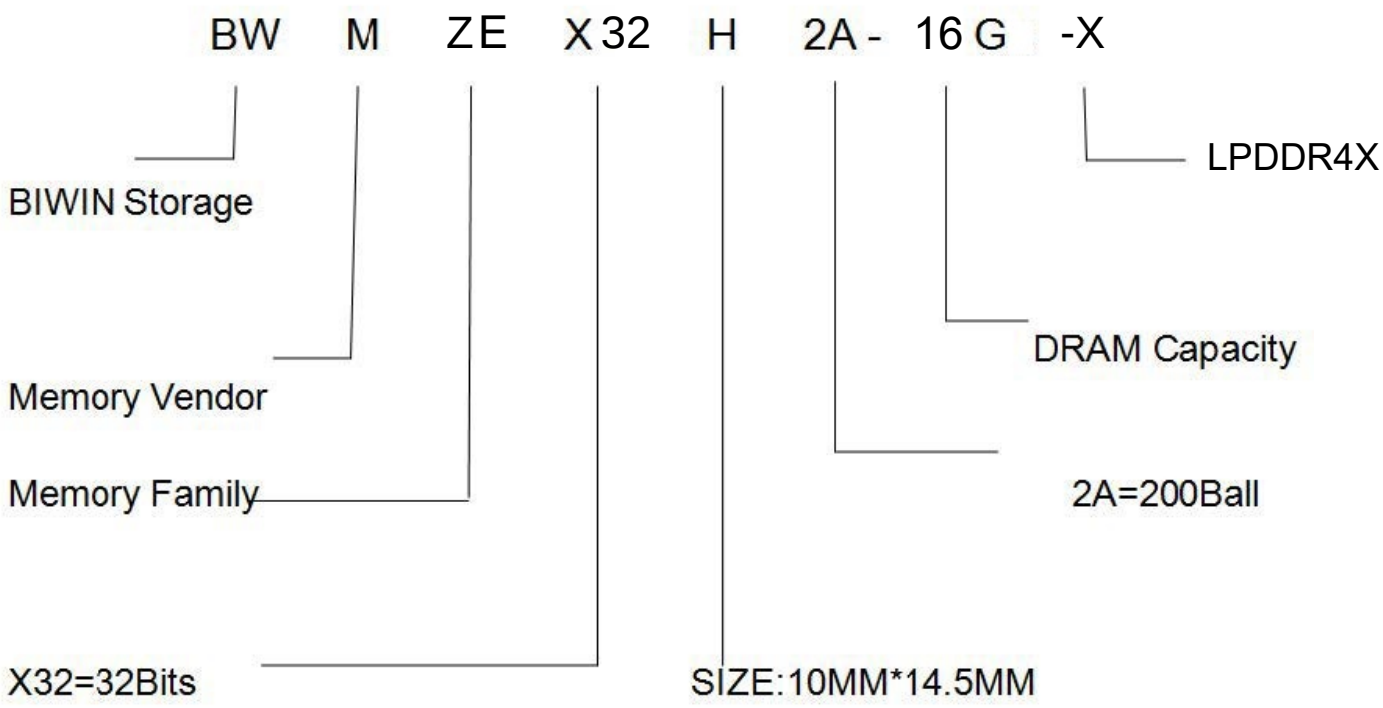


Figure 1 Part Numbering

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2.3 Package Block Diagrams

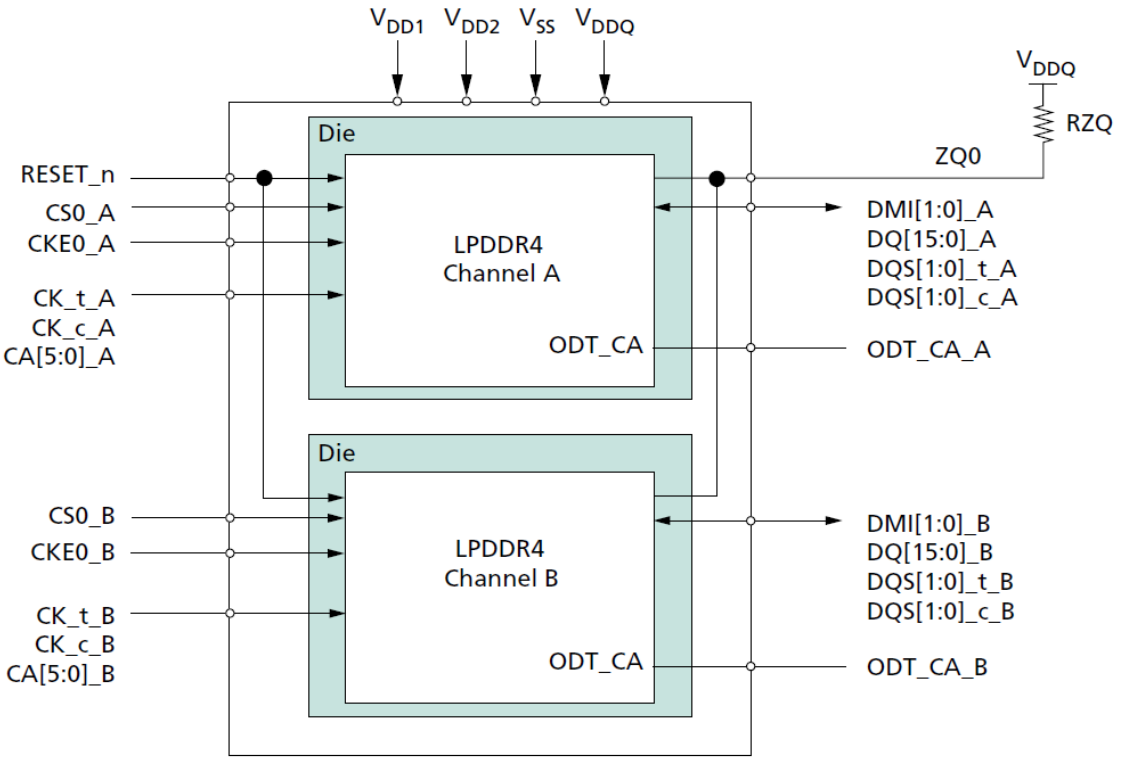
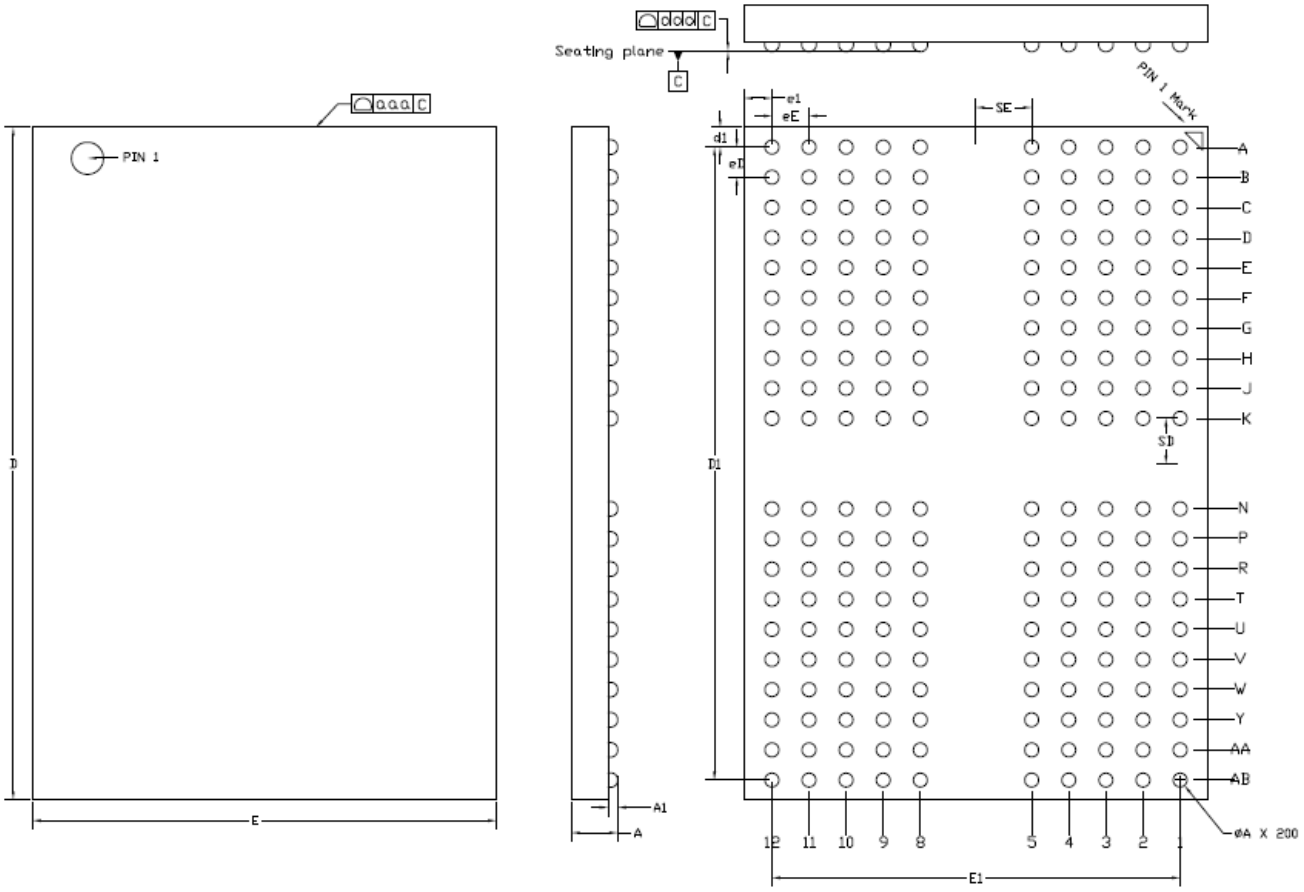


Figure 2 Dual-Die, Dual-Channel Package Block Diagram

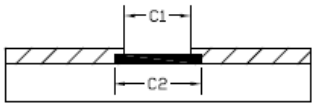
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2.4 Package Dimension



ITEM	Symble	Unit:mm		
		MIN	NORM	MAM
BODY SIZE	D	14.40	14.50	14.60
	E	9.90	10.00	10.10
TOTAL THICNESS	A	0.80	0.90	1.00
STAND OFF	A1	0.18	0.21	0.24
EDGE BALL (CENTER TO CENTER)	D1	13.65		
	E1	8.80		
BALL PITCH	eD	0.65		
	eE	0.80		
even number of balls (eE/2,eD/2) odd number of balls (0)	SE	1.20		
	SD	0.98		
BALL COUNT	n	200		
BALL WIDTH (after reflow)	ΦA	0.29	0.32	0.35
Solder mask opening	C1	0.27	0.30	0.33
Ball pad diameter	C2	0.33	0.36	0.39
BALL TO OUTLINE	d1	0.32	0.42	0.52
	e1	0.50	0.60	0.70
Mold package warpage	aaa	0.08		
COPLANARITY	ddd	0.08		



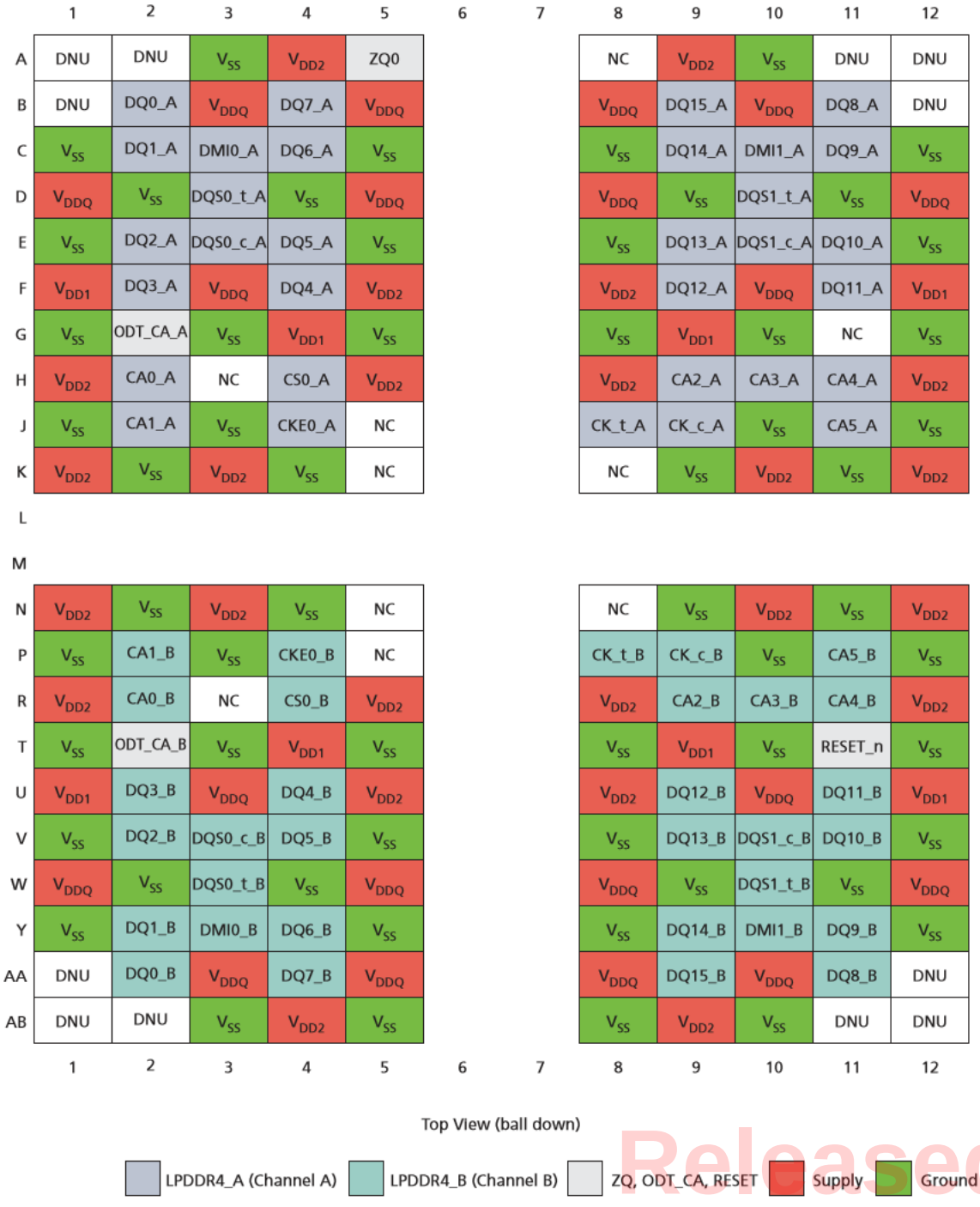
200ball Ø0.3mm Dimensions apply to solder balls postreflow on Ø0.3mm SMD ball pads.

Notice:
1.Ball diameter: 0.3mm
2."◗"---bumping ball location
3.In the diagram,there are 200 ball locations in all.

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Figure 3 Package Dimension (10mm*14.5mm*0.9mm)

2.5 Ball Assignments



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Figure 4 Dual-Channel, Dual-Rank Discrete FBGA

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Symbol	Type	Description
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel has its own clock pair.
CKE0_A, CKE1_A, CKE0_B, CKE1_B	Input	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK.
CS0_A, CS1_A, CS0_B, CS1_B	Input	Chip select: Each channel (A, B) has its own CS signals.
CA[5:0]_A, CA[5:0]_B	Input	Command/address inputs: Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals.
ODT_CA_A, ODT_CA_B	Input	CA ODT Control: The ODT_CA pin is used in conjunction with the mode register to turn on/off the on-die termination for CA pins. It is bonded to VDD2 within the package, or at the package ball, for the terminating rank, and the non-terminating ranks are bonded to VSS (or left floating with a weak pull-down on the DRAM die). The terminating rank is the DRAM that terminates the CA bus for all die on the same channel.
DQ[15:0]_A, DQ[15:0]_B	I/O	Data input/output: Bidirectional data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	Data strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	Data Mask/Data Bus Inversion: DMI is a dual use bi-directional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion (DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own DMI signals.
ZQ0, ZQ1	Reference	ZQ Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240Ω ±1% resistor.
VDDQ, VDD1, VDD2	Supply	Power supplies: Isolated on the die for improved noise immunity.
VSS	Supply	Ground Reference: Power supply ground reference.
RESET_n	Input	RESET: When asserted LOW, the RESET pin resets both channels of the die.
DNU	–	Do not use: Must be grounded or left floating.
NC	–	No connect: Not internally connected.

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Table 3 Ball/Pad Description

Note: ZQ1, CKE1_A, CKE1_B, CS1_A, and CS1_B balls are reserved for 2-rank package. For 1-rank package those balls are NC.

2.6 IDD Parameters–Single Die

VDD2 =1.06–1.17V, VDDQ = 0.57–0.65V or VDDQ = 1.06–1.17V; VDD1 = 1.70–1.95V

Symbol	Supply	Speed Grade	Unit	Note
		3733 Mb/s		
I_{DD01}	V_{DD1}	6.00	mA	
I_{DD02}	V_{DD2}	31.20		
I_{DD0Q}	V_{DDQ}	0.90		
I_{DD2P1}	V_{DD1}	2.88	mA	
I_{DD2P2}	V_{DD2}	4.08		
I_{DD2PQ}	V_{DDQ}	0.90		
I_{DD2PS1}	V_{DD1}	2.88	mA	
I_{DD2PS2}	V_{DD2}	4.08		
I_{DD2PSQ}	V_{DDQ}	0.90		
I_{DD2N1}	V_{DD1}	2.88	mA	
I_{DD2N2}	V_{DD2}	16.80		
I_{DD2NQ}	V_{DDQ}	0.90		
I_{DD2NS1}	V_{DD1}	2.88	mA	
I_{DD2NS2}	V_{DD2}	14.40		
I_{DD2NSQ}	V_{DDQ}	0.90		
I_{DD3P1}	V_{DD1}	2.88	mA	
I_{DD3P2}	V_{DD2}	7.44		
I_{DD3PQ}	V_{DDQ}	0.90		
I_{DD3PS1}	V_{DD1}	2.88	mA	
I_{DD3PS2}	V_{DD2}	7.44		
I_{DD3PSQ}	V_{DDQ}	0.90		
I_{DD3N1}	V_{DD1}	4.08	mA	
I_{DD3N2}	V_{DD2}	19.20		
I_{DD3NQ}	V_{DDQ}	0.90		
I_{DD3NS1}	V_{DD1}	4.08	mA	
I_{DD3NS2}	V_{DD2}	16.80		
I_{DD3NSQ}	V_{DDQ}	0.90		
I_{DD4R1}	V_{DD1}	13.20	mA	2, 3
I_{DD4R2}	V_{DD2}	246.00		
I_{DD4RQ}	V_{DDQ}	63.13		

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Symbol	Supply	Speed Grade	Unit	Note
		3733 Mb/s		
I_{DD4W1}	V_{DD1}	13.20	mA	2
I_{DD4W2}	V_{DD2}	192.00		
I_{DD4WQ}	V_{DDQ}	0.90		
I_{DD51}	V_{DD1}	27.60	mA	
I_{DD52}	V_{DD2}	132.00		
I_{DD5Q}	V_{DDQ}	0.90		
I_{DD5AB1}	V_{DD1}	7.92	mA	
I_{DD5AB2}	V_{DD2}	28.80		
I_{DD5ABQ}	V_{DDQ}	0.90		
I_{DD5PB1}	V_{DD1}	5.76	mA	
I_{DD5PB2}	V_{DD2}	28.80		
I_{DD5PBQ}	V_{DDQ}	0.90		

Table 4 IDD Parameters – Single-Die

Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
2. BL = 16, DBI disabled.
3. I_{DD4RQ} value is reference only. Typical value. $V_{OH} = 0.5 \times V_{DDQ}$; $T_C = 25°C$
4. I_{DD} values reflect dual-channel operation with the same pattern for each channel.

VDD2 =1.06–1.17V, VDDQ = 0.57-0.65V or VDDQ = 1.06–1.17V; VDD1 = 1.70–1.95V

Temperature	Supply	Full-Array Self Refresh Current	Unit
25°C	V_{DD1}	0.62	mA
	V_{DD2}	1.39	
	V_{DDQ}	0.01	
85°C	V_{DD1}	5.16	mA
	V_{DD2}	10.80	
	V_{DDQ}	0.90	

Table 5 IDD6 Full-Array Self Refresh Current

Notes: 1. I_{DD6} 25°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD6} 85°C is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.

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3. AC Timing

Parameter	Symbol	Min/ Max	Data Rate			Unit
			1600	3200	3733	
Average clock period	tCK(AVG)	Min	1250	625	535	ps
		Max	100	100	100	ns
Average HIGH pulse width	tCH(AVG)	Min	0.46			tCK(AVG)
		Max	0.54			
Average LOW pulse width	tCL(AVG)	Min	0.46			tCK(AVG)
		Max	0.54			
Absolute clock period	tCK(ABS)	Min	tCK(AVG)min + tJIT(per)min			ps
Absolute clock HIGH pulse width	tCH(ABS)	Min	0.43			tCK(AVG)
		Max	0.57			
Absolute clock LOW pulse width	tCL(ABS)	Min	0.43			tCK(AVG)
		Max	0.57			
Clock period jitter	tJIT(per)allowed	Min	–70	–40	–34	ps
		Max	70	40	34	
Maximum clock jitter between two consecutive clock cycles (includes clock period jitter)	tJIT(cc)allowed	Max	140	80	68	ps

Table 6 Clock Timing

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Parameter	Symbol	Min/ Max	Data Rate							Unit	Notes
			533	1066	1600	2133	2667	3200	3733		
DQS output access time from CK_t/CK_c	tDQSCK	Min	1500							ps	1
		Max	3500								
DQS output access time from CK_t/CK_c - voltage variation	tDQSCK_VOLT	Max	7							ps/mV	2
DQS output access time from CK_t/CK_c - temperature variation	tDQSCK_TEMP	Max	4							ps/°C	3
CK to DQS rank to rank variation	tDQSCK_rank2rank	Max	1.0							ns	4, 5
DQS_t, DQS_c to DQ skew total, per group, per access (DBI Disabled)	tDQSQ	Max	0.18							UI	6
DQ output hold time total from DQS_t, DQS_c (DBI Disabled)	tQH	Min	MIN(tQSH, tQSL)							ps	6
Data output valid window time total, per pin (DBI-Disabled)	^{t}QW_total	Min	0.75			0.73		0.70		UI	6, 11
DQS_t, DQS_c to DQ skew total, per group, per access (DBI-Enabled)	^{t}DQSQ_DBI	Max	0.18							UI	6
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	^{t}QH_DBI	Min	MIN(^{t}QSH_DBI, ^{t}QSL_DBI)							ps	6
Data output valid window time total, per pin (DBI-Enabled)	^{t}QW_total_DBI	Min	0.75			0.73		0.70		UI	6, 11
DQS_t, DQS_c differential output LOW time (DBI- Disabled)	^{t}QSL	Min	^{t}CL(ABS) – 0.05							tCK(AVG)	9, 11
DQS_t, DQS_c differential output HIGH time (DBI- Disabled)	^{t}QSH	Min	^{t}CH(ABS) – 0.05							tCK(AVG)	10, 11

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DQS_t, DQS_c differential output LOW time (DBI- Enabled)	^{t}QSL-DBI	Min	^{t}CL(ABS) – 0.045	tCK(AVG)	9, 11
DQS_t, DQS_c differential output HIGH time (DBI- Enabled)	^{t}QSH-DBI	Min	^{t}CH(ABS) – 0.045	tCK(AVG)	10, 11
Read preamble	^{t}RPRE	Min	1.8	tCK(AVG)	
Read postamble	^{t}RPST	Min	0.4 (or 1.4 if extra postamble is programmed in MR)	tCK(AVG)	
DQS Low-Z from clock	tLZ(DQS)	Min	(RL × tCK) + tDQSCK(MIN) - (tRPRE(MAX) × tCK) - 200ps	ps	
DQ Low-Z from clock	tLZ(DQ)	Min	(RL × tCK) + tDQSCK(MIN) - 200ps	ps	
DQS High-Z from clock	tHZ(DQS)	Min	(RL × tCK) + tDQSCK(MAX)+(BL/2 × tCK) + (tRPST(MAX) ×tCK) - 100ps	ps	
DQ High-Z from clock	tHZ(DQ)	Min	(RL × tCK) + tDQSCK(MAX) + tDQSQ(MAX) + (BL/2 × tCK) - 100ps	ps	

Table 7 Read Output Timing

Notes: 1. This parameter includes DRAM process, voltage, and temperature variation. It also includes the AC noise impact for frequencies >20 MHz and a max voltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply with the component MIN/MAX DC operating conditions.

2. ^{t}DQSCK_volt max delay variation as a function of DC voltage variation for V_{DDQ} and V_{DD2}. The voltage supply noise must comply with the component MIN/MAX DC operating conditions The voltage variation is defined as the MAX[ABS(^{t}DQSCK(MIN)@V1 - ^{t}DQSCK(MAX)@V2), ABS(^{t}DQSCK(MAX)@V1 - ^{t}DQSCK(MIN)@V2)]/ABS(V1 - V2).
3. ^{t}DQSCK_temp MAX delay variation as a function of temperature.
4. The same voltage and temperature are applied to ^{t}DQSCK_rank2rank.
5. ^{t}DQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design die.
6. DQ-to-DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER.
7. The deterministic component of the total timing.
8. This parameter will be characterized and guaranteed by design.
9. ^{t}QSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from one falling edge to the next consecutive rising edge.
10. ^{t}QSH describes the instantaneous differential output high pulse width on DQS_t -DQS_c, as measured from one falling edge to the next consecutive rising edge.
11. This parameter is a function of input clock jitter. These values assume MIN ^{t}CH(ABS) and CL(ABS). ^{t}When the input clock jitter MIN ^{t}CH(ABS) and ^{t}CL(ABS) is 0.44 or greater than CK(AVG), ^{t}the minimum value of ^{t}QSL will be ^{t}CL(ABS) - 0.04 and ^{t}QSH will be ^{t}CH(ABS) _0.04.

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Parameter	Symbol	Min/ Max	Data Rate							Unit	Notes
			533	1066	1600	2133	2667	3200	3733		
Rx timing window total at V_{dIVW} voltage levels	TdIVW_total	Max	0.22					0.25		UI	1, 2, 3
DQ and DMI input pulse width (at V_{CENT_DQ})	TdIPW	Min	0.45							UI	7
DQ-to-DQS offset	t_{DQS2DQ}	Min	200							ps	6
		Max	800								
DQ-to-DQ offset	t_{DQDQ}	Max	30							ps	7
DQ-to-DQS offset temperature variation	t_{DQS2DQ_temp}	Max	0.6							ps/°C	8
DQ-to-DQS offset voltage variation	t_{DQS2DQ_volt}	Max	33							ps/50mV	9
DQ-to-DQS offset rank to rank variation	$t_{DQS2DQ_rank2rank}$	Max	200							ps	10, 11
WRITE command to first DQS transition	t_{DQSS}	Min	0.75							tCK(AVG)	
		Max	1.25								
DQS input HIGH-level width	t_{DQSH}	Min	0.4							tCK(AVG)	
DQS input LOW-level width	t_{DQSL}	Min	0.4							tCK(AVG)	
DQS falling edge to CK setup time	t_{DSS}	Min	0.2							tCK(AVG)	
DQS falling edge from CK hold time	t_{DSH}	Min	0.2							tCK(AVG)	
Write postamble	t_{WPST}	Min	0.4 (or 1.4 if extra postamble is programmed in MR)							tCK(AVG)	
Write preamble	t_{WPRE}	Min	1.8							tCK(AVG)	

Table 8 Write Timing

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Notes:
1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltage of 45mV peak-to-peak at a fixed temperature on the package. The voltage supply noise must comply to the component MIN/MAX DC operating conditions.
2. Rx differential DQ-to-DQS jitter total timing window at the V_{dIVW} voltage levels.
3. Defined over the DQ internal V_{REF} range. The Rx mask at the pin must be within the internal VREF(DQ) range irrespective of the input signal common mode.
4. Rx mask defined for one pin toggling with other DQ signals in a steady state.
5. DQ-only minimum input pulse width defined at the $V_{CENT_DQ(pin_mid)}$.
6. DQ-to-DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage, and temperature variations.

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7. DQ-to-DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
8. ^{t}DQS2DQ(MAX) delay variation as a function of temperature.
9. ^{t}DQS2DQ(MAX) delay variation as a function of the DC voltage variation for V_{DDQ} and V_{DD2}. It includes the V_{DDQ} and V_{DD2} AC noise impact for frequencies >20 MHz and MAX voltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature on the package.
10. The same voltage and temperature are applied to ^{t}DQS2DQ_rank2rank.
11. ^{t}DQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design die.

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Parameter	Symbol	Min/ Max	Data Rate			Unit	Notes
			1600	3200	3733		
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	Min	MAX(7.5ns, 4*n*CK)			ns	1
Delay from valid command to CKE input LOW	tCMDCKE	Min	MAX(1.75ns, 3*n*CK)			ns	1
Valid clock requirement after CKE input LOW	tCKELCK	Min	MAX(5ns, 5*n*CK)			ns	1
Valid CS requirement before CKE input LOW	tCSCKE	Min	1.75			ns	
Valid CS requirement after CKE input LOW	tCKELCS	Min	MAX(5ns, 5*n*CK)			ns	1
Valid Clock requirement before CKE Input HIGH	tCKCKEH	Min	MAX(1.75ns, 3*n*CK)			ns	1
Exit power-down to next valid command delay	tXP	Min	MAX(7.5ns, 5*n*CK)			ns	1
Valid CS requirement before CKE input HIGH	tCSCKEH	Min	1.75			ns	
Valid CS requirement after CKE input HIGH	tCKEHCS	Min	MAX(7.5ns, 5*n*CK)			ns	1
Valid clock and CS requirement after CKE input LOW after MRW command	tMRWCKEL	Min	MAX(14ns, 10*n*CK)			ns	1
Valid clock and CS requirement after CKE input LOW after ZQCALSTART command	tZQCKE	Min	MAX(1.75ns, 3*n*CK)			ns	1

Table 9 CKE Input Timing

Note:

1. Delay time has to satisfy both analog time(ns) and clock count (nCK). For example, tCMDCKE will not expire until CK has toggled through at least 3 full cycles (3tCK) and 3.75ns has transpired. The case that 3nCK is applied to is shown below.

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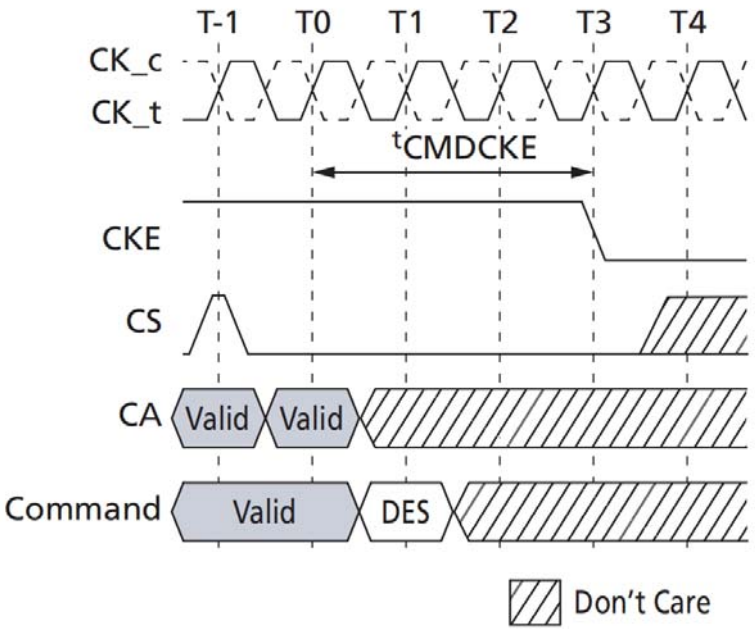


Figure 5 tCMDCKE Timing

Parameter	Symbol	Min/ Max	Data Rate							Unit	Notes
			533	1066	1600	2133	2667	3200	3733		
Command/address valid window (referenced from CA VIL/VIH to CK VIX)	tcIVW	Min	0.3							tCK(AVG)	1, 2, 3
Address and control input pulse width (referenced to VREF)	tcIPW	Min	0.55	0.55	0.55	0.6	0.6	0.6	0.6	tCK(AVG)	4

Table 10 Command Address Input Timing

Notes:

1. CA Rx mask timing parameters at the pin including voltage and temperature drift.
2. Rx differential CA to CK jitter total timing window at the VcIVW voltage levels.
3. Defined over the CA internal VREF range. The Rx mask at the pin must be within the internal VREF(CA) range irrespective of the input signal common mode.
4. CA only minimum input pulse width defined at the VCENT_CA(pin mid).

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Parameter	Symbol	Min/ Max	Value	Unit
Clock cycle time	tCKb	Min	18	ns
		Max	100	
DQS output data access time from CK	tDQSCKb	Min	1.0	ns
		Max	10.0	
DQS edge to output data edge	tDQSQb	Max	1.2	ns

Table 11 Boot Timing Parameters (10–55 MHz)

Parameter	Symbol	Min/ Max	Data Rate			Unit
			1600	3200	3733	
MODE REGISTER WRITE (MRW) command period	tMRW	Min	MAX(10ns, 10nCK)			ns
MODE REGISTER READ (MRR) command period	tMRR	Min	8			tCK(avg)
Additional time after tXP has expired until the MRR command may be issued	tMRRI	Min	tRCD(min) + 3nCK			ns
Delay from MRW command to DQS driven out	tSDO	Max	MAX(12nCK, 20ns)			ns

Table 12 Mode Register Timing Parameters

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Parameter	Symbol	Min/ Max	Data Rate							Unit	Note
			533	1066	1600	2133	2667	3200	3733		
READ latency (DBI disabled)	RL-A	Min	6	10	14	20	24	28	32	tCK(avg)	
READ latency (DBI enabled)	RL-B	Min	6	12	16	22	28	32	36	tCK(avg)	
WRITE latency (Set A)	WL-A	Min	4	6	8	10	12	14	16	tCK(avg)	
WRITE latency (Set B)	WL-B	Min	4	8	12	18	22	26	30	tCK(avg)	
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	Min	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb							ns	
Minimum self refresh time (entry to exit)	tSR	Min	MAX(15ns, 3nCK)							ns	
Self refresh exit to next valid command delay	tXSR	Min	MAX(tRFCab + 7.5ns, 2nCK)							ns	
CAS-to-CAS delay	tCCD	Min	8							tCK(avg)	
CAS-to-CAS delay masked write	tCCDMW	MIN	32							tCK(avg)	
Internal READ-to-PRE-CHARGE command delay	tRTP	Min	MAX(7.5ns, 8nCK)							ns	
RAS-to-CAS delay	tRCD	Min	MAX(18ns, 4nCK)							ns	
Row precharge time (single bank)	tRPpb	Min	MAX(18ns, 3nCK)							ns	
Row precharge time (all banks)	tRPab	Min	MAX(21ns, 3nCK)							ns	
Row active time	tRAS	Min	MAX(42ns, 3nCK)							ns	
		Max	MIN(9 × tREFI × Refresh Rate1, 70.2)							µs	
Write recovery time	tWR	Min	MAX(18ns, 4nCK)							ns	
Write-to-read delay	tWTR	Min	MAX(10ns, 8nCK)							ns	
Active bank A to active bank B	tRRD	Min	MAX(10ns, 4nCK)							ns	1
Precharge-to-precharge delay	tPPD	Min	4							tCK(avg)	2
Four-bank activate window	tFAW	Min	40							ns	1
Delay from SRE command to CKE input LOW	tESCKE	Min	MAX(1.75ns,3nCK)							–	3

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Table 13 Core Timing Parameters

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Notes:

1.Precharge to precharge timing restriction does not apply to AUTO PRECHARGE commands.

2.Delay time has to satisfy both analog time(ns) and clock count (nCK). It means that tESCKE will not expire until CK has toggled through at least three full cycles (3 tCK) and 1.75ns has transpired. The case which 3nCK is applied to is shown below.

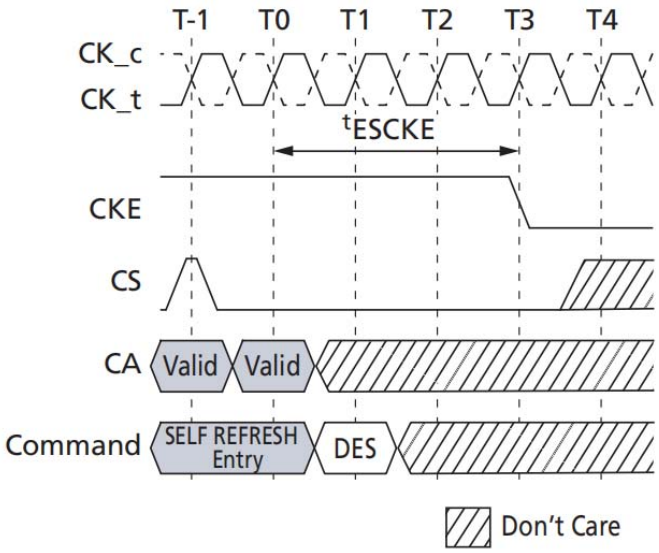


Figure 6 tESCKE Timing

Parameter	Symbol	Min/Max	Data Rate
			533-3733
CA ODT value update time	t_{ODTUP}	Min	RU(20ns/$t_{CK(AVG)}$)

Table 14 CA Bus ODT Timing

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Parameter	Symbol	Min/ Max	Data Rate			Unit	Note
			1600	3200	3733		
Valid clock requirement after CKE input LOW	tCKELCK	Min	MAX(5ns, 5*n*CK)			tCK	
Data setup for V_{REF} training mode	$t_{DStrain}$	Min	2			ns	
Data hold for V_{REF} training mode	$t_{DHtrain}$	Min	2			ns	
Asynchronous data read	tADR	Max	20			ns	
CA BUS TRAINING command-to-command delay	tCACD	Min	RU(t_{ADR}/t_{CK})			tCK	1
Valid strobe requirement before CKE LOW	tDQSCKE	Min	10			ns	
First CA BUS TRAINING command following CKE LOW	tCAENT	Min	250			ns	
V_{REF} step time – multiple steps	tVREFca_LONG	Max	250			ns	
V_{REF} step time – one step	tVREFca_SHORT	Max	80			ns	
Valid clock requirement before CS HIGH	tCKPRECS	Min	2tCK + tXP			–	
Valid clock requirement after CS HIGH	tCKPSTCS	Min	MAX(7.5ns, 5*n*CK)			–	
Minimum delay from CS to DQS toggle in command bus training	tCS_VREF	Min	2			tCK	
Minimum delay from CKE HIGH to strobe High-Z	tCKEHDQS	Min	10			ns	
CA bus training CKE HIGH to DQ tristate	tMRZ	Min	1.5			ns	
ODT turn-on latency from CKE	tCKELODTon	Min	20			ns	
ODT turn-off latency from CKE	tCKEHODToff	Min	20			ns	
Exit command bus training mode to next valid command delay	tXCBT_Short	Min	MAX(200ns, 5*n*CK)			–	2
	tXCBT_Middle	Min	MAX(200ns, 5*n*CK)			–	2
	tXCBT_Long	Min	MAX(250ns, 5*n*CK)			–	2

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Table 15 CA Bus Training Parameters

Notes:

1. If tCACD is violated, the data for samples which violate tCACD will not be available, ex- cept for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.
2. Exit command bus training mode to next valid command delay time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in tFC value mapping table. Additionally exit command bus training mode to next valid command delay time may affect VREF(DQ) setting. Settling time of VREF(DQ) level is same as VREF(CA) level.

Symbol	800–2133 MHz	Unit
$t_{ODTon,min}$	1.5	ns
$t_{ODTon,max}$	3.5	ns
$t_{ODToff,min}$	1.5	ns
$t_{ODToff,max}$	3.5	ns

Table 16 Asynchronous ODT Turn On and Turn Off Timing

Parameter	Symbol	Min/ Max	Data Rate							Unit
			533	1066	1600	2133	2667	3200	3733	
DQS output access time from CK_t/CK_c (derated)	tDQSCKd	Max	3600							ps
RAS-to-CAS delay (derated)	tRCDd	Min	tRCD + 1.875							ns
ACTIVATE-to-ACTIVATE command period (same bank, derated)	tRCd	Min	tRC + 3.75							ns
Row active time (derated)	tRASd	Min	tRAS + 1.875							ns
Row precharge time (derated)	tRPd	Min	tRP + 1.875							ns
Active bank A to active bank B (derated)	tRRD	Min	tRRD + 1.875							ns

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Table 17 Temperature Derating Parameters

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Note: 1. At higher temperatures (>85°C), AC timing derating may be required. If derating is required the device will set MR4 OP[2:0] = 110b.

4. CA Rx Voltage and Timing

The command and address (CA), including CS input receiver compliance mask for voltage and timing, is shown in the CA Receiver (Rx) Mask figure below. All CA and CS signals apply the same compliance mask and operate in single data rate mode.

The CA input Rx mask for voltage and timing is applied across all pins, as shown in the figure below. The Rx mask defines the area that the input signal must not encroach if the DRAM input receiver is expected to successfully capture a valid input signal; it is not the valid data eye.

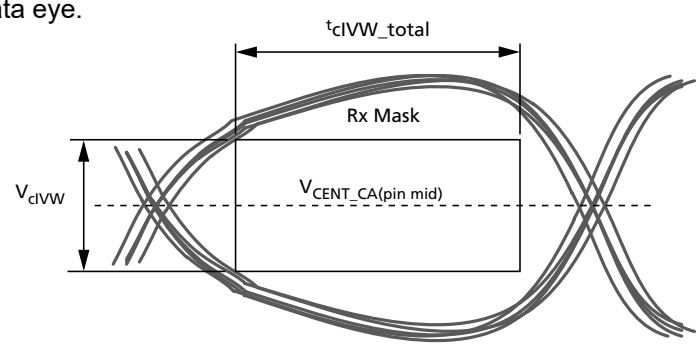


Figure 7 CA Receiver (Rx) Mask

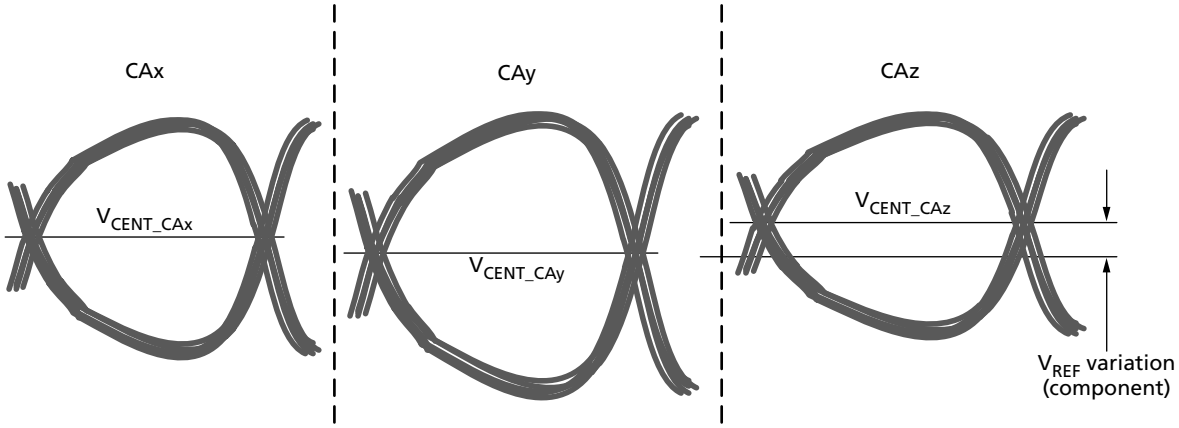
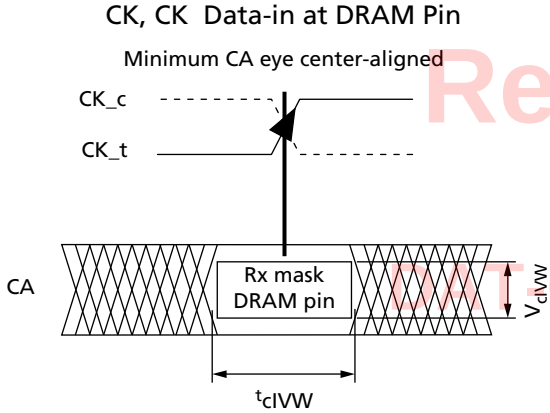


Figure 8 Across Pin $V_{REF\ (CA)}$ Voltage Variation

$V_{CENT_CA(pin\ mid)}$ is defined as the midpoint between the largest V_{CENT_CA} voltage level and the smallest V_{CENT_CA} voltage level across all CA and CS pins for a given DRAM component. Each CA V_{CENT} level is defined by the center, which is, the widest opening of the cumulative data input eye, as depicted in the figure above. This clarifies that any DRAM component level variation must be accounted for within the CA Rx mask. The component-level V_{REF} will be set by the system to account for R_{ON} and ODT settings.



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TcIVW for all CA signals is defined as centered on the CK_t/CK_c crossing at the DRAM pin.

Figure 9 CA Timings at the DRAM Pins

Note:

1. All of the timing terms in above figure are measured from the CK_t/CK_c to the center (midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around VCENT_CA(pin mid).

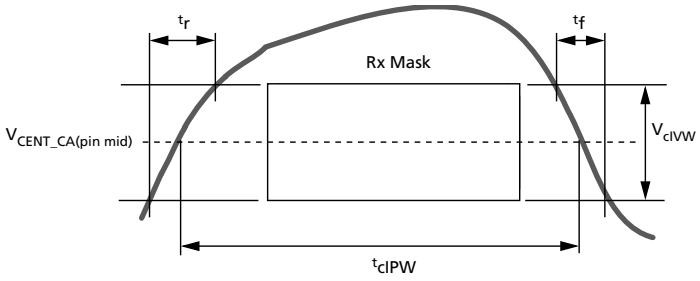


Figure 10 CA tcIPW and SRIN_cIVW Definition (for Each Input Pulse)

Note:

1. SRIN_cIVW = V_{dIVW_total}/(^{t}r or ^{t}f); signal must be monotonic within ^{t}r and ^{t}f range.

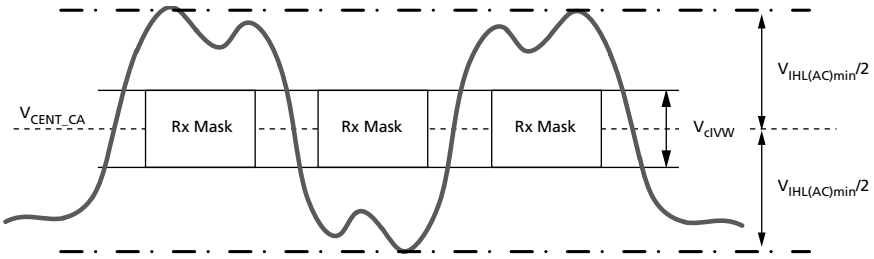


Figure 11 CA V_{IHL_AC}Definition (for Each Input Pulse)

Symbol	Parameter	DQ – 1333[7]		DQ – 1600/1867		DQ – 3200/3733		DQ – 4267		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
V_{cIVW}	Rx mask voltage peak-to-peak	–	175	–	175	–	155	–	145	mV	1, 2, 3
$V_{IHL(AC)}$	CA AC input pulse amplitude peak-to-peak	210	–	210	–	190	–	180	–	mV	4, 6
SRIN_cIVW	Input slew rate over V_{cIVW}	1	7	1	7	1	7	1	7	V/ns	5

Table 18 DRAM CMD/ADR, CS

Notes:

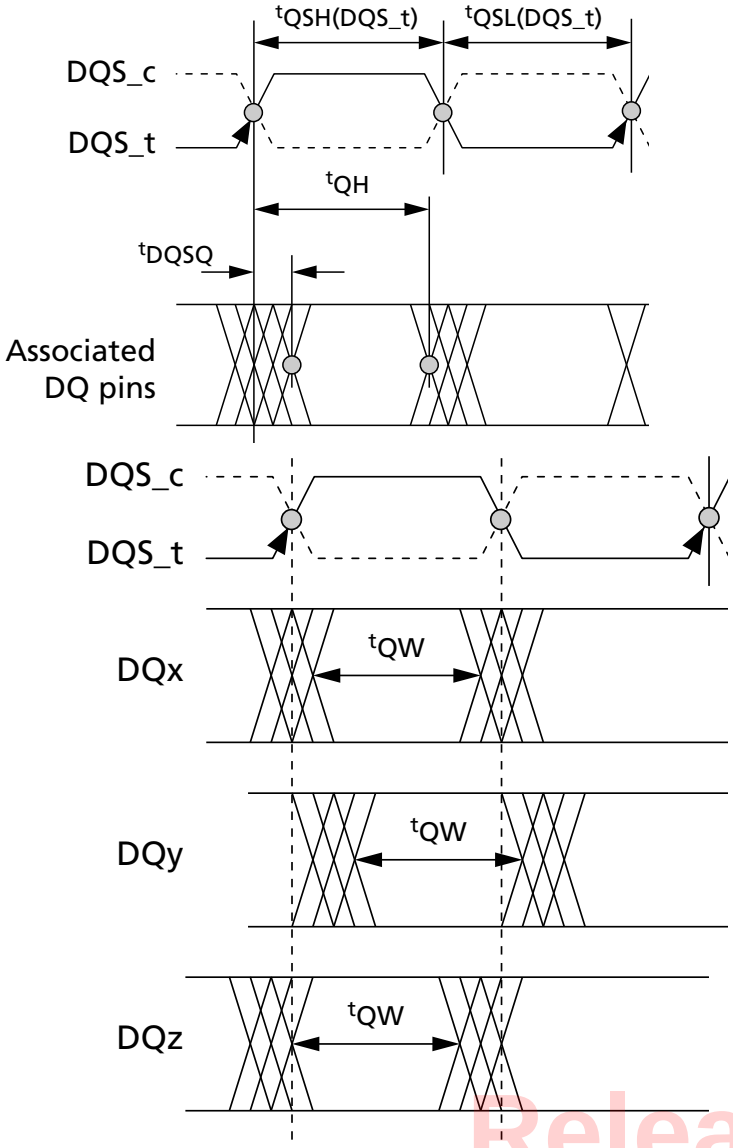
1. CA Rx mask voltage and timing parameters at the pin, including voltage and temperature drift.
2. Rx mask voltage V_{cIVW} total(MAX) must be centered around $V_{CENT_CA(pin\ mid)}$.
3. Defined over the CA internal V_{REF} range. The Rx mask at the pin must be within the internal $V_{REF(CA)}$ range irrespective of the input signal common mode.
4. CA-only input pulse signal amplitude into the receiver must meet or exceed $V_{IHL(AC)}$ at any point over the total UI. No timing requirement above level. $V_{IHL(AC)}$ is the peak-to-peak voltage centered around $V_{CENT_CA(pin\ mid)}$, such that $V_{IHL(AC)}$/2 (MIN) must be met both above and below V_{CENT_CA}.
5. Input slew rate over V_{cIVW} mask is centered at $V_{CENT_CA(pin\ mid)}$.
6. $V_{IHL(AC)}$ does not have to be met when no transitions are occurring.
7. The Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the ^{t}cIVW (ps) = 450ps at or below 1333 operating frequencies.
8. UI = ^{t}CK(AVG)MIN.

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5. DQ Tx Voltage and Timing

The DQ input receiver mask for voltage and timing is applied per pin, as shown in the DQ Receiver (Rx) Mask figure below. The total mask (V_{dIVW_total}, TdIVW_total) defines the area that the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal. The mask is a receiver property, and it is not the valid data eye.

5.1 DRAM Data Timing



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Figure 12 Read Data Timing Definitions – ^{t}QH and ^{t}DQSQ Across DQ Signals per DQS Group

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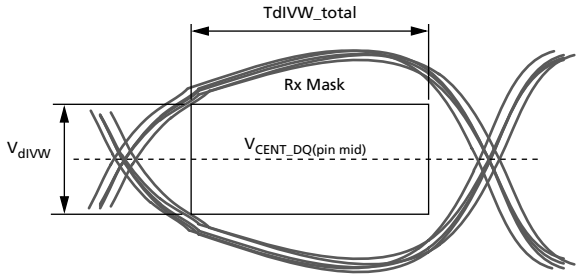


Figure 13 DQ Receiver (Rx) Mask

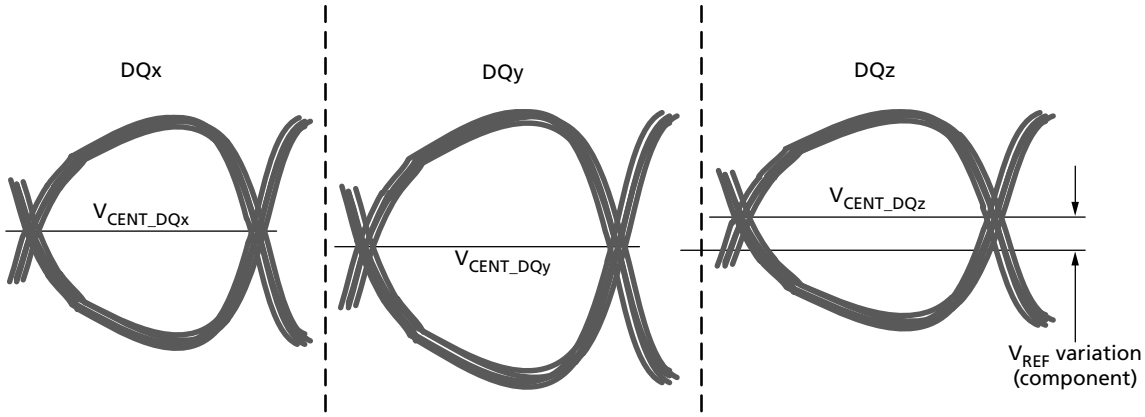


Figure 14 Across Pin V_{REF} DQ Voltage Variation

$V_{CENT_DQ(pin_mid)}$ is defined as the midpoint between the largest V_{CENT_DQ} voltage level and the smallest V_{CENT_DQ} voltage level across all DQ pins for a given DRAM component. Each V_{CENT_DQ} is defined by the center, which is the widest opening of the cumulative data input eye as shown in the figure above. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component-level V_{REF} will be set by the system to account for R_{ON} and ODT settings.

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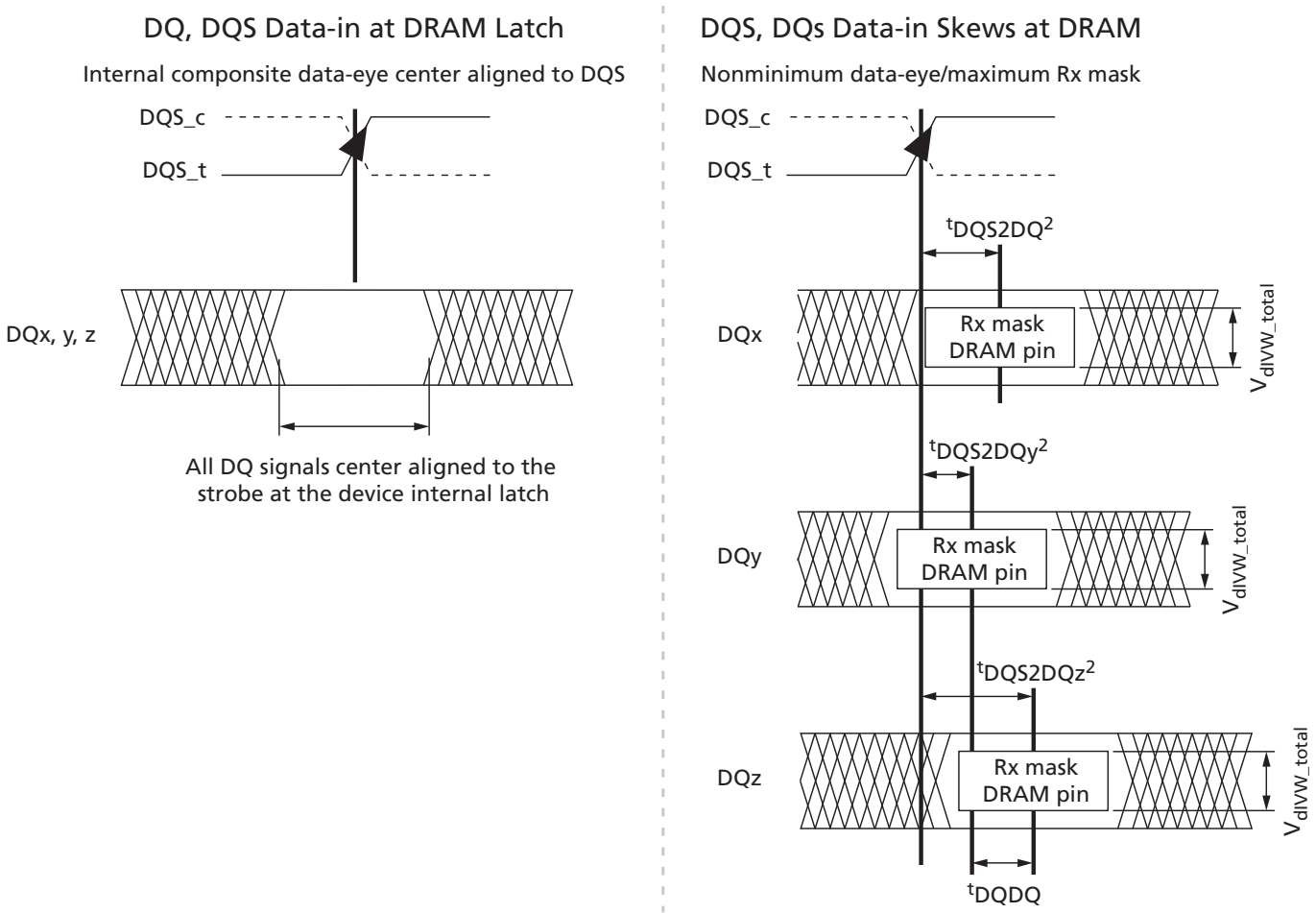


Figure 15 DQ-to-DQS ^{t}DQS2DQ and ^{t}DQDQ

Notes:

1. These timings at the DRAM pins are referenced from the internal latch.
2. tDQS2DQ is measured at the center (midpoint) of the TdIVW window.
3. DQz represents the MAX tDQS2DQ in this example.
4. DQy represents the MIN tDQS2DQ in this example.

All of the timing terms in DQ to DQS_t are measured from the DQS_t/DQS_c to the center (midpoint) of the TdIVW window taken at the V_{dIVW_total} voltage levels centered around $V_{CENT_DQ(pin_mid)}$. In figure above, the timings at the pins are referenced with respect to all DQ signals center-aligned to the DRAM internal latch. The data-to-data offset is defined as the difference between the MIN and MAX ^{t}DQS2DQ for a given component.

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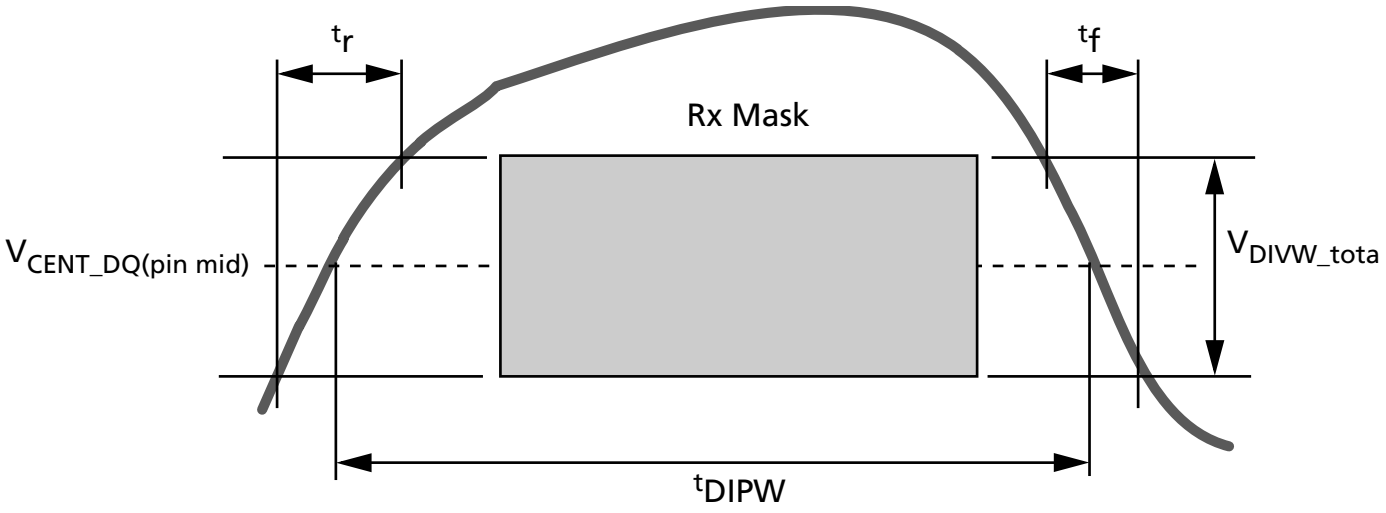
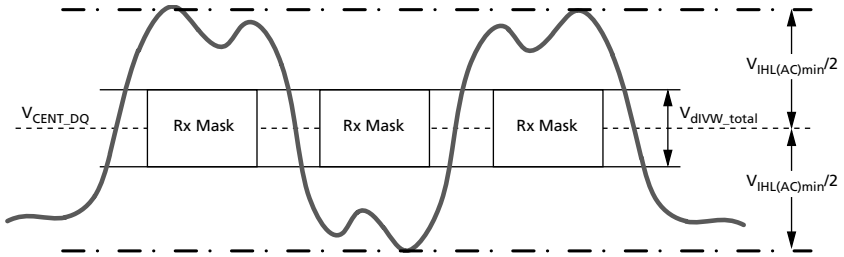


Figure 16 DQ ^{t}DIPW and SRIN_dIVW Definition for Each Input Pulse

$$UI = {}^{t}CK(AVG)\ MIN/2$$

Note:

1. SRIN_dIVW = V_{dIVW_total}/(^{t}r or ^{t}f) signal must be monotonic within ^{t}r and ^{t}f range.



Symbol	Parameter	1600/1867		2133/2400		3200/3733		4267		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
V_{dIVW_total}	Rx mask voltage – peak-to-peak	–	140	–	140	–	140	–	120	mV	1, 2, 3
$V_{IHL(AC)}$	DQ AC input pulse amplitude peak-to-peak	180	–	180	–	180	–	170	–	mV	1, 7
SRIN_dIVW	Input slew rate over V_{dIVW_total}	1	7	1	7	1	7	1	7	V/ns	6

Table 19 DQs In Receive Mode

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Notes:

1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltage of 45mV peak-to-peak at a fixed temperature on the package. The voltage supply noise must comply to the component MIN/MAX DC operating conditions.
2. Rx mask voltage VdIVW_total(MAX) must be centered around VCENT_DQ(pin_mid).
3. Defined over the DQ internal VREF range. The Rx mask at the pin must be within the internal VREF DQ range irre-spective of the input signal common mode.
4. Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design.

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5. DQ-only input pulse amplitude into the receiver must meet or exceed $V_{IHL(AC)}$ at any point over the total UI. No timing requirement above level. $V_{IHL(AC)}$ is the peak-to-peak voltage centered around $V_{CENT_DQ(pin_mid)}$, such that $V_{IHL(AC)}/2$ (MIN) must be met both above and below V_{CENT_DQ}.
6. Input slew rate over V_{dIVW} mask centered at $V_{CENT_DQ(pin_mid)}$.
7. $V_{IHL(AC)}$ does not have to be met when no transitions are occurring.
8. UI = ^{t}CK(AVG)(MIN)/2.

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6. Clock Specification

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction.

Symbol	Description	Calculation	Notes
$^{t}CK(avg)$ and *n*CK	The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge. Unit $^{t}CK(avg)$ represents the actual clock average $^{t}CK(avg)$ of the input clock under operation. Unit *n*CK represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge. $^{t}CK(avg)$ can change no more than ±1% within a 100-clock-cycle window, provided that all jitter and timing specifications are met.	$^{t}CK(avg) = \left(\sum_{j=1}^{N} {}^{t}CK_j\right)/N$ Where $N = 200$	
$^{t}CK(abs)$	The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge.		1
$^{t}CH(avg)$	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	$^{t}CH(avg) = \left(\sum_{j=1}^{N} {}^{t}CH_j\right) / (N \times {}^{t}CK(avg))$ Where $N = 200$	
$^{t}CL(avg)$	The average LOW pulse width, as calculated across any 200 consecutive LOW pulses.	$^{t}CL(avg) = \left(\sum_{j=1}^{N} {}^{t}CL_j\right) / (N \times {}^{t}CK(avg))$ Where $N = 200$	
$^{t}JIT(per)$	The single-period jitter defined as the largest deviation of any signal ^{t}CK from $^{t}CK(avg)$.	$^{t}JIT(per) = \min/\max \text{ of } \left({}^{t}CK_i - {}^{t}CK(avg)\right)$ Where $i = 1$ to 200	1
$^{t}JIT(per),act$	The actual clock jitter for a given system.		
$^{t}JIT(per),allowed$	The specified clock period jitter allowance.		
$^{t}JIT(cc)$	The absolute difference in clock periods between two consecutive clock cycles. $^{t}JIT(cc)$ defines the cycle-to-cycle jitter.	$^{t}JIT(cc) = \max \text{ of } \left({}^{t}CK_{i+1} - {}^{t}CK_i\right)$	1
$^{t}ERR(nper)$	The cumulative error across *n* multiple consecutive cycles from $^{t}CK(avg)$.	$^{t}ERR(nper) = \left(\sum_{j=i}^{i+n-1} {}^{t}CK_j\right) - (n \times {}^{t}CK(avg))$	1
$^{t}ERR(nper),act$	The actual clock jitter over *n* cycles for a given system.		
$^{t}ERR(nper),allowed$	The specified clock jitter allowance over *n* cycles.		
$^{t}ERR(nper),min$	The minimum $^{t}ERR(nper)$.	$^{t}ERR(nper),min = (1 + 0.68LN(n)) \times {}^{t}JIT(per),min$	2
$^{t}ERR(nper),max$	The maximum $^{t}ERR(nper)$.	$^{t}ERR(nper),max = (1 + 0.68LN(n)) \times {}^{t}JIT(per),max$	2
$^{t}JIT(duty)$	Defined with absolute and average specifications for ^{t}CH and ^{t}CL, respectively.	$^{t}JIT(duty),min = MIN((^{t}CH(abs),min - {}^{t}CH(avg),min), (^{t}CL(abs),min - {}^{t}CL(avg),min)) \times {}^{t}CK(avg)$ $^{t}JIT(duty),max = MAX((^{t}CH(abs),max - {}^{t}CH(avg),max), (^{t}CL(abs),max - {}^{t}CL(avg),max)) \times {}^{t}CK(avg)$	

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Table 20 Definitions and Calculations

Notes:

1. Not subject to production testing.
2. Using these equations, tERR(nper) tables can be generated for each tJIT(per),act value.

6.1 tCK(abs), tCH(abs), and tCL(abs)

These parameters are specified with their average values; however, the relationship between the average timing and the absolute instantaneous timing (defined in the following table) is applicable at all times.

Parameter	Symbol	Minimum	Unit
Absolute clock period	^{t}CK(abs)	^{t}CK(avg),min + ^{t}JIT(per),min	ps[1]
Absolute clock HIGH pulse width	^{t}CH(abs)	^{t}CH(avg),min + ^{t}JIT(duty),min^{2}/^{t}CK(avg),min	^{t}CK(avg)
Absolute clock LOW pulse width	^{t}CL(abs)	^{t}CL(avg),min + ^{t}JIT(duty),min^{2}/^{t}CK(avg),min	^{t}CK(avg)

Table 21 ^{t}CK(abs), ^{t}CH(abs), and ^{t}CL(abs) Definitions

Notes:

1. ^{t}CK(avg),min is expressed in ps for this table.
2. tJIT(duty),min is a negative value.

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7. Clock Period Jitter

LPDDR4 devices can tolerate some clock period jitter without core timing parameter derating. This section describes device timing requirements with clock period jitter (^{t}JIT(per)) in excess of the values found in the AC Timing table. Calculating cycle time derating and clock cycle derating are also described.

7.1 Clock Period Jitter Effects on Core Timing Parameters

Core timing parameters (^{t}RCD, ^{t}RP, ^{t}RTP, ^{t}WR, ^{t}WRA, ^{t}WTR, ^{t}RC, ^{t}RAS, ^{t}RRD, ^{t}FAW) extend across multiple clock cycles. Clock period jitter impacts these parameters when measured in numbers of clock cycles. Within the specification limits, the device is characterized and verified to support ^{t}nPARAM = RU[^{t}PARAM/^{t}CK(avg)]. During device operation where clock jitter is outside specification limits, the number of clocks, or ^{t}CK(avg), may need to be increased based on the values for each core timing parameter.

7.2 Cycle Time Derating for Core Timing Parameters

For a given number of clocks (^{t}nPARAM), when ^{t}CK(avg) and ^{t}ERR(^{t}nPARAM),act exceed ^{t}ERR(^{t}nPARAM),allowed, cycle time derating may be required for core timing parameters.

$$\text{CycleTimeDerating} = \max\left\{\left(\frac{^{t}\text{PARAM} + {}^{t}\text{ERR}(^{t}\text{nPARAM}),\text{act} - {}^{t}\text{ERR}(^{t}\text{nPARAM}),\text{allowed}}{^{t}\text{nPARAM}} - {}^{t}\text{CK(avg)}\right), 0\right\}$$

Cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time deratings determined for each individual core timing parameter.

7.3 Clock Cycle Derating for Core Timing Parameters

For each core timing parameter and a given number of clocks (^{t}nPARAM), clock cycle derating should be specified with ^{t}JIT(per).

For a given number of clocks (^{t}nPARAM), when ^{t}CK(avg) plus (^{t}ERR(^{t}nPARAM),act) exceed the supported cumulative ^{t}ERR(^{t}nPARAM),allowed, derating is required. If the equation below results in a positive value for a core timing parameter (^{t}CORE), the required clock cycle derating will be that posi-tive value (in clocks).

$$\text{ClockCycleDerating} = \text{RU}\left\{\frac{^{t}\text{PARAM} + {}^{t}\text{ERR}(^{t}\text{nPARAM}),\text{act} - {}^{t}\text{ERR}(^{t}\text{nPARAM}),\text{allowed}}{\text{CK(avg)}\ ^{t}}\right\} - {}^{t}\text{nPARAM}$$

Cycle-time derating analysis should be conducted for each core timing parameter.

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7.4 Clock Jitter Effects on Command/Address Timing Parameters

Command/address timing parameters (t_{IS}, t_{IH}, t_{ISb}, t_{IHb}) are measured from a command/address signal (CS or CA[5:0]) transition edge to its respective clock signal (CK_t/CK_c) crossing. The specification values are not affected by the $t_{JIT(per)}$ applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

7.5 Clock Jitter Effects on READ Timing Parameters

t_{RPRE}

When the device is operated with input clock jitter, t_{RPRE} must be derated by the $t_{JIT(per),act,max}$ of the input clock that exceeds $t_{JIT(per),allowed,max}$. Output deratings are relative to the input clock:

$$t_{RPRE(min,derated)} = 0.9 - \left(\frac{t_{JIT(per),act,max} - t_{JIT(per),allowed,max}}{t_{CK(avg)}}\right)$$

For example, if the measured jitter into a LPDDR4 device has $t_{CK(avg)}$ = 625ps, $t_{JIT(per),act,min}$ = –xx, and $t_{JIT(per),act,max}$ = +xx ps, then $t_{RPRE,min,derated}$ = 0.9 - ($t_{JIT(per),act,max}$ - $t_{JIT(per),allowed,max}$)/$t_{CK(avg)}$ = 0.9 - (xx - xx)/xx = yy $t_{CK(avg)}$.

$t_{LZ(DQ)}$,$t_{HZ(DQ)}$,t_{DQSCK},$t_{LZ(DQS)}$,$t_{HZ(DQS)}$

These parameters are measured from a specific clock edge to a data signal transition (DM*n* or DQ*m*, where:*n*= 0,1; and*m*= 0–15, and specified timings must be met with respect to that clock edge. Therefore, they are not affected by $t_{JIT(per)}$.

t_{QSH},t_{QSL}

These parameters are affected by duty cycle jitter, represented by $t_{CH(abs)min}$ and $t_{CL(abs)min}$. These parameters determine the absolute data-valid window at the device pin. The absolute minimum data-valid window at the device pin = MIN {($t_{QSH(abs)min}$ - $t_{DQSQmax}$), ($t_{QSL(abs)min}$ - $t_{DQSQmax}$)}. This minimum data valid window must be met at the target frequency regardless of clock jitter.

t_{RPST}

t_{RPST} is affected by duty cycle jitter, represented by $t_{CL(abs)}$. Therefore, $t_{RPST(abs)min}$ can be specified by $t_{CL(abs)min}$. $t_{RPST(abs)min}$ = $t_{CL(abs)min}$ - 0.05 = $t_{QSL(abs)min}$.

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7.6 Clock Jitter Effects on WRITE Timing Parameters

t_{DS},t_{DH}

These parameters are measured from a data signal (DMI*n* or DQ*m*, where *n*= 0, 1 and *m*= 0–15) transition edge to its respective data strobe signal (DQSn_t, DQSn_c: *n* = 0,1) crossing. The specification values are not affected by the amount of $t_{JIT(per)}$ applied, because the setup and hold times are relative to the data strobe signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

t_{DSS},t_{DSH}

These parameters are measured from a data signal (DQS_t, DQSn_c) crossing to its respective clock signal (CK_t, CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT(per)act}$ of the input clock in excess of the allowed period jitter $t_{JIT(per)allowed}$.

t_{DQSS}

t_{DQSS} is measured from a data strobe signal (DQSn_t, DQSn_c) crossing to its respective clock signal (CK_t, CK_c) crossing. When the device is operated with input clock jitter, this parameter must be derated by the actual $t_{JIT(per),act}$ of the input clock in excess of $t_{JIT(per)allowed}$.

$$t_{DQSS(min,derated)} = 0.75 - \left(\frac{t_{JIT(per),act,min} - t_{JIT(per),allowed,}}{t_{CK(avg)}} \right) min$$

$$t_{DQSS(max,derated)} = 1.25 - \left(\frac{t_{JIT(per),act,max} -}{t_{CK(avg)}} \right)$$
$$t_{JIT(per),allowed,\ max}$$

For example, if the measured jitter into an LPDDR4 device has tCK(avg) = 625ps, tJIT(per),act,min = -xxps, and tJIT(per),act,max = +xx ps, then:

$t_{DQSS,(min,derated)}$ = 0.75 - (-xx + yy)/625 = xxxx $t_{CK(avg)}$

$t_{DQSS,(max,derated)}$ = 1.25 - (xx – yy)/625 = xxxx $t_{CK(avg)}$

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