BIWIN qNAND Datasheet

eMMC5.0

TLC 3D NAND

Ver.2.0

Aug. 2020

深圳佰维存储科技股份有限公司

BIWIN STORAGE TECHNOLOGY CO.,LTD.

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Revision History

Version	Date	Description
1.0	Jul. 2019	First Release
2.0	Aug. 2020	Update the Performance

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1. Introduction

1.1 Overview

BIWIN qNAND is an embedded flash storage designed in the form of LFBGA package, using MMC protocol V5.0 interface. It combines advanced NAND flash and intelligent flash controller in single package, offering excellent performance and high reliability storage solution to embedded applications.

With industry standard eMMC5.0 protocol, BIWIN qNAND is empowered with many new features such as Discard, Boot partitions, Secure Erase, and Trim, which are optimal for code reliability and data storage.

qNAND has an intelligent controller to manage interface protocols, data storage and retrieval, error detect and correction(ECC) algorithms, defect handling and diagnostics, and power management. The firmware inside has functions of Wear Leveling Management, Garbage Collection, and Bad Block Management.

qNAND also has features as small size, low power consumption, non-volatile, wild range of operation temperature, high reliability, which makes qNAND the ideal solution for industry PC, vehicle electronic device.

1.2 Product Information:

qNAND Part ID	Capacity	Size	Package
BWCTAK411G32G	32GB	11.5*13*0.9mm	LFBGA153

1.3 Features

- Complies with the eMMC standard JESD84-B50
- 12 signal interface (including CMD, CLK, DS, DAT[7:0], and RST_n)
- Programmable bus width: 1-bit, 4-bit, and 8-bit
- Support wide range of power supply voltage: 1.2V, 1.8V and 3.3V

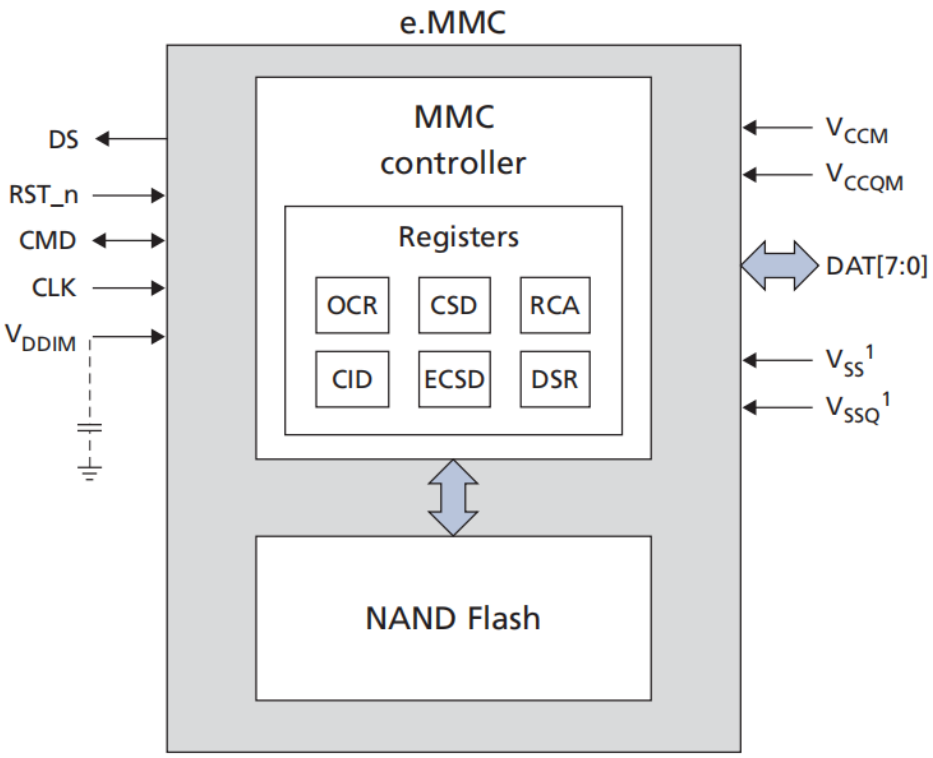
- Support normal speed SDR mode and high speed DDR mode
- HS400 and HS200 mode support
- Up to 200MHz clock speed
- MMC Mode Command Class
- Class 0 (basic), Class 2 (block read), Class 4 (block write), Class 5 (erase), Class 6 (write protection), Class 7 (lock/unlock)
- High-speed, Dual Data Rate Boot support
- Supports Boot and Alternative Boot Mode
- Replay Protected Memory Block (RPMB)
- Secure Erase, Secure Trim, and Trim
- Enhanced Partition Attributes
- High Priority Interrupt (HPI)
- Background Operations
- Enhanced Reliable Write
- 32-bit RISC based architecture with advanced mapping technology
- Optimized algorithm for embedded system access
- Dynamic power management technology
- Quick standby, auto-suspend, and sleep operations
- Standby current: <100uA@25°C
- Dimensions& Package:
  - 11.5mm x 13mm x 0.9mm LFBGA153ball
- Capacities: 32GB

- High data transfer speed
- Up to 104MB/s transfer rate(52MHz, DDR mode)
- Up to 400MB/s transfer rate(200MHz, HS400 mode)
- Operating temperature range -20°C----- 85°C
- Storage temperature range -50°C----- 95°C
- Soldering Temperature (10s) 260°C

1.4 Performance

Capacity	Typical Sequential Read (MB/s)	Typical Sequential Write(MB/s)
32GB	130MB/s	70MB/s

1.5 Functional Block Diagram



Note: 1. VSS and VSSQ are internally connected.

Figure.1 qNAND Functional Block Diagram

1.6 Function Description

Biwin qNAND contains an intelligent eMMC Flash controller with JEDEC eMMC V5.0 interface, which achieves high data transfer rate and provides many new features. The feature was not founded in the other types of storage device:

- Support Multiple User Data Partition with Enhanced User Data Area options
- Signed access to a replay Protected Memory Block
- Support dual data rate transfer
- High speed boot
- Enhanced Write Protection with Permanent and Partial protection options
- Support hardware reset signal
- Optional high priority interrupt mechanism

1.7 Independent Technology

The eMMC V5.0 interface defines the communication protocol between host and eMMC device. It can not only manage wear leveling, bad block management and ECC, but also isolate host from advancing Nand flash technology. Nand flash memory, as main part of eMMC devices, is always rapidly changed to keep close tabs on generation shift. Thanks to this eMMC interface, the host can be independent of Nand flash change, which greatly accelerates product development and reduces time-to-market.

1.8 Error Detect and Management

Biwin qNAND incorporates advanced technology for error detect and management. If a defective block is identified, qNAND can completely replace the defective block with one of the spare blocks. This process is invisible to the host and generally does not affect data space allocated for the user.

2. Package Dimensions

2.1 Physical Specifications

2.1.1 11.5mm*13mm*0.9mm Package Dimension

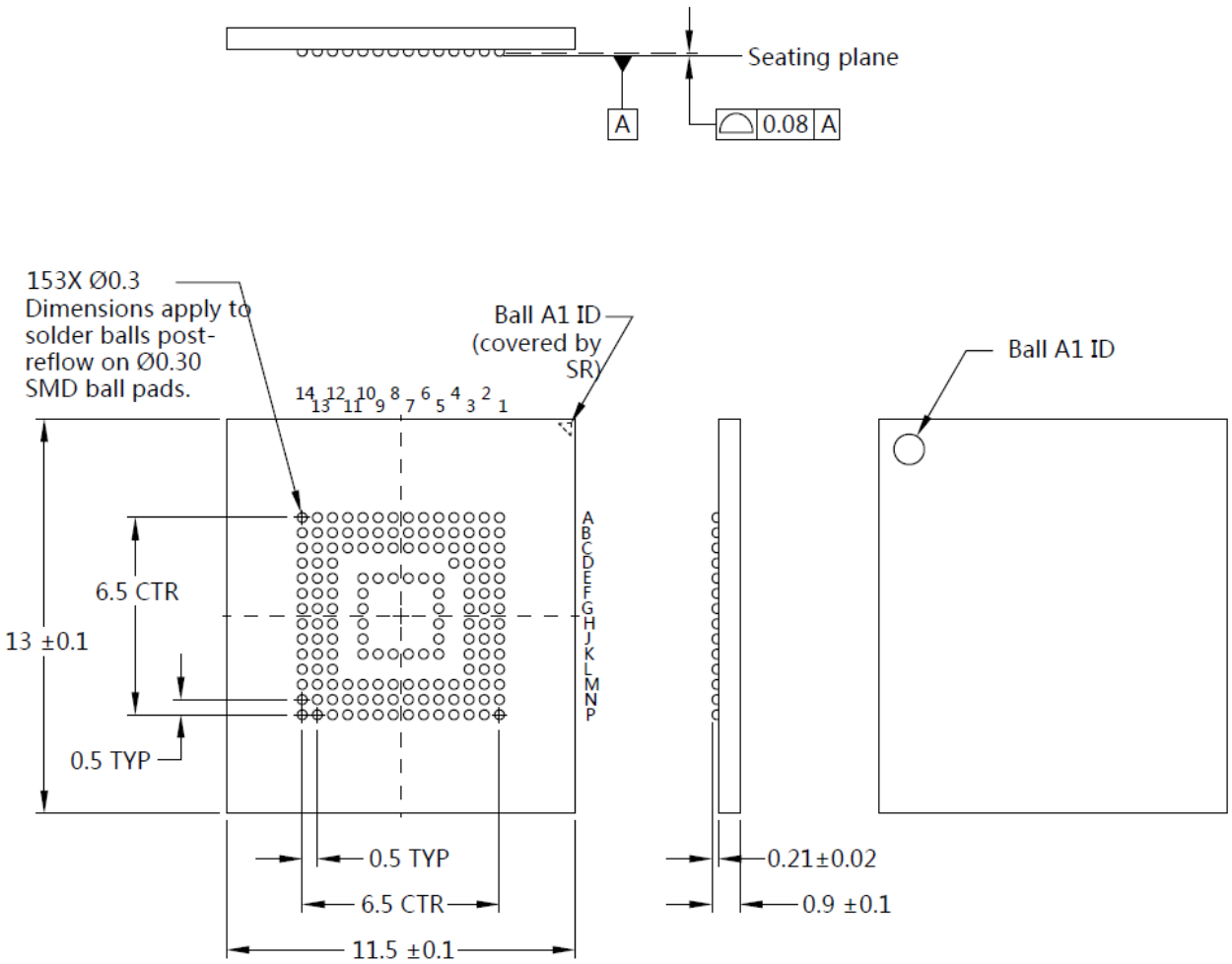


Figure.2 11.5mm * 13mm * 0.9mm Package Dimension

2.1.2 153 Ball Pin Configuration

TFBGA153 Pin Out

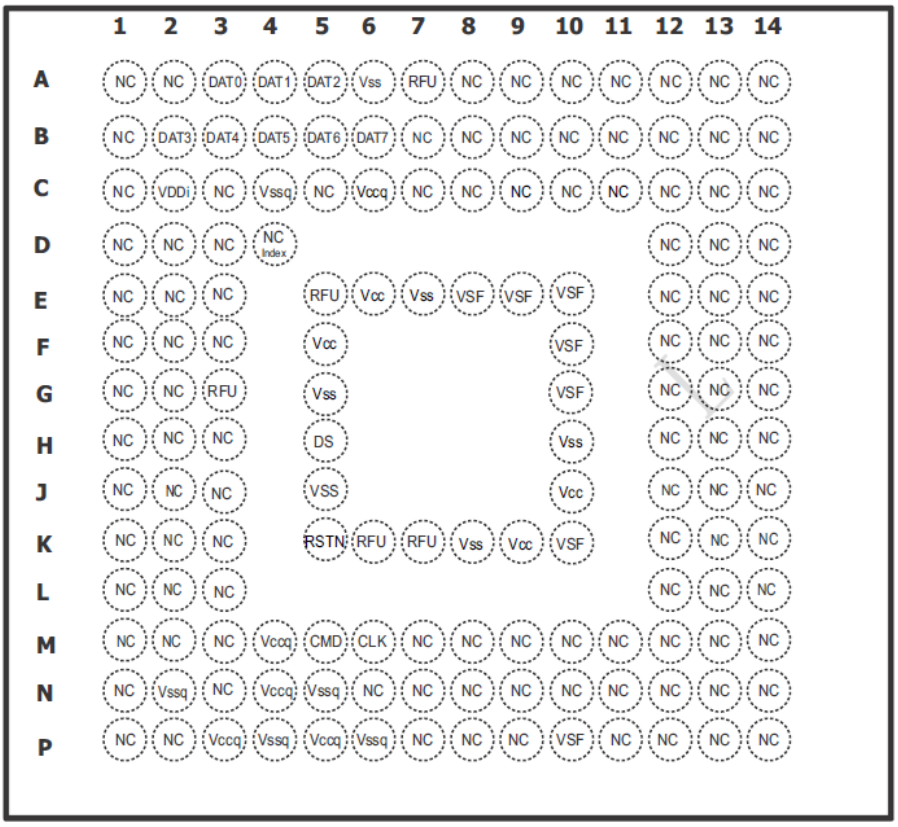


Figure.3 BGA153 Pin Out

Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name
A3	DAT0	**C4**	Vssq	**G10**	VSF	**M5**	CMD
A4	DAT1	**C6**	Vccq	**H5**	DS	**M6**	CLK
A5	DAT2	**E6**	Vcc	**H10**	Vss	**N2**	Vssq
A6	Vss	**E7**	Vss	**J5**	VSS	**N4**	Vccq
B2	DAT3	**E8**	VSF	**J10**	Vcc	**N5**	Vssq
B3	DAT4	**E9**	VSF	**K5**	RSTN	**P3**	Vccq
B4	DAT5	**E10**	VSF	**K8**	Vss	**P4**	Vssq
B5	DAT6	**F5**	Vcc	**K9**	Vcc	**P5**	Vccq
B6	DAT7	**F10**	VSF	**K10**	VSF	**P6**	Vssq
C2	VDDi	**G5**	Vss	**M4**	Vccq	**P10**	VSF

3. qNAND Registers

Within the qNAND interface six registers are defined: OCR, CID, CSD, EXT_CSD, RCA and DSR.

These registers can only be accessed by corresponding commands. The OCR, CID and CSD registers carry the qNAND specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters. The EXT_CSD register carries both qNAND specific information and actual configuration parameters.

3.1 OCR Register

The 32-bit operation conditions register stores the VCCQ voltage profile of the qNAND. In addition, the register contains a status information bit. This status bit is set if the qNAND power up procedure has been finished. The OCR register shall be implemented by qNAND.

OCR bit	Description	q-NAND
[6:0]	Reserved	000 0000b
[7]	1.7-1.95	1b
[14:8]	2.0-2.6	000 0000b
[23:15]	2.7-3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	00b (byte mode)
		10b (sector mode)
[31]	q-NAND power up status bit(busy)[1]	

Table.1 OCR Register Value

This bit is set to low if the qNAND has not finished the power up routine.

3.2 CID Register

Name	Field	Width	CID-slice	CID Value	COMMENT
Manufacturer ID	MID	**8**	[127:120]	0XF4	BIWIN Manufacture ID
Reserved		**6**	[119:114]	-	

Device/BGA	CBX	**2**	[113:112]	0X01	
OEM/Application ID	OID	**8**	[111:104]	0X22	
Product name	PNM	**48**	[103:56]	426977696E20h	
Product revision	PRV	**8**	[55:48]	0X10	
Product serial number	PSN	**32**	[47:16]	random number	
Manufacturing date	MDT	**8**	[15:8]	Year Month	Biwin
CRC7 checksum	CRC	**7**	[7:1]	a	
not used, always '1'	-	**1**	[0:0]	**1**	

Table.2 CID Register Value

3.3 CSD Register

The Device-Specific Data register provides information on how to access time, data transfer speed, and whether the DSR register can be used, etc. The programmable part of the register can be changed by CMD27. The type of the entries in Table 6 below is coded as follows:

- R: Read only.
- W: One time programmable and not readable.
- R/W: One time programmable and readable.
- W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
- R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
- R/W/C_P: Writable after value cleared by power failure and H/W reset assertion (the value not cleared by CMD0 reset) and readable.
- R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
- W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

Name	Field	Width	Type	CSD Slice	CSD Value	Note
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h	
System specification version	SPEC_VERS	4	R	[125:122]	4h	
Reserved	-	2	R	[121:120]	-	
Data read access-time-1	TAAC	8	R	[119:112]	27h	
Data read access-time-2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	1h	
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	32h	
Device Command classes	CCC	12	R	[95:84]	0F5h	
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h	
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h	
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h	
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]		
DSR implemented	DSR_IMP	1	R	[76:76]	0h	
Reserved	-	2	R	[75:74]	-	
Device size	C_SIZE	12	R	[73:62]	FFFH	
Max.read current @VDD min	VDD_R_CURR_MIN	3	R	[61:59]	7h	
Max.read current @VDD max	VDD_R_CURR_MAX	3	R	[58:56]	7h	
Max.write current @VDD min	VDD_W_CURR_MIN	3	R	[55:53]	7h	
Max.write current @VDD max	VDD_W_CURR_MAX	3	R	[52:50]	7h	
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h	
Erase group size	ERASE_GRP_EN	5	R	[46:42]	1Fh	
Erase group size multiplier	ERASE _GRP_MULT	5	R	[41:37]	1Fh	
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0Fh	
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h	
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h	
Write speed factor	R2W_FACTOR	3	R	[28:26]	2h	
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h	
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h	
Reserved	-	1	-	[20:20]	-	
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h	

File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h	
Copy flag(OTP)	COPY	1	R/W	[14:14]	0h	
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h	
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h	
File format	FILE_FORMAT	2	R/W	[11:10]	0h	
ECC code	ECC	2	R/W/E	[9:8]	0h	
CRC	CRC	7	R/W/E	[7:1]	TBD	
Not used, always' 1'	-	1	-	[0:0]	TBD	

Table.3 CSD Register Value

3.4 Extended CSD Register

The Extended CSD register defines the qNAND properties and selected modes. It is 512 bytes long.

The most significant 320 bytes are the Properties segment, which defines the qNAND capabilities and cannot be modified by the host. The lower 192 bytes are the modes segment, which defines the configuration the qNAND is working in. These modes can be changed by the host by means of the SWITCH command.

- R: Read only.
- W: One time programmable and not readable.
- R/W: One time programmable and readable.
- W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
- R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
- R/W/C_P: Writable after value cleared by power failure and H/W rest assertion (the value not cleared by CMD0 reset) and readable.
- R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
- W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

Name	Field	Byte	Type	Slice	Value	Note
Reserved	-	6	-	[511:506]	-	
Extended Security Commands Error	EXT_SECURITY_ ERR	1	R	[505]	0h	
Supported command sets	S_CMD_SET	1	R	[504]	1h	Standard MMC
HPI features	HPI_FEATURES	1	R	[503]	1h	HPI supported with CMD13
Background operations support	BKOPS_SUPPORT	1	R	[502]	1h	BKOPS supported
Max packed read commands	MAX_PACKED_READS	1	R	[501]	3Fh	Max. 63 commands in a packed command
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	3Fh	Max. 63 commands in a packed command
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	1h	support Data tag
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	0h	
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	06h	
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	78h	Max Tag Size = 8*2 = 16MB; Max_ Context ID = 8
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	1h	1MB*2=2MB
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	3h	Support "System code"; Support "Non-persistent"
Support modes	SUPPORT_MODES	1	R	[493]	1h	FFU is Supported
FFU features	FFU_FEATURES	1	R	[492]	0h	
Operation code time out	OPERATION_CODE_TIMEOUT	1	R	[491]	17h	(2^23)*100us=838.86s
FFU Argument	FFU_ARG	4	R	[490:487]	FFFAFFF0h	
Barrier support	BARRIER_SUPPORT	1	R	[486]	1h	Support barrier
Reserved	-	177	-	[485:309]	-	
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	1h	Support CMQD
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	1Fh	32 CMDQ_DEPTH
Reserved	-	1	-	[306]		
Number of FW sectors correctly	NUMBER_OF_FW_SECTORS_CORRECTLY_PR	4	R	[305:302]	0000h	

programmed	OGRAMMED					
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	TBD	
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYPE_B	1	R	[269]	1h	
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYPE_A	1	R	[268]	1h	
Pre EOL information	PRO_EOL_INFO	1	R	[267]	1h	
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	40h	
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	40h	
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	7h	
Device version	DEVICE_VERSION	2	R	[263:262]	TBD	SDP:385h DDP:415h QDP:425h ODP:435h
Firmware version	FIREWARE_ VERSION	8	R	[261:254]	TBD	Fill PRV value as FW version
Power class for 200MHz,DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	R	[253]	0h	
Cache size	CACHE_SIZE	4	R	[252:249]	0400h	128KB (depending on 16KB*CE)
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	5h	5x10ms= 50ms
Power off notification (long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	64h	100x10ms = 1000ms
Background operations status	BKOPS_STATUS	1	R	[246]	0h	No operations required
Number of Correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0h	Run Time update
First initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0Ah	Initial time out 1s
Cache flushing policy	CACHE_FLUSH_POLICY	1	R	[240]	1h	Support cache flushing policy
Power class for 52MHz,DDR at Vcc=3.6V	PWR_CL_DDR_52_360	1	R	[239]	0h	RMS 100mA PEAK 200mA

Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0h	RMS 65mA, PEAK 130mA
Power class for 200MHz at Vccq=1.95V,Vcc=3.6V	PWR_CL_200_195	1	R	[237]	0h	
Power class for 200MHz at Vccq=1.3V, Vcc=3.6V	PWR_CL_200_130	1	R	[236]	0h	
Minimum write performance for 8 bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0h	For devices not reaching the 4.8MB/s value
Minimum read performance for 8 bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0h	For devices not reaching the 4.8MB/s value
Reserved	-	1	-	[233]	-	
TRIM multiplier	TRIM_MULT	1	R	[232]	02h	Trim time out 300ms
Secure feature support	SEC_FEATURE_SUPPORT	1	R	[231]	55h	1. Support the secure and insecure trim operations 2. Support the automatic secure purge operation on retired defective portions of the array 3. Secure purge operations are supported
Secure erase multiple	SEC_ERASE_MULT	1	R	[230]	TBD	SDP:19h DDP:32h QDP:64h ODP:64h
Secure trim multiple	SEC_ERASE_MULT	1	R	[229]	0A	10x1x300ms = 3s
Boot information	BOOT_INFO	1	R	[228]	7h	

Reserved	-	1	-	[227]	-	
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	20h	128KB*32 = 4MB
Access size	ACC_SIZE	1	R	[225]	6h	Super page size = 64 x 512B = 32KB
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	1h	High capacity erase group size 1 x 512KB
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	2h	
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	10h	
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	TBD	SDP:10h DDP:32h QDP:64h ODP:20h
Sleep current (VCC)	S_C_VCC	1	R	[220]	7h	VCC < 128μA for sleep
Sleep current (VCCQ)	S_C_VCCQ	1	R	[219]	7h	VCCQ < 128μA for sleep
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	[218]	17h	(2^23)*100us=838.86s
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	11h	(2^17)*100ns = 13ms
Sleep Notification timeout	SLEEP_NOTIFICATION_TIME	1	R	[216]	0Ch	(2^12)*10us = 40.960ms
Sector count	SEC_COUNT	4	R	[215:212]	TBD	SDP:0x39A0000h
Secure write protect information	SECURE_WP_INFC	1	R	[211]	1h	Support secure write protect
Minimum write performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	[210]	0h	
Minimum read performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	R	[209]	0h	
Minimum write performance for 8bit at 26MHz,for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0h	
Minimum read performance for 8bit at 26MHz,for	MIN_PERF_R_8_26_4_52	1	R	[207]	0h	

4bit at 52MHz						
Minimum write performance for 8bit at 26MHz	MIN_PERF_W_4_26	1	R	[206]	0h	
Minimum read performance for 8bit at 26MHz	MIN_PERF_R_4_26	1	R	[205]	0h	
Reserved	-	1	-	[204]	-	
Power class for 26MHz at 3.6V 1R	PWR_CL_26_360	1	R	[203]	0h	
Power class for 52MHz at 3.6V	PWR_CL_52_360	1	R	[202]	0h	
Power class for 26MHz at 1.95V	PWR_CL_26_195	1	R	[201]	0h	
Power class for 52MHz at 1.95V	PWR_CL_52_195	1	R	[200]	0h	
Partition switching	PARTITION_SWITCH_TIME	1	R	[199]	1h	1x10ms = 10ms
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	Ah	10x10ms = 100ms
I/O Driver Strength	DRIVER_STRENGTH	1	-	[197]	1Fh	Support JEDEC eMMC v5.1
Device type	DEVICE_TYPE	1	R	[196]	57h	
Reserved	-	1	-	[195]	-	
CSD structure	CSD_STRUCTURE	1	R	[194]	2h	
Reserved	-	1	-	[193]	-	
Extended CSD revision	EXT_CSD_REV	1	R	[192]	7h	EXT_CSD 1.6 (MMC v5.1)
Command set	CMD_SET	1	R/W/E_P	[191]	0h	
Reserved	-	1	-	[190]	-	
Command set revision	CMD_SET_REV	1	R	[189]	0h	
Reserved	-	1	R	[188]	-	
Power class	POWER_SUPPORT	1	R	[187]	0h	
Reserved	-	1	-	[186]	-	
High-speed interface timing	HS_TIMING	1	W/E_P	[185]	0h	
Strobe support	STROBE_SUPPORT	1	R	[184]	1h	
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	0h	

Reserved	-	1	-	[182]	-	
Erased memory content	ERASED_MEM_CONT	1	R	[181]	0h	
Reserved	-	1	-	[180]		
Partition configuration	PARTITION_CONFIRATION	1	R/W/E R/W/E_P	[179]	0h	
Boot configuration protection	BOOT_COMFIG_PROT	1	R/W R/W/C_P	[178]	0h	
Boot bus condition	BOOT_BUS_CONDITION	1	R/W/E	[177]	0h	
Reserved	-	1	-	[176]	-	
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E	[175]	0h	
Boot write protection status register	BOOT_WP_STATUS	1	R	[174]	0h	
Boot area protection status register	BOOT_WP	1	R/W R/W/C_P	[173]	0h	
Reserved	-	1	-	[172]	-	
User area write protection register	USER_WP	1	R/W R/W/C_P R/W/E_P	[171]	0h	
Reserved	-	1	-	[170]	-	
FW configuration	FW_CONFIG	1	R/W	[169]	0h	
PRMB size	PRMB_SIZE_MULT	1	R	[168]	20h	
Write reliability setting register	WR_REL_PARAM	1	R/W	[167]	1Fh	
Write parameter setting register	WR_REL_PARAM	1	R	[166]	15h	
Start sanitize operation	SANITIZE_START	1	W/E_P	[165]	0h	
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0h	
Enable background operations handshake	BKOPS_EN	1	R/W R/W/E	[163]	0h	
H/W reset function	RST_ R_FUCTION	1	R/W	[162]	0h	
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0h	
Max enhanced area size	MAX_ENH_SIZE_MULT	3	R	[159:157]	TBD	
Partitions attribute	PARTITIONS_ATTRIBU	1	R/W	[156]	0h	

	TE					
Partitioning setting	PARTITION_SETTING_	1	R/W	[155]	0h	
General purpose partition size	GP_SIZE_MULT	12	R/w	[154:143]	0h	
Enhanced user data area size	ENH_SIZE_MULT	3	R/W	[142:140]	0h	
Enhanced user data start	ENH_START_ADDR	4	R	[139:136]	0h	
Reserved	-	1	-	[135]	-	
Secure bad block	SEC_BAD_BLK_MGMNT	1	R	[134]	0h	
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0h	
Package Case temperature is control	TCASE_SUPPORT	1	W/E_P	[132]	0h	
Periodic Wake-up	PERIODIC_WAKEUP	1	R	[131]	0h	
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	0h	
Reserved	-	2	-	[129:128]	-	
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	<vendor specific>	[127:64]	37FFFFh	
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	1h	4kB
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0h	
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0h	Default 512B
1st initialization after	INI_TIMEOUT_EMU	1	R	[60]	0A	100ms*10=1000 ms
Class 6 commands	CLASS_6_CTRL	1	R	[59]	0h	
Number of addressed	DYNCAP_NEEDED	1	R	[58]	0h	
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	00h	1. URGENT_BKOPS status bit is supported. 2. DYNCAP_NEEDED status bit is supported. 3. SYSPOOL_EXHAUSTED status bit is supported.

						4. PACKED_ FAILURE
Exception events status	EXCEPTION_EVENTS_ ST	2	R	[55:54]	00h	Device Run Time update
Extended Partitions attribute	EXT_PARTITIONS_ATT RIBUTE	2	R/W	[53:52]	00h	
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0h	
Packed command status	PACKED_COMMAND_ ST	1	R	[36]	0h	Device Run Time update
Packed command failure index	PACKED_FAILURE_IN DEX	1	R	[35]	0h	Device Run Time update
Power Off Notification	POWER_OFF_NOTIFIC AT	1	R	[34]	0h	
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0h	
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0h	
Control to turn the barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0h	
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0h	
Mode operation codes	MODE_OPERATION_C ODES	1	W/E_P	[29]	0h	
Reserved	-	1	TBD	[28:27]	-	
FFU status	FFU_STATUS	1	R	[26]	0h	
Pre loading data size	PRE_LOADING_DATA_ SIZE	4	R/W/E_P	[25:22]	0h	
Max pre loading data size	MAX_PRE_LOADING_ DATA_E	4	R	[21:18]	TBD	SDP:0x39A0000h
Product state awareness enablement	PRODUCT_STATE_AW ARENESS_ENABLEME NT	1	R/W/E&R	[17]	01h	Manual mode only
Secure removal type	SETURE_REMOVAL_TY PE	1	R/E&R	[16]	3Bh	
Command queue mode enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0h	Enable ny CMDQ process
Reserved	-	15	-	[14:0]	-	

NOTE: Reversed bits should read as ‘0’.

Table.4 Extended CSD Register Table

3.4.1 Capacity for User Data

Capacity	LBA[Hex]	LBA[Dec]	Capacity[Bytes]
BWCTAK411G32G	0X3,9A0,000	60,424,192	30,937,186,304

Table.5 Capacity for User Data

3.5 RCA Register

The writable 16-bit relative device address register carries the device address assigned by the host during the device identification. This address is used for the addressing host device communication after the device identification procedure. The default value of the RCA register is 0x0001. The value 0x000 is reserved to set all devices into the stand-by status with CMD7.

3.6 DSR (Drivers Stage Register)

The 16-bit driver stage register (DSR) is described in detail in 0. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of device). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

4. eMMC5.0 New Features Description

4.1 General Description

All communication between host and device is controlled by the host (master). The host sends commands, which result in a device response.such as:

- HS400 ultra speed mode (Data Strobe Line)
- Production State Awareness function
- FFU function (Field Firmware Update)
- Sleep Notification in Power Off Notification
- Device Health Report
- Secure Removal Type
- Overshoot and undershoot
- Reference load for HS400
- RPMB address failure on Read operation

4.2 HS400 Bus Speed Mode

4.2.1 The HS400 mode features

Driver Type Values	Support	Nominal Impedance	Approximated driving capability compared to Type0	Remark
0	Mandatory	50Ω	X1	Default Driver Type, support up to 200MHz operation.
1	Optional	33Ω	×1.5	Support up to 200MHz operation.
2		66Ω	×0.75	The weakest drive that supports up to 200MHz Operation.
3		100Ω	×0.5	
4		40Ω	×1.2	

Table.6 I/0 Driver Strength Types

Note: Selecting HS Timing is depends on Host I/F speed, default is 0, but it can be '1' by host.

4.2.2 HS400 Device Input Timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode.

The device input timing is shown in figure below.

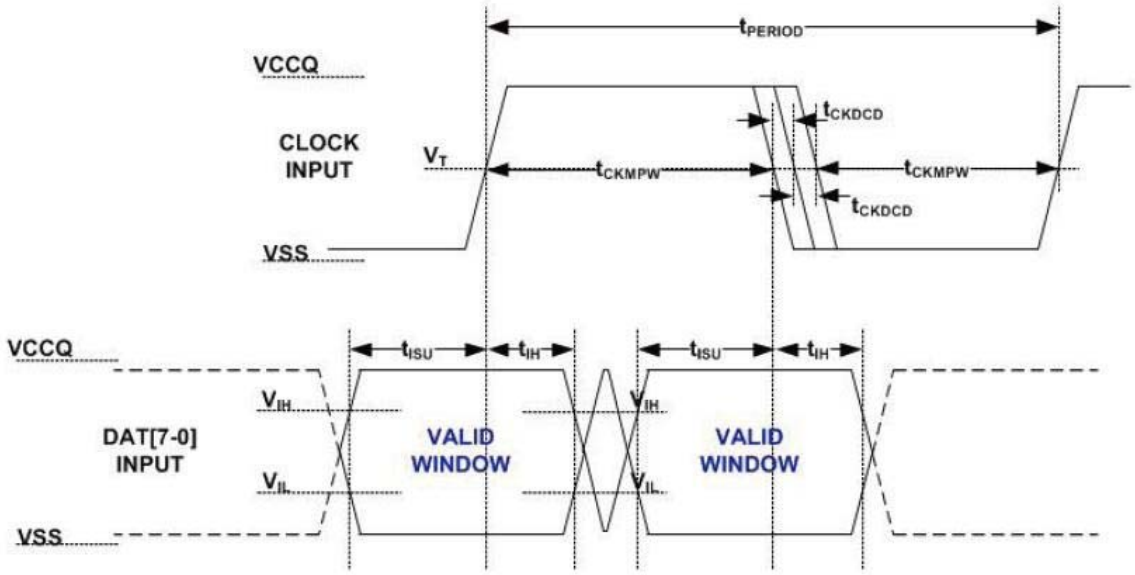


Figure.4 HS400 qNAND input timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	tPERIOD	5			200MHz(Max), between rising edges With respect to VT.
Slew rate	SR	1.125		V/ns	With respect to VIH/VIL.
Duty cycle distortion	tCKDCD	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to VT. includes jitter, phase noise
Minimum pulse width	tCKMPW	2.2		ns	With respect to VT.
Input DAT (referenced to CLK)					
Input set-up	tISUddr	0.4		ns	CDevice ≤ 6pF

time					With respect to VIH/VIL.
Input hold time	tIHddr	0.4		ns	CDevice ≤ 6pF With respect to VIH/VIL.
Slew rate	SR	1.125		V/ns	With respect to VIH/VIL.

Table.7 HS400 qNAND input timing

4.2.3 HS400 Device Output Timing

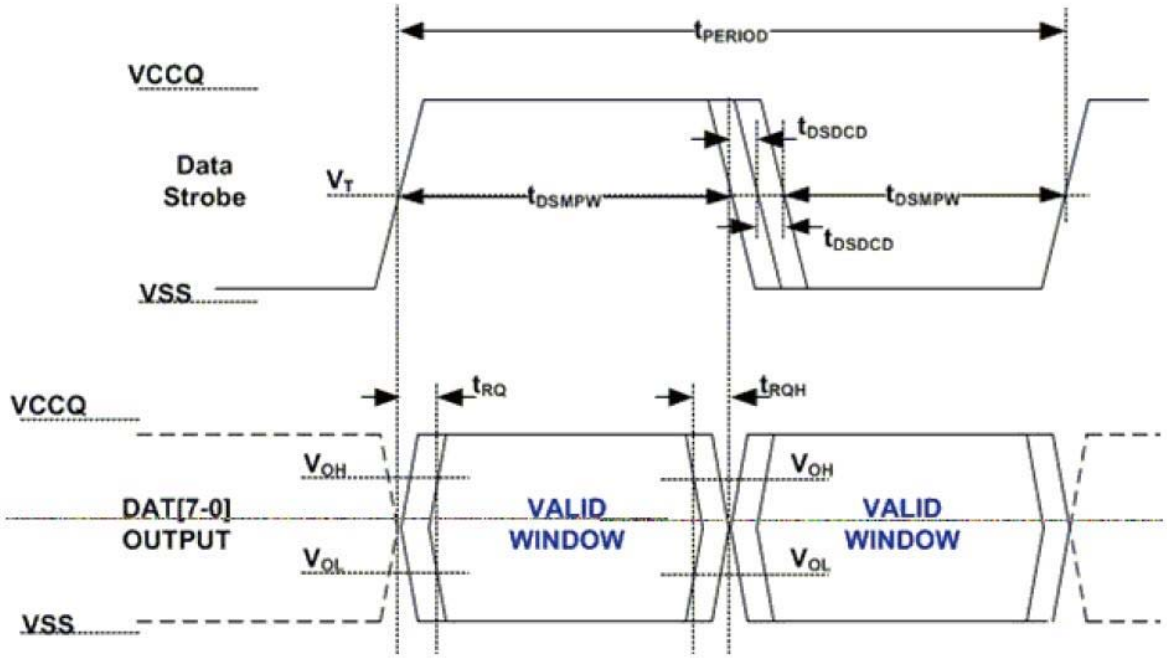


Figure.5 HS400 qNAND mode output timing

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	tPERIOD	5			200MHz(Max),between rising edges, with respect to VT
Slew rate	SR	1.125	------	V/ns	With respect to VOH/VOL and HS400 reference load
Duty cycle distortion	tDSDCD	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (tCKDCD)

					With respect to VT Includes jitter, phase noise
Minimum pulse width	tDSMPW	2.0		ns	With respect to VT
Read pre-amble	tRPRE	0.4	-	tPERIOD	Max value is specified by manufacturer. Value up to infinite is valid
Read post-amble	tRPST	0.4	-	tPERIOD	Max value is specified by manufacturer. Value up to infinite is valid
Output DAT (referenced to Data Strobe)					
Output skew	tRQ		0.4	ns	With respect to VOH/VOL and HS400reference load
Output hold skew	tRQH		0.4	ns	With respect to VOH/VOL and HS400reference load.
Slew rate	SR	1.125		V/ns	With respect to VOH/VOL and HS400reference load

Table.8 HS400 qNAND output timing

4.2.4 H400 (cont'd)

Parameter	Symbol	Min	Type	Max	Unit	Remark
Pull-up resistance for CMD	RCMD	4.7		100(1)	Kohm	
Pull-up resistance for DAT0-7	RDAT	10		100(1)	Kohm	
Pull-down resistance for Data Strobe	RDS	10		100(1)	Kohm	
Internal pull up resistance DAT1-DAT7	Rint	10		150	Kohm	
Bus signal line capacitance	CL			13	pF	
Single Device capacitance	CDevice			6	pF	

Table.9 HS400 Capacitance

4.3. Additional Timing changes in HS400 mode

4.3.1 Write Timing

In HS400 mode, default Start Bit position is valid at rising edge. In addition, the host should not stop CLK during transfer of data within a data block. The Data Strobe is used only in read operation. The Data Strobe is always "High-Z or Low" in write operation.

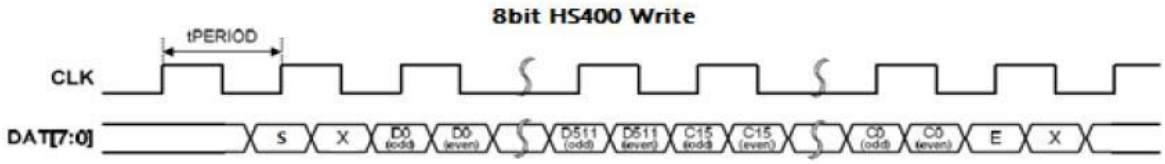


Figure.6 HS400 Write Timing

4.3.2 Read Timing

The Data Strobe is toggled only during data valid period (Start bit, Data, CRC16, End bit, CRC status token). In HS400 mode, Start Bit position is valid at both rising and falling edge. In addition, the host may stop CLK between data blocks rather than within a data block.

Data Strobe shall be driven tRPRE prior to the first Data Strobe rising edge and tRPST after the last falling edge.

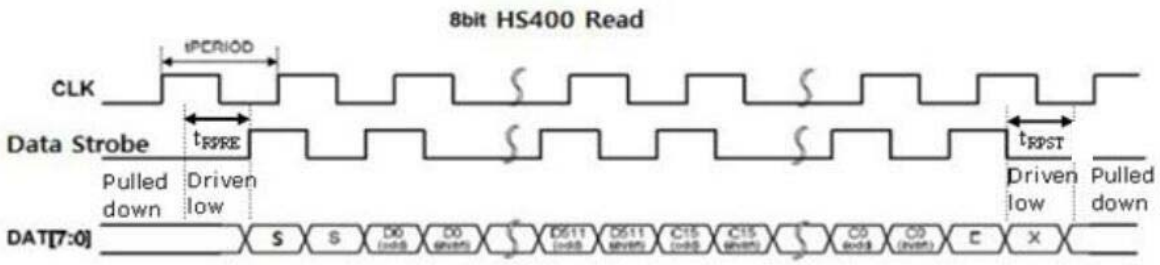


Figure.7 HS400 Read Timing

4.4 Production State Awareness

qNAND device can utilize the information of whether it is in production environment and operate differently than it operates in the field.

For example, content that was loaded into the storage device prior to soldering might get corrupted at higher probability during device soldering. The qNAND device could

use "special" internal operations for loading content prior to device soldering which can reduce production failures and use "regular" operations post-soldering.
PRODUCTION_STATE_AWARENESS [133] field in extended CSD is used as a mechanism through which the host should report to the device whether it is pre or post soldering state.
This standard defines two methods, Manual Mode and Auto Mode, to manage the device production state.
The trigger for starting or re-starting the process is setting correctly PRE_LOADING_DATA_SIZE field. Before setting this field the host is expected to make sure that the device is clean and any data which was written before to the device is expected to be erased using CMD35, CMD36 and CMD38.
In case the host erased data, override existing data or preformed re-partition during production state awareness , the production state awareness should be restarted by re-setting PRE_LOADING_DATA_SIZE.

4.5 Field Firmware Update (FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism the host downloads a new version of the firmware to the qNAND device and, following a successful download, instructs the e•MMC device to install the new downloaded firmware into the device.
In order to start the FFU process the host first checks if the qNAND device supports FFU capabilities by reading SUPPPORTED_MODES and FW_CONFIG fields in the EXT_CSD. If the qNAND device supports the FFU feature the host may start the FFU process. The FFU process starts by switching to FFU Mode in MODE_CONFIG field in the EXT_CSD. In FFU Mode host should use closed-ended or open ended commands for downloading the new firmware and reading vendor proprietary data. In this mode, the host should set the argument of these commands to be as defined in FFU_ARG field. In case these commands have a different argument the device behavior is not defined and the FFU process may fail. The host should set Block Length to be DATA_SECTOR_SIZE. Downloaded firmware bundle must be DATA_SECTOR_SIZE size aligned (internal padding of the bundle might be required).
Once in FFU Mode the host may send the new firmware bundle to the device using one or more write commands.
The host could regain regular functionally of write and read commands by setting

MODE_CONFIG field in the EXT_CSD back to Normal state. Switching out of FFU mode may abort the firmware download operation. When switched back-in to FFU Mode, the host should check the FFU Status to get indication about the number of sectors which were downloaded successfully by reading the NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED in the extended CSD. In case the number of sectors which were downloaded successfully is zero the host should re-start downloading the new firmware bundle from its first sector. In case the number of sectors which were downloaded successfully is positive the host should continue the download from the next sector, which would resume the firmware download operation.

4.6 Sleep Notification

Host may use to a power off notification when it intends to turn-off VCC after moving the device to sleep state. Some features are added to clarify the spec for entering sleep mode when power off notification enabled.

■ **Add the SLEEP_NOTIFICATION on the interruptible Command List**

CMD	Description	Is interruptible
CMD6	SWITCH, Byte POWER_OFF_NOTIFICATION, Value POWER_OFF_LONG or SLEEP_NOTIFICATION	Yes

■ **SLEEP_NOTIFICATION_TIME[216](Read Only)**

Maximum timeout for the SWITCH command when notifying the device that it is about to move to sleep state by writing SLEEP_NOTIFICATION to POWER_OFF_NOTIFICATION [34] byte. (Unit: 10us)

Value	Description	Timeout value
0x01 ~ 0x17	Sleep Notification Timeout = 10us x 2 SLEEP_NOTIFICATION_TIME	0xC (40.96ms)
0x18 ~ 0xFF	Reserved	

■ **Power_ Off_ NOTIFICATION[34] (R/W/E_P)**

Add 0x04h for the SLEEP_NOTIFICATION as a valid value

Value	Field	Description
:	:	:
0x03	POWER_OFF_LONG	Host is going to power off the device, the device shall respond within POWER_OFF_LONG_TIME
0x04	SLEEP_NOTIFICATION	Host is going to put device in sleep mode, the device shall respond within SLEEP_NOTIFICATION_TIME

4.7 Health (Smart) Report [301-270]

This field is undefined for now.

4.8 Secure Removal Type

This field indicates that how information is removed from the physical memory during a Purge operation.

The first 4bits (Bit0~Bit3) indicate the capability of the qNAND device. The next two bit indicates configurable option. It can be set once during system integration by host.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		Configure Secure Removal Type		Supported Secure Removal Type			
		R/W		R			

Table.10 Secure Removal Type

Supported Secure Removal Type

Bit [7:6]: Reserved

Bit [5:4]: Configure Secure Removal Type

0x0: information removed by an erase of the physical memory

0x1: information removed by an overwriting the addressed locations with a character followed by an erase

0x2: information removed by an overwriting the addressed locations with a character, its complement, then a random character

0x3: information removed using a vendor defined

Bit [3:0]: Supported Secure Removal Type

Bit 0: information removed by an erase of the physical memory

Bit 1: information removed by an overwriting the addressed locations with a character followed by an erase

Bit 2: information removed by an overwriting the addressed locations with a character, its complement, then a random character

Bit 3: Information removed using a vendor defined.

4.9 Overshoot/Undershoot Specification

		VCCQ	Unit
		1.70V – 1.95V	
Maximum peak amplitude allowed for overshoot area.	Max	0.9	V
Maximum peak amplitude allowed for undershoot area.	Max	0.9	V
Maximum area above VCCQ	Max	1.5	V-ns
Maximum area below VSSQ	Max	1.5	V-ns

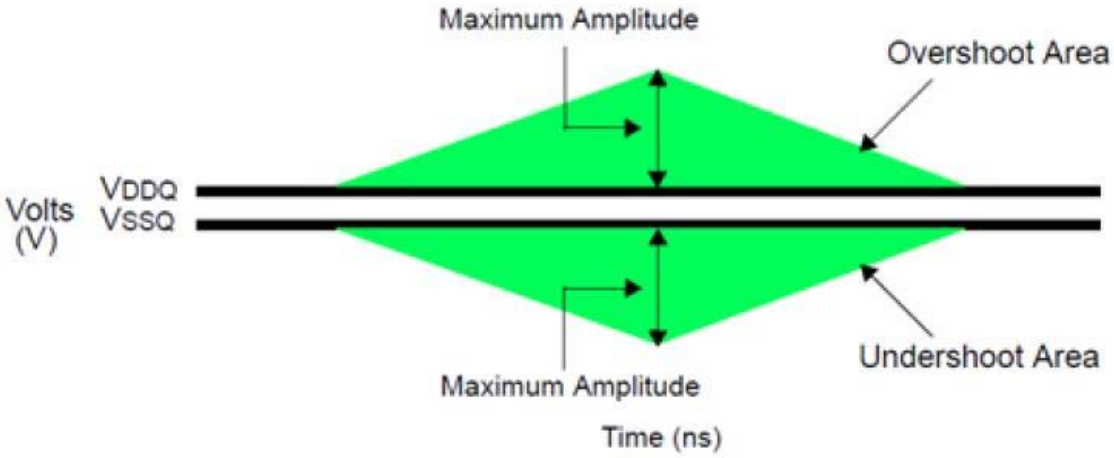


Figure.8 Overshoot/undershoot definition

4.10 HS400 reference load

The circuit in Figure 9 shows the reference load used to define the HS400 Device Output Timings and overshoot / undershoot parameters.

The reference load is made up by the transmission line and the CREFERENCE capacitance.

The reference load is not intended to be a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester.

System designers should use IBIS or other simulation tools to correlate the reference load to system environment. Manufacturers should correlate to their production test conditions.

Delay time (td) of the transmission line has been introduced to make the reference load independent from the PCB technology and trace length.

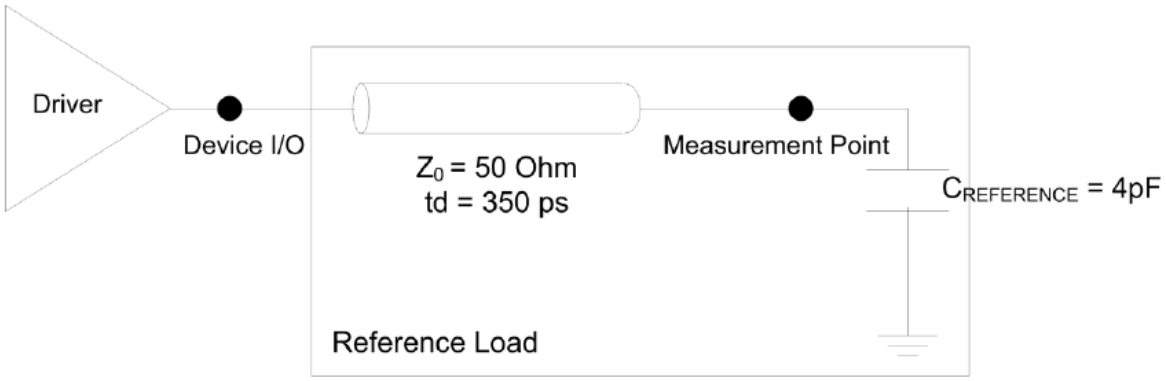


Figure.9 HS400 reference load

4.11 RPMB Throughput Improvement (For future eMMC spec)

This feature is proposed for RPMB write data size to improve the RPMB throughput at eMMC5.x spec. The supported maximum data size of RPMB write access is 8KB (32ea).

At this moment for qNAND device, supported Max. Data size is up 64ea (32KB). More information is shown in the following tables.

■ **RPMB Throughput**

qNAND provides up to 64ea for RPMB write data size.

	Max. data size	Using for improve RPMB Throughput
eMMC5.x Spec.	32ea (<=8KB)	Setting the EN_RPMB_REL_WR (Bit[4] of EXT_CSD)[166]) Value
Present status for qNAND	64ea (<=16KB)	Set the value for 'Number of block[15:0]' argument of CMD23 and Bit[31] 'reliable Write Request' is set to '1'

5. Electrical Characteristics

5.1 DC Power Specification

Parameter	Min	Typ	Max	Unit	Remark
Supply voltage (Controller and I/O)	2.7(1.7)	3.3(1.8)	3.6(1.95)	V	VCCQ
Supply voltage (NAND Flash and NAND Flash interface)	2.7	3.3	3.6	V	VCC
Supply voltage for core	-0.5	0	0.5	V	VSS
I/O input leakage current	-100		100	uA	
I/O output leakage current	-100		100	uA	
Programmable pull-up resistor	50	75	100	Kohm	VCCQ = 3.3V
Programmable pull-down resistor	50	75	100	Kohm	VCCQ = 3.3V
Pre-initial standby current				uA	
Sleep current				uA	
Operating temperature	-20	+25	+85	°C	

Table.11 General DC Characteristics for qNAND

5.2 Typical Power Consumption

Density	$I_{CC\ (3.3V)}$	$I_{CCQ(1.8V)}$	Unit
32GB	100	100	μA

Table.12 Sleep Current

Density	$I_{CC(3.3V)}$	$I_{CCQ(1.8V)}$	Unit
32GB	40	40	mA

Table.14 Active Power Consumption during operation

6. qNAND Connection Guide

This appendix is just guideline for qNAND connection. The values in the below Schematic can be changed depending on the system environment.

Coupling capacitor should be connected with VDD and VSS as closely as possible. VDDI capacitor is min 1uF.

If host does not use H/W reset, it is not needed to put 10K pull-up resistance on H/W rest line. It is recommended to separate VCCQ and VCC power.

The below connection guide is an example for customers to adopt qNAND more easily.

