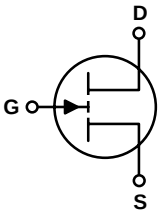
INN050W094FAD

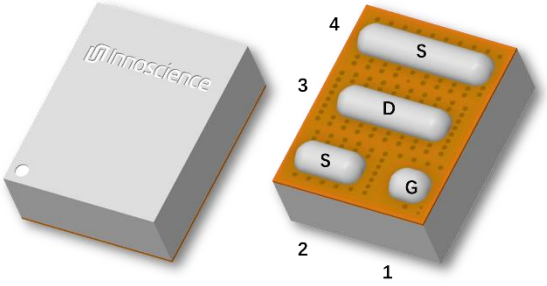
1. General Description

GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in WLCSP with 1.5 mm x 1.2 mm package size.



2. Features

- GaN-on-Silicon E-mode HEMT technology
- Industry application
- Very low gate charge
- Ultra-low on resistance
- Very small footprint



Top View Bottom View

3. Applications

- High frequency DC-DC converter
- High density DC/DC power module
- LED lighting
- 12V-24V input motor drivers
- USB-C battery chargers

4. Key Performance Parameters

Table 1 Key performance parameters at T_J = 25 ˚C

Parameter	Value	Unit
$V_{DS,max}$	50	V
$R_{DS(on),typ}$ @ V_{GS} = 5 V	7.1	mΩ
$R_{DS(on),max}$ @ V_{GS} = 5 V	9.4	mΩ
$Q_{G,typ}$ @ V_{DS} = 25 V	3.2	nC
$I_{DS,Pulse}$ (T_J = 25 ˚C)	100	A
Q_{OSS} @ V_{DS} = 25 V	8.6	nC

5. Pin Information

Table 2 Pin information

PIN	Pin Description	Pin Function
2,4	Source	Power Source
3	Drain	Power Drain
1	Gate	Driver Gate

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN050W094FAD	WLCSP 1.5 x 1.2	E06

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6. Maximum Ratings

at T_J = 25 ˚C unless otherwise specified.

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage	50	V
$V_{DS(tr)}$	Drain-to-Source Voltage [1] (V_{GS} = 0 V, 1h total time, $T_A = T_{JMAX}$)	60	V
I_D	Continuous Current (V_{GS} = 5 V, T_C = 25 ˚C, $R_{\theta JC}$ = 2.20 ˚C/W)	54	A
	Continuous Current (V_{GS} = 5 V, T_C = 100 ˚C, $R_{\theta JC}$ = 2.20 ˚C/W)	34	A
	Continuous Current (V_{GS} = 5 V, T_C = 25 ˚C, $R_{\theta JC}$ = 6.15 ˚C/W)	33	A
	Continuous Current (V_{GS} = 5 V, T_C = 100 ˚C, $R_{\theta JC}$ = 6.15 ˚C/W)	21	A
	Continuous Current (V_{GS} = 5 V, T_A = 25 ˚C, $R_{\theta JA}$ = 57.66 ˚C/W)	11	A
	Pulsed (V_{GS} = 5 V, T_J = 25 ˚C, T_{Pulse} = 100 µs)	100	A
	Pulsed (V_{GS} = 5 V, T_J = 150 ˚C, T_{Pulse} = 100 µs)	90	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
$V_{GS(tr)}$	Gate-to-Source Voltage [1] (V_{DS} = 0 V, 168h total time, $T_A = T_{JMAX}$)	6.5	V
P_{tot}	Power Dissipation (V_{GS} = 5 V, T_C = 25˚C, $R_{\theta JC}$ = 2.20 ˚C/W)	57	W
	Power Dissipation (V_{GS} = 5 V, T_A = 25˚C, $R_{\theta JA}$ = 57.66 ˚C/W)	2.2	W
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	˚C

Note:

1. Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

7. Thermal Characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Top	2.20	˚C/W	-
$R_{\theta JC}$	Thermal Resistance, Junction to Board, Bottom	6.15	˚C/W	-
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient [2]	57.66	˚C/W	-
T_{sold}	Maximum Reflow Soldering Temperature	260	˚C	MSL1

Note:

2. $R_{\theta JA}$ is determined with the device on FR4 PCB (2s2p with thermal vias) defined in accordance with JEDEC standards. PCB is mounted in horizontal position without air stream cooling.

8. Electric Characteristics

at T_J = 25 °C unless otherwise specified.

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
I_{DSS}	Drain Source Leakage	-	0.5	5	μA	V_{GS} = 0 V, V_{DS} = 50 V
	Drain Source Leakage (T_J = 125 ˚C)	-	25	-	μA	V_{GS} = 0 V, V_{DS} = 50 V
I_{GSS}	Gate-to-Source Forward Leakage	-	0.5	5	μA	V_{GS} = 5 V
	Gate-to-Source Forward Leakage (T_J = 125 ˚C)	-	15	150	μA	V_{GS} = 5 V
	Gate-to-Source Forward Leakage	-	1	50	μA	V_{GS} = 6 V
	Gate-to-Source Reverse Leakage	-	0.1	10	μA	V_{GS} = -4 V
$V_{GS(TH)}$	Gate Threshold Voltage [3]	0.9	1.1	2.1	V	V_{DS} = V_{GS}, I_D = 2.3 mA
$R_{DS(on)}$	Drain-Source On-state Resistance [3]	-	7.1	9.4	mΩ	V_{GS} = 5 V, I_D = 2.5 A
V_{SD}	Source-Drain Forward Voltage	-	2.0	-	V	I_S = 6 A, V_{GS} = 0 V

Note:

3. $V_{GS(TH)}$ and $R_{DS(on)}$ is measured without prior drain bias or switching stress.

Table 7 Dynamic characteristics [4]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{ISS}	Input Capacitance	-	460	-	pF	V_{GS} = 0 V, V_{DS} = 25 V
C_{OSS}	Output Capacitance	-	175	-		V_{GS} = 0 V, V_{DS} = 25 V
C_{RSS}	Reverse Transfer Capacitance	-	3.9	-		V_{GS} = 0 V, V_{DS} = 25 V
$C_{OSS(ER)}$	Energy Related C_{OSS}	-	295	-		V_{GS} = 0 V, V_{DS} = 0 V to 25 V
$C_{OSS(TR)}$	Time Related C_{OSS}	-	345	-		V_{GS} = 0 V, V_{DS} = 0 V to 25 V
R_G	Gate Resistance	-	1.1	-	Ω	f= 5 MHz, open drain
Q_G	Total Gate Charge	-	3.2	-	nC	V_{GS} = 5 V, V_{DS} = 0 V to 25 V, I_D= 6 A
Q_{GS}	Gate to Source Charge	-	0.8	-		V_{GS} = 5 V, V_{DS} = 0 V to 25 V, I_D = 6 A
Q_{GD}	Gate to Drain Charge	-	0.4	-		V_{GS} = 5 V, V_{DS} = 0 V to 25 V, I_D = 6 A
V_{Plat}	Gate Plateau Voltage	-	1.8	-	V	I_D = 6 A, V_{DS} = 25 V, V_{GS} = 0 V to 5 V
$Q_{G(TH)}$	Gate Charge at Threshold	-	0.5	-	nC	V_{GS} = 5 V, V_{DS} = 0 V to 25 V, I_D = 6 A
Q_{OSS}	Output Charge	-	8.6	-		V_{GS} = 0 V, V_{DS} = 0 V to 25 V
Q_{RR}	Reverse Recovery Charge	-	0	-		V_{DS} = 25 V, I_S = 6 A

Note:

4. Guaranteed by design.

9. Electric Characteristics Diagrams

at T_J = 25 °C, unless specified otherwise

Fig. 1 Typ. Output Characteristics (T_J = 25 ˚C)

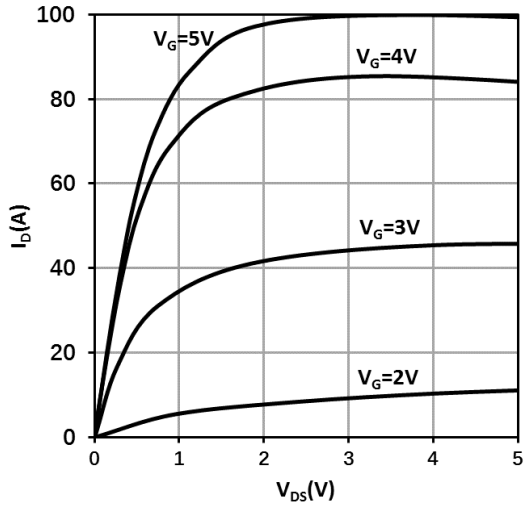


Fig. 2 Typ. Output Characteristics (T_J = 125 ˚C)

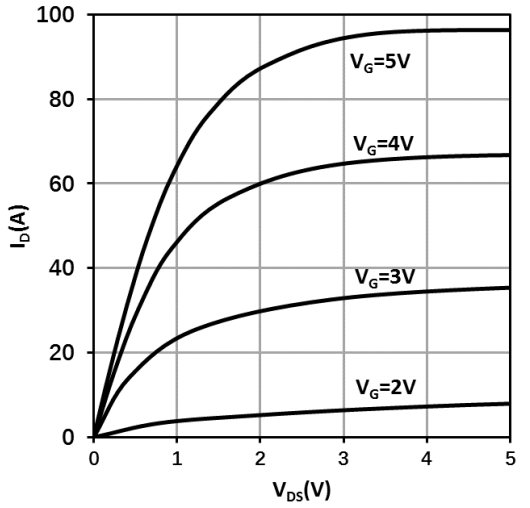


Fig. 3 Typ. Drain On-State Resistance (T_J = 25 ˚C)

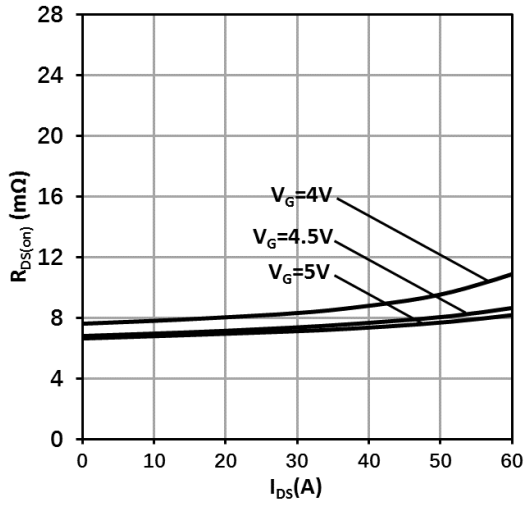


Fig. 4 Typ. Drain On-State Resistance (T_J = 125 ˚C)

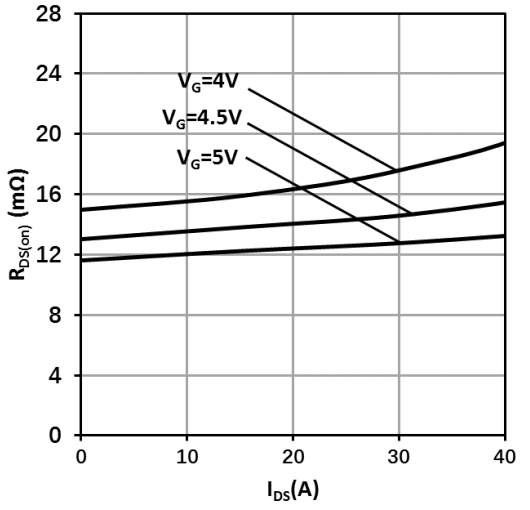


Fig. 5 Normalized On-State Resistance vs. Temp.

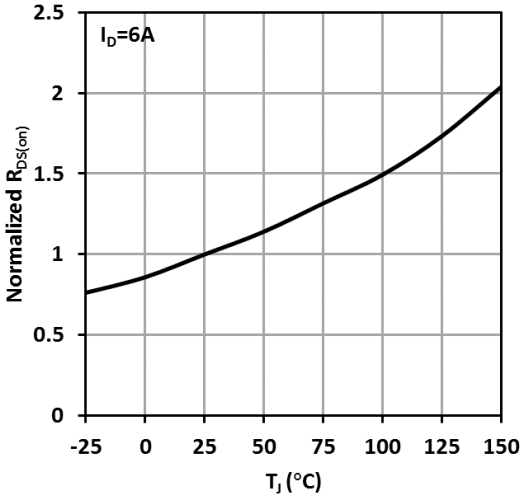


Fig. 6 Typ. Transfer Characteristics

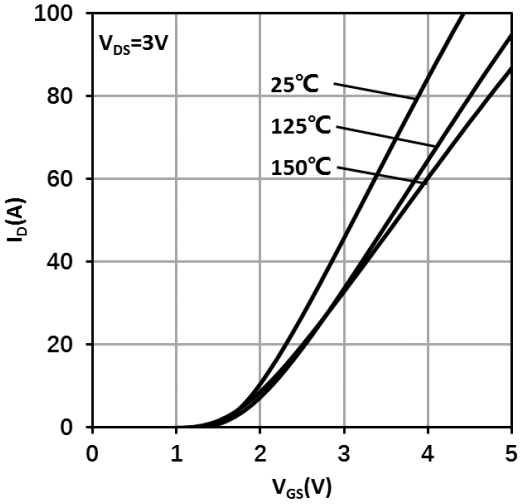


Fig. 7 Typ. Reverse Drain-Source Characteristics (V_{GS} ≤ 0,T_J = 25 ˚C)

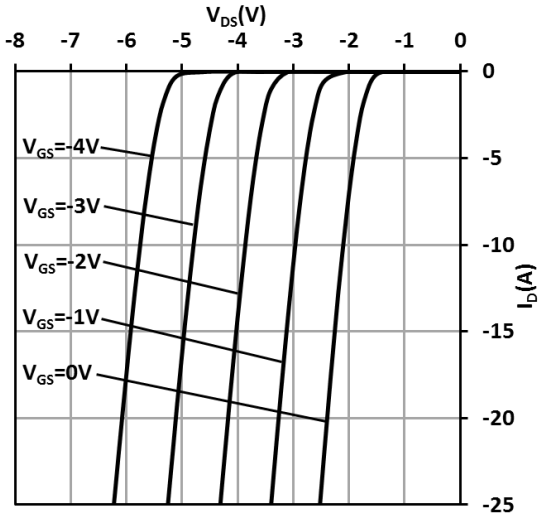


Fig. 8 Typ. Reverse Drain-Source Characteristics (V_{GS} ≥ 0,T_J = 25 ˚C)

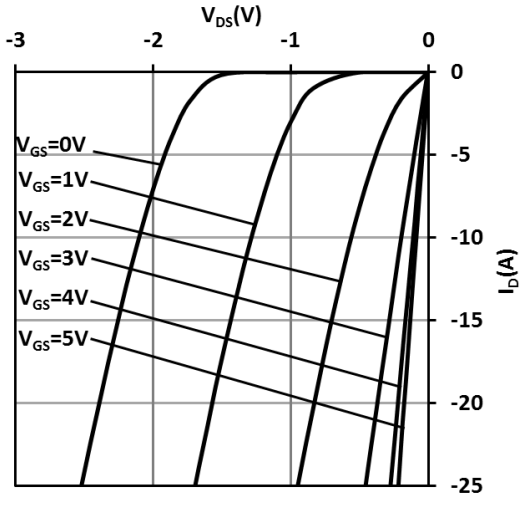


Fig. 9 Typ. Reverse Drain-Source Characteristics ($V_{GS} \leq 0$, T_J = 125 ˚C)

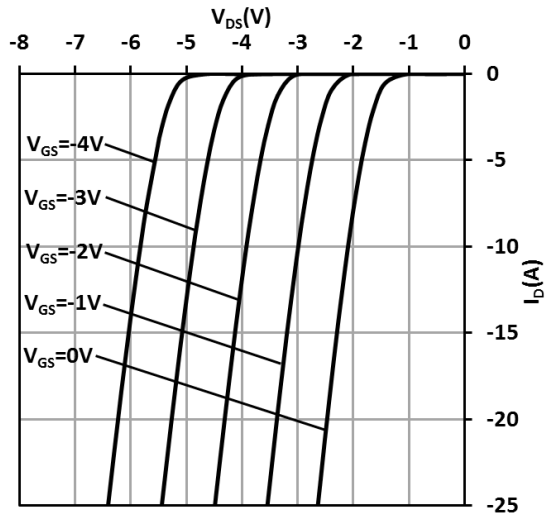


Fig. 10 Typ. Reverse Drain-Source Characteristics ($V_{GS} \geq 0$,T_J = 125 ˚C)

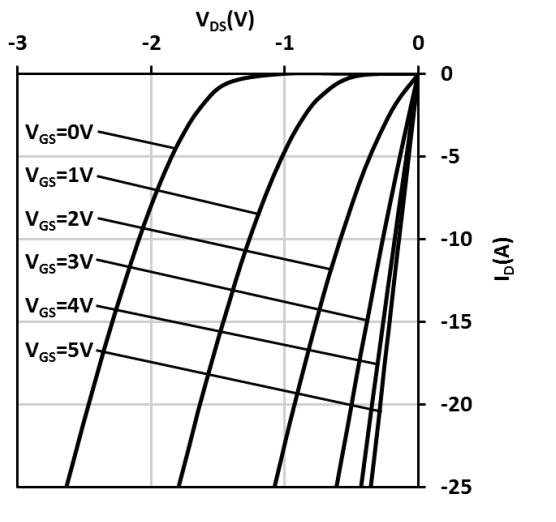


Fig. 11 Typ. Capacitances Characteristics

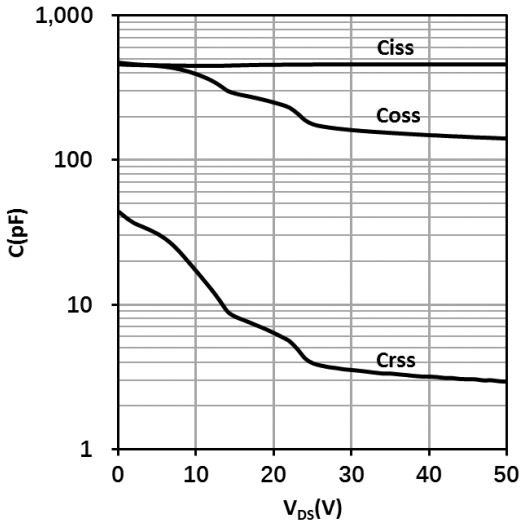


Fig. 12 Typ. Gate Charge

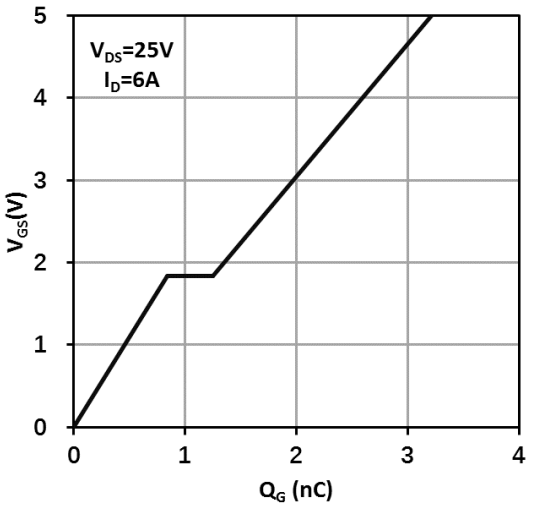


Fig. 13 Normalized Threshold Voltage vs. Temp.

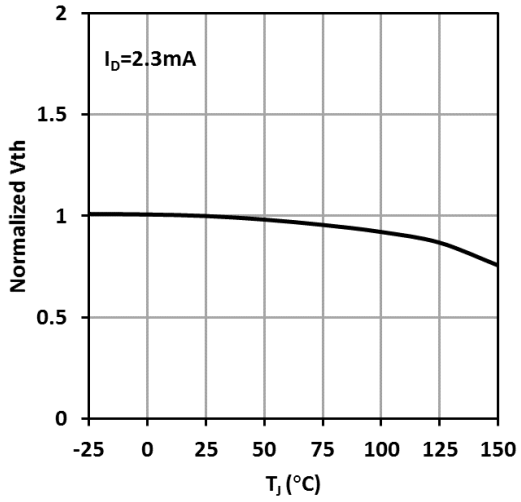


Fig. 14 Typ. Output Charge

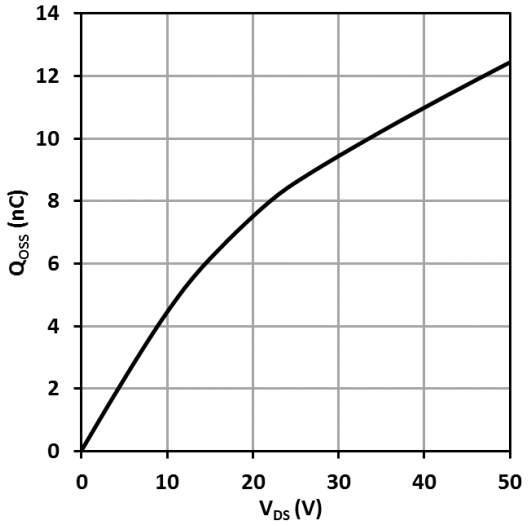


Fig. 15 Typ. Output Capacitance Stored Energy

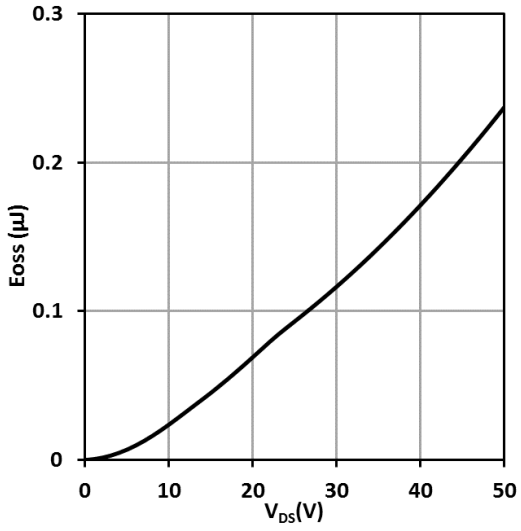


Fig. 16 Power Dissipation $P_{tot} = f(T_C)$, $R_{\theta JC}$ = 2.2 ˚C/W

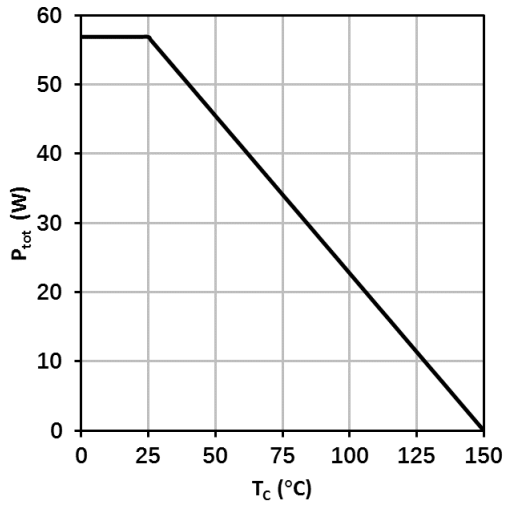


Fig. 17 Power Dissipation P_{tot} = f(T_A), $R_{\theta JA}$ = 57.66 ˚C/W

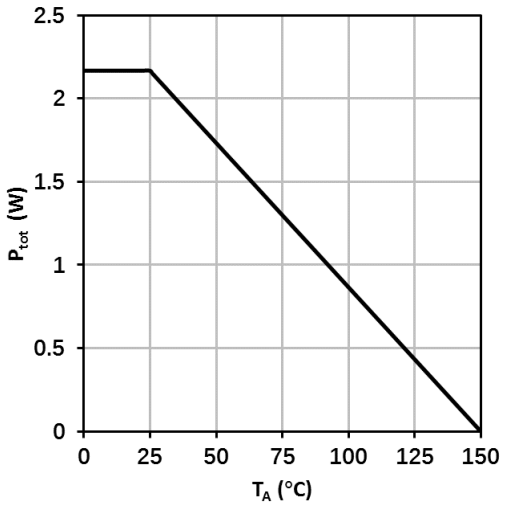


Fig. 18 Typ. Gate-to-Source Leakage Characteristics
I_G = f(V_{GS}); Drain Open

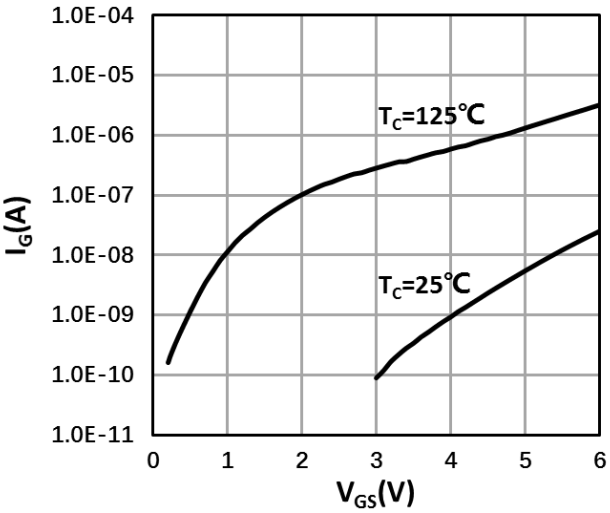


Fig. 19 Typ. Drain-Source Leakage Characteristics
I_{DSS} = f(V_{DS}); V_{GS} = 0 V

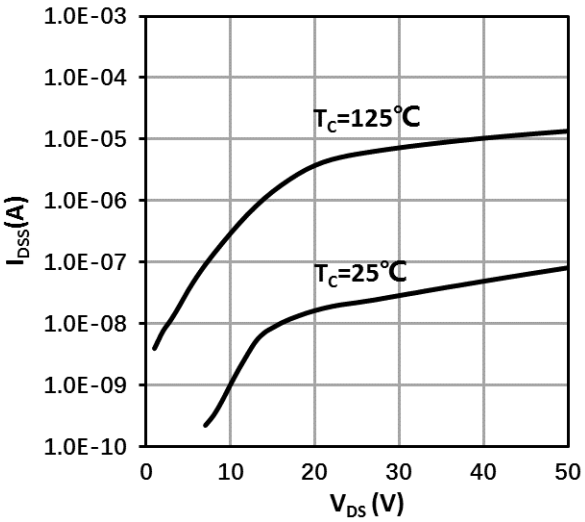


Fig. 20 Safe Operating Area
I_D = f(V_{DS}); T_C = 25 ˚C; Single Pulse; Parameter: t_p

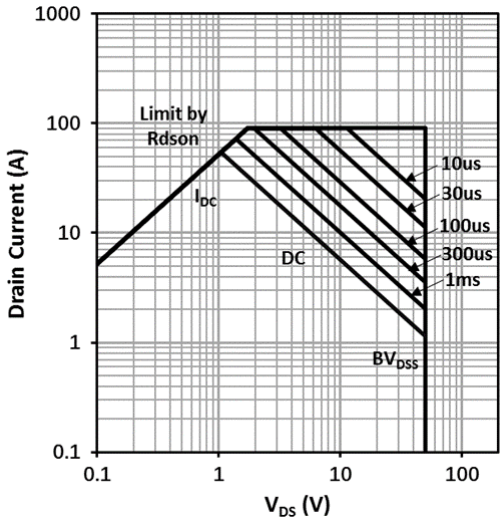


Fig. 21 Safe Operating Area
$I_D = f(V_{DS})$; T_C = 125 ˚C; Single Pulse; Parameter: t_p

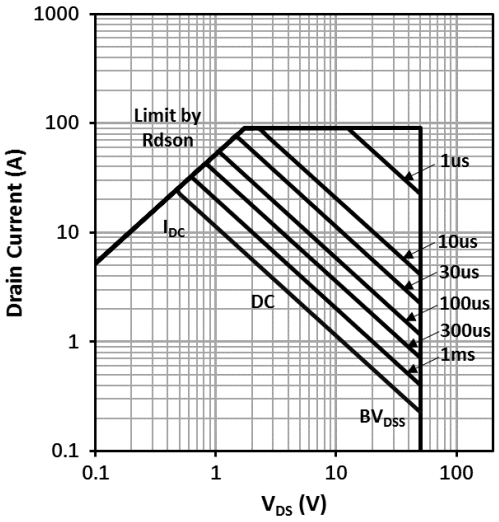
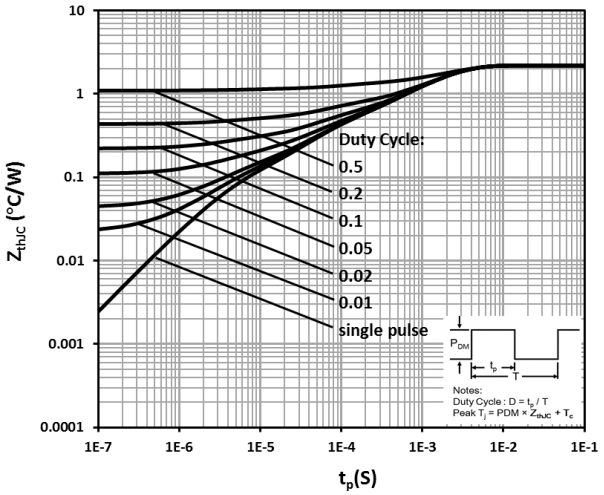
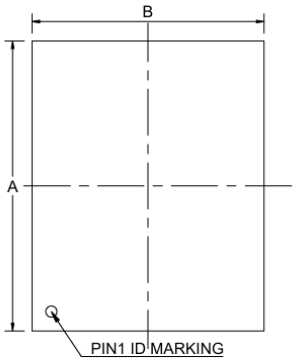


Fig. 22 Max. Transient Thermal Impedance
$Z_{thJC} = f(t_p)$; Parameter: $D=t_p/T$

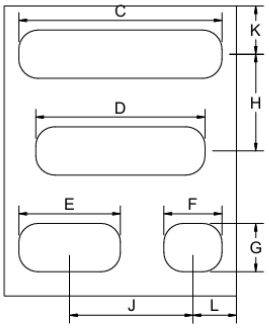


10. Package Outlines

Package Reference

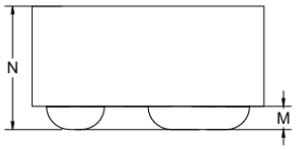


TOP VIEW



BOTTOM VIEW

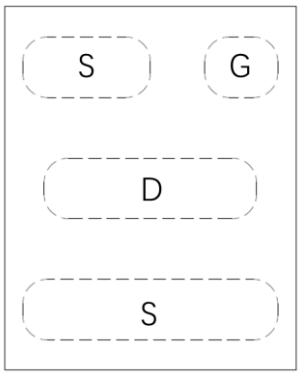
SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	1.475	1.500	1.525	
B	1.175	1.200	1.225	
C	1.030	1.050	1.070	
D	0.855	0.875	0.895	
E	0.505	0.525	0.545	
F	0.280	0.300	0.320	
G	0.230	0.250	0.270	4X
H	0.500 BSC			3X
J	0.6375 BSC			
K	0.250 REF			3X
L	0.225 REF			
M	0.100	0.120	0.140	
N	0.603	0.638	0.673	



SIDE VIEW

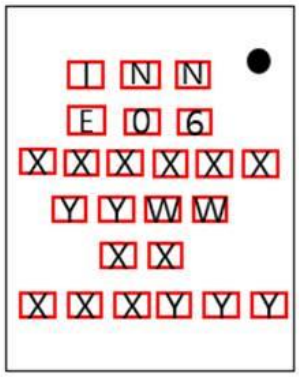
NOTE:
1)ALL DIMENSIONS ARE IN MILLIMETERS.
2)BOTTOM VIEW IS SOLDER BAR VIEW.
3)COMPLIES WITH JEDEC MO-211.
4)DRAWING IS NOT TO SCALE.
5)A,B IS PACKAGE SIZE.
6)BUMP STRUCTURE:10umCu+ 3umNi+ 107umSnAg.
7)BAR COPLANARITY SHALL BE 0.05 MILLIMETERS MAX.

Pin Configuration



TOP VIEW

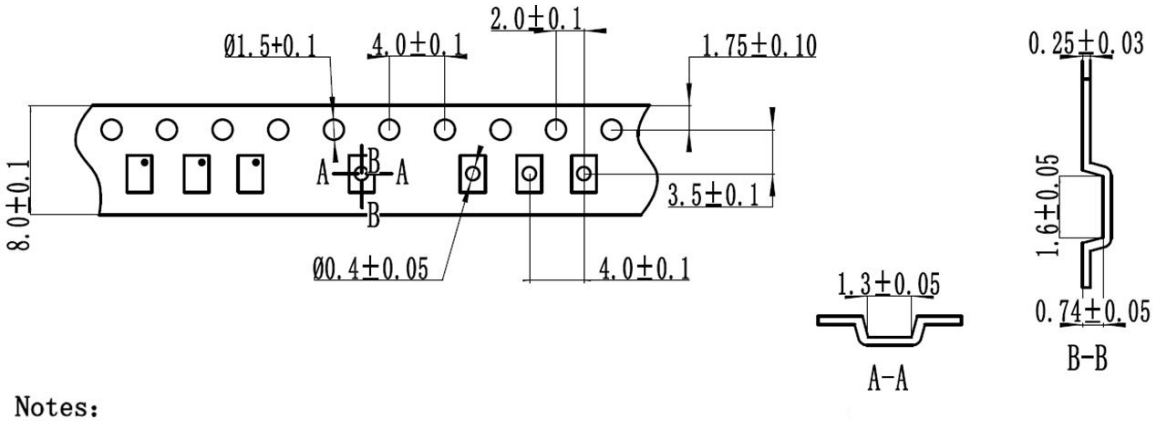
Marking Reference



TOP VIEW

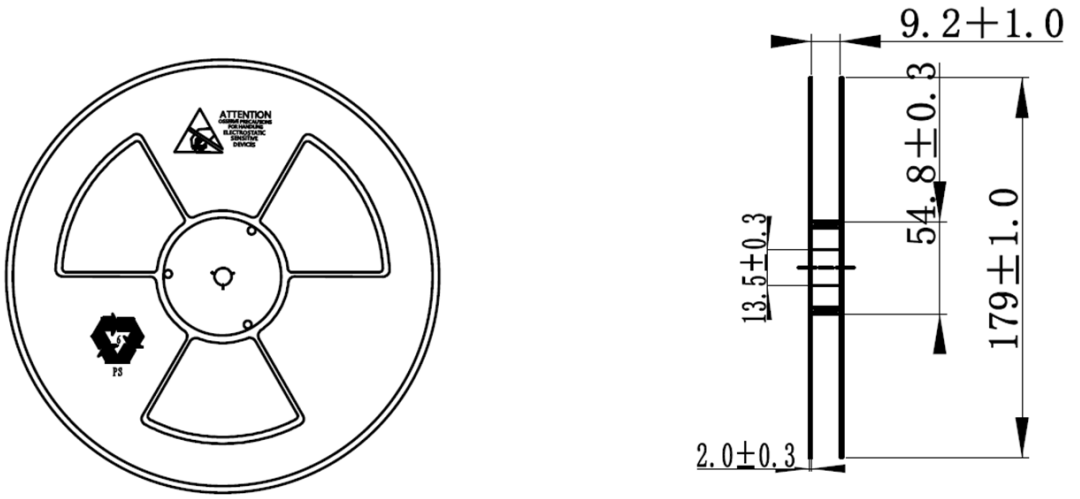
Row	Description	Example
Row 1	Company Name	INN
Row 2	Product Code	XXX
Row 3	Lot Code	XXXXXX
Row 4	Date Code	YYWW
Row 5	Wafer ID	XX
Row 6	Location ID	XXXYYY

11. Reel Information



Notes:
(1)The cumulative error of any 10 sprocket holes shall not exceed ± 0.20mm;
(2)The material thickness shall be measured based on the edge of the carrier tape;
(3)The unspecified tolerance is ± 0.1mm, and R<0.3mm is not specified;
(4)The unmarked demolding slope is 5 ° ;
(5)Surface Resistivity: 1*10 e 5 Ω/Δ ~ 1*11 e11

Unit: mm

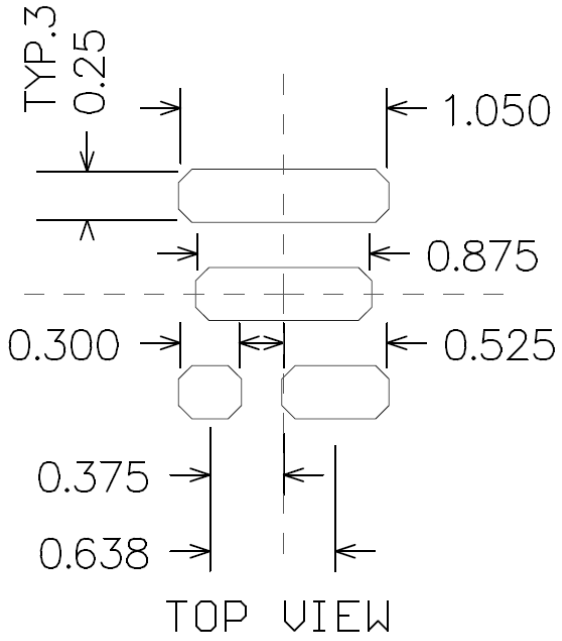


Notes:
1、The surface of the product should be smooth, clean, and free of injection molding defects, and there should be no significant burrs;
2、Material surface resistance:1*10e5Ω/Δ~1*10e10Ω/Δ;
3、No tolerance marked: ±0.3mm;

Unit: mm

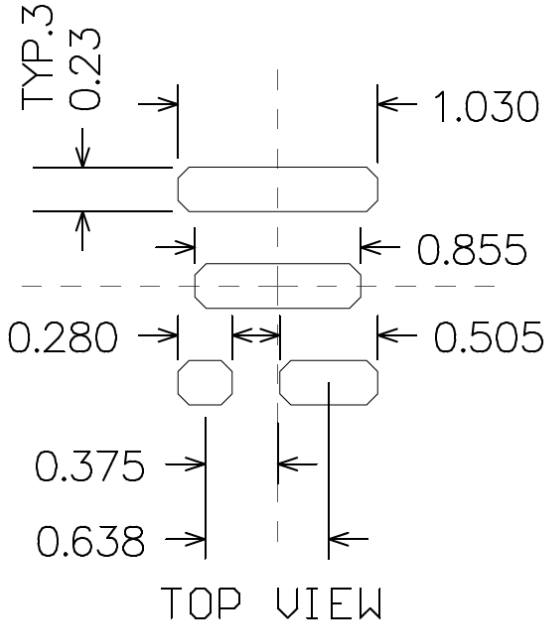
12. Land Pattern

Recommended Land Pattern



Unit: mm

Recommended Stencil Drawing



Unit: mm

13. Revision History

Major changes since the last revision

Revision	Date	Description of Changes
1.0	2026-3-23	1.0 version release

Important Notice

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