500mA, Low Quiescent Current, Low-Noise, High PSRR, Low-Dropout Linear Regulator

1 FEATURES

- **Input voltage range: 1.9 V to 5.5 V**
- **Output voltage range: 1.2 V to 4.2 V**
- **Up to 500mA load current**
- **Very low I_Q: 20μA(typical)**
- **Very high PSRR: 77dB at 1kHz**
- **Ultra low noise: 17μVrms at 1.8V output**
- **No noise bypass capacitor required**
- **Excellent load/line transient response**
- **Short circuit protection is typical 105mA**
- **With auto discharge function**
- **Output Voltage Accuracy: ±1%**
- **Micro Size Packages: SOT23-5, XDFN1X1-4**

2 APPLICATIONS

- **Smart Phones and Cellular Phones**
- **PDAs**
- **MP3/MP4 Player**
- **Digital Still Cameras**
- **Portable instrument**

3 DESCRIPTIONS

The RS3217F is a low-noise LDO that can supply up to 500mA output current. Designed to meet the requirements of RF and analog circuits, the RS3217F device provides low noise, high PSRR, low quiescent current, and low line or load transient response figures.

RS3217F is stable with a 1.0μF ceramic input and output capacitor, Using the new innovative design techniques, the RS3217F offers class-leading noise performance without a noise bypass capacitor.

RS3217F is available with fixed output voltages from 1.2V to 4.2V.

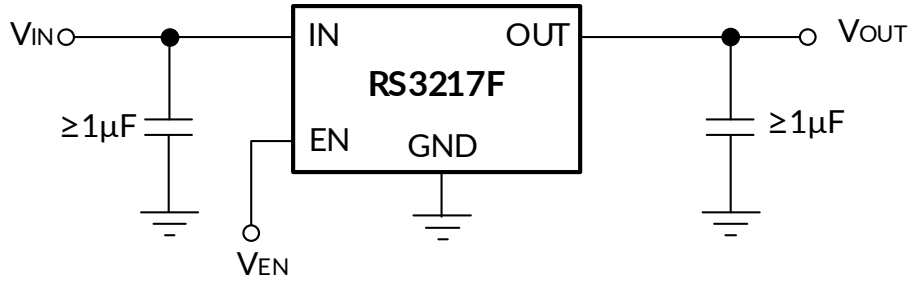
RS3217F is offered in a small SOT23-5 and XDFN1X1-4 packages, which is ideal for small form factor portable equipment.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS3217F	SOT23-5	1.60mm×2.92mm
	XDFN1X1-4	1.00mm×1.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



4 FUNCTIONAL BLOCK DIAGRAM

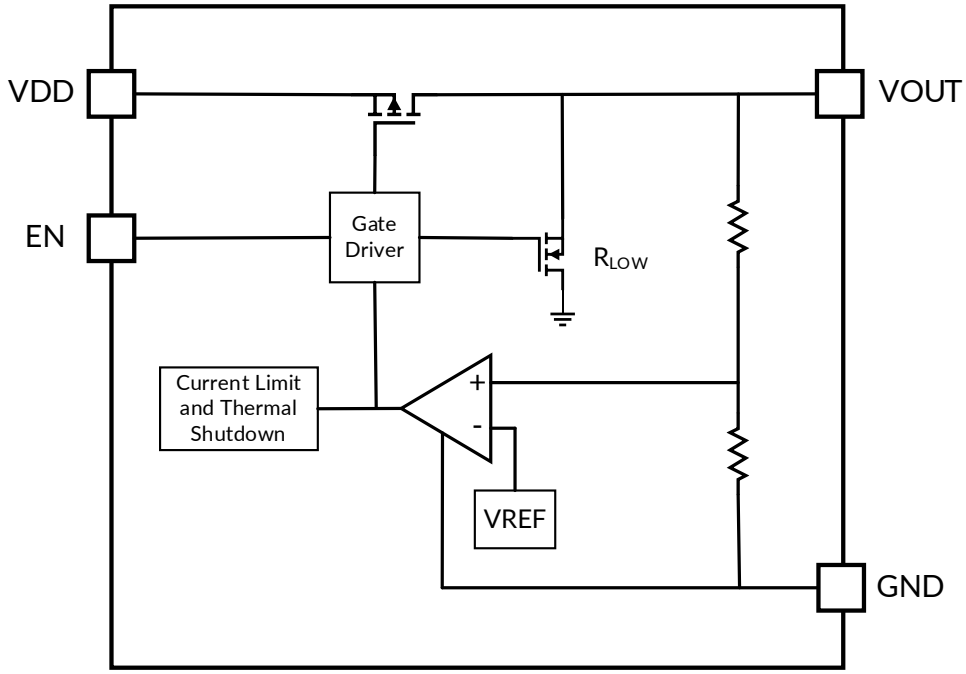


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5 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2024/09/14	Preliminary version completed
A.1	2024/12/18	Initial version completed
A.2	2025/03/03	Update HBM ESD Ratings
A.3	2025/04/29	Update Device Marking
A.4	2026/04/22	Add V_{DO} and I_{SHORT} parameter values for different output voltage versions in Electrical Characteristics
A.5	2026/10/28	Add RS3217F-1.9XF5 Orderable Device

6 PACKAGE/ORDERING INFORMATION (1)

Orderable Device	V_{OUT}(V)	Package Type	Op Temp(°C)	Device Marking (2)	MSL (3)	Package Qty
RS3217F-1.2XF5	1.2	SOT23-5	-40°C ~125°C	LT12	MSL3	Tape and Reel,3000
RS3217F-1.5XF5	1.5	SOT23-5	-40°C ~125°C	LT15	MSL3	Tape and Reel,3000
RS3217F-1.8XF5	1.8	SOT23-5	-40°C ~125°C	LT18	MSL3	Tape and Reel,3000
RS3217F-1.9XF5	1.9	SOT23-5	-40°C ~125°C	LT19	MSL3	Tape and Reel,3000
RS3217F-2.5XF5	2.5	SOT23-5	-40°C ~125°C	LT25	MSL3	Tape and Reel,3000
RS3217F-2.8XF5	2.8	SOT23-5	-40°C ~125°C	LT28	MSL3	Tape and Reel,3000
RS3217F-2.9XF5	2.9	SOT23-5	-40°C ~125°C	LT29	MSL3	Tape and Reel,3000
RS3217F-3.0XF5	3.0	SOT23-5	-40°C ~125°C	LT30	MSL3	Tape and Reel,3000
RS3217F-3.2XF5	3.2	SOT23-5	-40°C ~125°C	LT32	MSL3	Tape and Reel,3000
RS3217F-3.3XF5	3.3	SOT23-5	-40°C ~125°C	LT33	MSL3	Tape and Reel,3000
RS3217F-3.6XF5	3.6	SOT23-5	-40°C ~125°C	LT36	MSL3	Tape and Reel,3000
RS3217F-4.0XF5	4.0	SOT23-5	-40°C ~125°C	LT40	MSL3	Tape and Reel,3000
RS3217F-4.2XF5	4.2	SOT23-5	-40°C ~125°C	LT42	MSL3	Tape and Reel,3000
RS3217F-1.2XUTDN4	1.2	XDFN1X1-4	-40°C ~125°C	TA	MSL3	Tape and Reel,10000
RS3217F-1.5XUTDN4	1.5	XDFN1X1-4	-40°C ~125°C	TB	MSL3	Tape and Reel,10000
RS3217F-1.8XUTDN4	1.8	XDFN1X1-4	-40°C ~125°C	TC	MSL3	Tape and Reel,10000
RS3217F-2.5XUTDN4	2.5	XDFN1X1-4	-40°C ~125°C	TD	MSL3	Tape and Reel,10000
RS3217F-2.8XUTDN4	2.8	XDFN1X1-4	-40°C ~125°C	TE	MSL3	Tape and Reel,10000
RS3217F-2.9XUTDN4	2.9	XDFN1X1-4	-40°C ~125°C	TF	MSL3	Tape and Reel,10000
RS3217F-3.0XUTDN4	3.0	XDFN1X1-4	-40°C ~125°C	TG	MSL3	Tape and Reel,10000
RS3217F-3.2XUTDN4	3.2	XDFN1X1-4	-40°C ~125°C	TH	MSL3	Tape and Reel,10000
RS3217F-3.3XUTDN4	3.3	XDFN1X1-4	-40°C ~125°C	TJ	MSL3	Tape and Reel,10000
RS3217F-3.6XUTDN4	3.6	XDFN1X1-4	-40°C ~125°C	TK	MSL3	Tape and Reel,10000
RS3217F-4.0XUTDN4	4.0	XDFN1X1-4	-40°C ~125°C	TL	MSL3	Tape and Reel,10000
RS3217F-4.2XUTDN4	4.2	XDFN1X1-4	-40°C ~125°C	TN	MSL3	Tape and Reel,10000

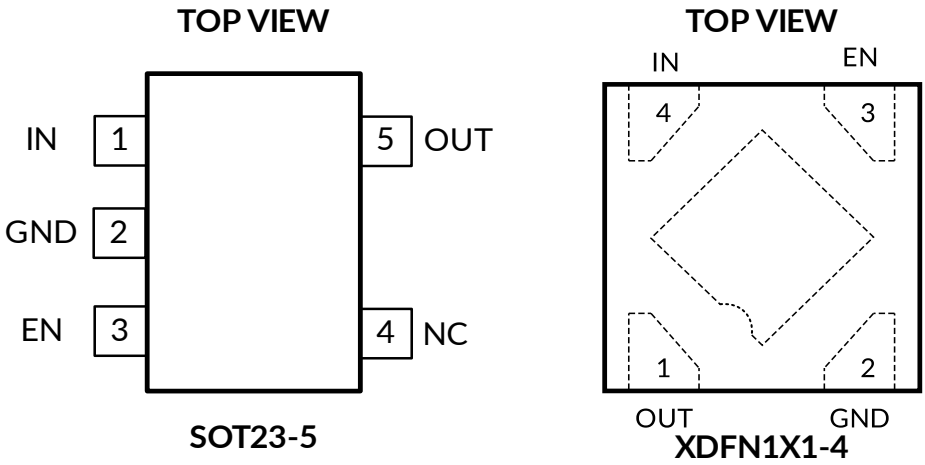
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F, Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

7 PIN CONFIGURATION AND FUNCTIONS



Pin Description

NAME	PIN		I/O (1)	DESCRIPTION
	SOT23-5	XDFN1X1-4		
IN	1	4	I	Input voltage supply. Must be closely decoupled to GND with a 1μF or greater capacitor.
GND	2	2	G	Common ground.
EN	3	3	I	Enable input. A low voltage (< V_{IL}) on this pin turns the regulator off and discharges the output pin to GND through an internal pulldown resistor. A high voltage (> V_{IH}) on this pin enables the regulator output. The EN pin can be connected to the IN pin if not used. Do not leave floating.
NC	4	-	-	Not internally connected.
OUT	5	1	O	Regulated output voltage. Connect a minimum 1μF low-ESR capacitor to this pin.
-	-	Thermal Pad	-	Connect the thermal pad to a large-area ground plane. This pad is not an electrical connection to the device ground.

(1) I=input, O=output, G= Ground.

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

			MIN	MAX	UNIT
V_{IN}	Input voltage		-0.3	6	V
V_{EN}	Enable input voltage		-0.3	6	V
V_{OUT}	Output voltage		-0.3	V_{IN} + 0.3	V
I_{OUT}	Maximum Load Current		Internally limited		mA
θ_{JA}	Package thermal impedance (3)	SOT23-5		200	°C/W
		XDFN1X1-4		315	
T_J	Junction temperature (4)		-40	150	°C
T_{stg}	Storage temperature		-65	150	°C
	Load Temperature (Soldering, 10sec)			260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to the GND pin.

(3) The package thermal impedance is calculated in accordance with JESD-51.

(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), MIL-STD-883K METHOD 3015.9	±4000	V
		Charged-Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2022	±1500	



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input Voltage Range on IN	1.9	5.5	V
V_{OUT}	Output Voltage Range on OUT	1.2	4.2	V
V_{EN}	Input Voltage Range on EN	0	5.5	V
I_{OUT}	Output Current Range on IOUT	0	500	mA
T_J	Junction Temperature	-40	125	°C

8.4 Electrical Characteristics

Over operating temperature range (–40°C≤ T_J ≤ 125°C). V_{OUT}=1.8V, V_{IN}=V_{OUTNOM}+1V, V_{EN}=1.2V, I_{OUT}=1mA, C_{IN}=1μF, C_{OUT}=1μF. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY AND CURRENTS							
Input Voltage (1)	V_{IN}			1.9		5.5	V
Quiescent Current	I_Q	V_{EN}=1.2V, I_{OUT}=0mA			20	35	μA
Ground Pin Current	I_{GND}	V_{EN}=1.2V, I_{OUT}=500mA			275		μA
Shutdown Current	I_{SD}	V_{EN} = 0V, V_{IN}=5.5V			0.01	1	μA
OUTPUT VOLTAGE							
Output Voltage Range	V_{OUT}			1.2		4.2	V
DC Output Accuracy (1)	ΔV_{OUT}	T_J = 25°C		-1		1	%
Line Regulation (1)	$\Delta V_{OUT(\Delta VIN)}$	V_{IN}=2.8 to 5.5V, I_{OUT}=1mA			0.01	0.1	%/V
Load Regulation	$\Delta V_{OUT(\Delta IOUT)}$	I_{OUT}=1mA to 500mA			5	10	mV
Output Voltage Temperature Coefficient	$\frac{\Delta V_{OUT}}{\Delta T_A \times V_{OUT}}$	I_{OUT} = 1mA, T_J = -40°C ~125°C			60		ppm/°C
Maximum output current	I_{OUTMAX}			500			mA
Line transient	ΔV_{OUT} (3)	V_{IN}=2.8 to 5.5V in 30μs			1		mV
		V_{IN}=5.5 to 2.8V in 30μs			1		mV
Load transient		I_{OUT}=1mA to 500mA in 10μs			25		mV
		I_{OUT}=500mA to 1mA in 10μs			25		mV
DROPOUT VOLTAGE							
Dropout Voltage (2)	V_{DO}	I_{OUT}=500mA	V_{OUT}=1.2V		700	1000	mV
			V_{OUT}=1.8V		320	400	
			V_{OUT}=2.8V		230	290	
			V_{OUT}=3.3V		220	280	
			V_{OUT}=4.2V		190	240	
POWER SUPPLY REJECTION RATIO AND NOISE							
Power Supply Rejection Ratio	PSRR (3)	f=100Hz, I_{OUT}=20mA			78		dB
		f=1kHz, I_{OUT}=20mA			77		dB
		f=10kHz, I_{OUT}=20mA			77		dB
		f=100kHz, I_{OUT}=20mA			68		dB
		f=1MHz, I_{OUT}=20mA			60		dB
Output Noise Voltage	V_N (3)	BW=10Hz to 100kHz, I_{OUT}=1mA			18		μV_{RMS}
		BW=10Hz to 100kHz, I_{OUT}=500mA			17		μV_{RMS}
ENABLE AND STARTUP TIME							
EN Input Logic High Voltage	V_{IH}	V_{IN}= 1.9 V to 5.5V, V_{EN} rising until the output is enabled		1.2			V
EN Input Logic Low Voltage	V_{IL}	V_{IN}= 1.9V to 5.5V, V_{EN} falling until the output is disabled				0.4	V
EN Input leakage current	I_{EN}	V_{IN}=5.5, V_{EN} = 0V			0.001	0.1	μA
		V_{IN}=5.5, V_{EN} = 5.5V			0.6	1	μA
Output Turn-on Delay Time	T_{ON}	From V_{EN}> V_{IH} to V_{OUT} = 95% of $V_{OUT(NOM)}$			75		μs
Overshoot on start-up		Stated as percentage of $V_{OUT(NOM)}$			0.2		%
Output discharge FET Rdson	R_{DIS}	V_{EN}<V_{IL} (output disable), V_{IN}=2.8V		50	75	100	Ω

PROTECTIONS						
Over Current Limit	I_{LMT}		600	850		mA
Short Current Limit	I_{SHORT}	V_{OUT}=0V	65	105	200	mA
Thermal shutdown threshold	T_{TSD} (3)	V_{IN}=2.8V, T_J rising		165		°C
Thermal shutdown hysteresis	T_{HYS} (3)	V_{IN}=2.8V, T_J falling from shutdown		30		°C

NOTES:

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 1.9V, whichever is greater.

(2) V_{DROP} FT test method: test the V_{OUT} voltage at V_{SET} +$V_{DROPMAX}$ with output current.

(3) Guaranteed by design and characterization, not a FT item.

8.5 Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

V_{IN} = 2.8V, I_{OUT} = 1mA, C_{IN} = Ceramic 1.0µF, C_{OUT} = Ceramic 1.0µF, unless otherwise noted.

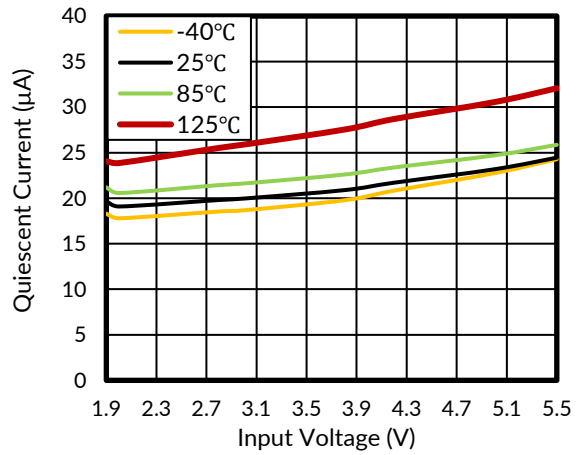


Figure 1. Quiescent Current vs Input Voltage

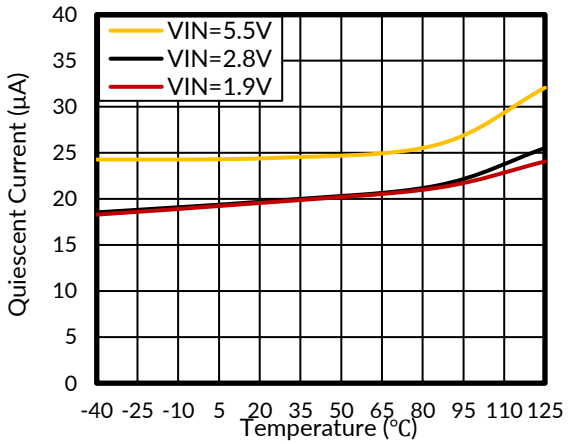


Figure 2. Quiescent Current vs Junction Temperature

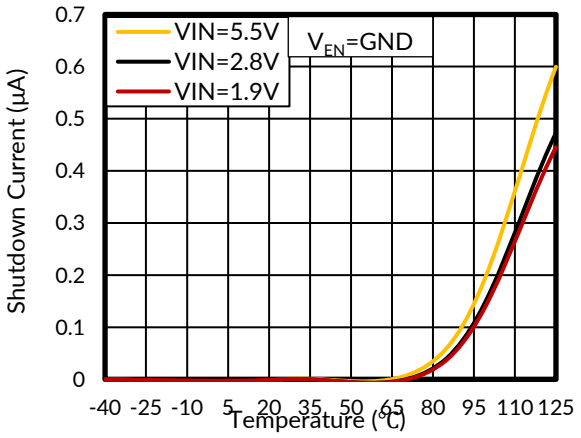


Figure 3. Shutdown Current vs Junction Temperature

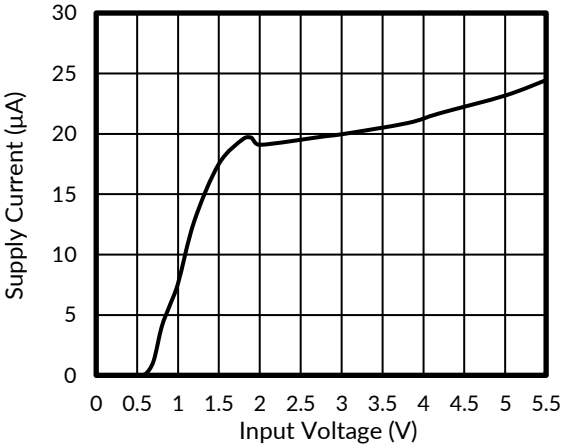


Figure 4. Supply Current vs Input Voltage

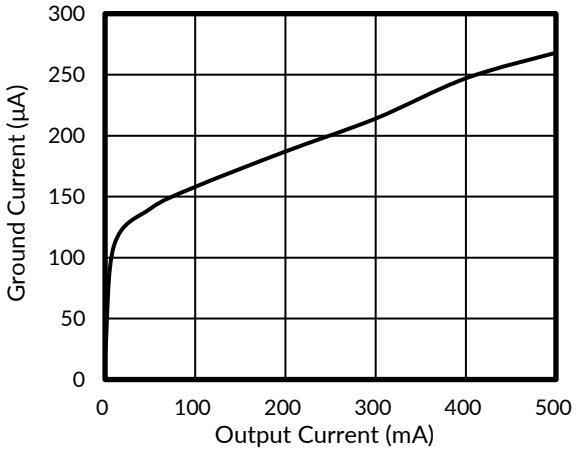


Figure 5. Ground Current vs Output Current

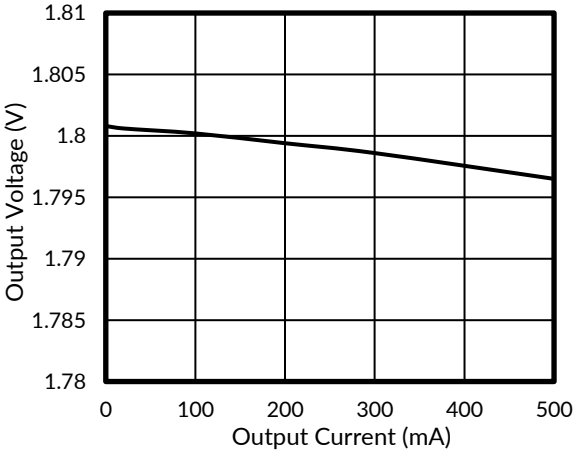


Figure 6. Load Regulation

Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

V_{IN} = 2.8V, I_{OUT} = 1mA, C_{IN} = Ceramic 1.0µF, C_{OUT} = Ceramic 1.0µF, unless otherwise noted.

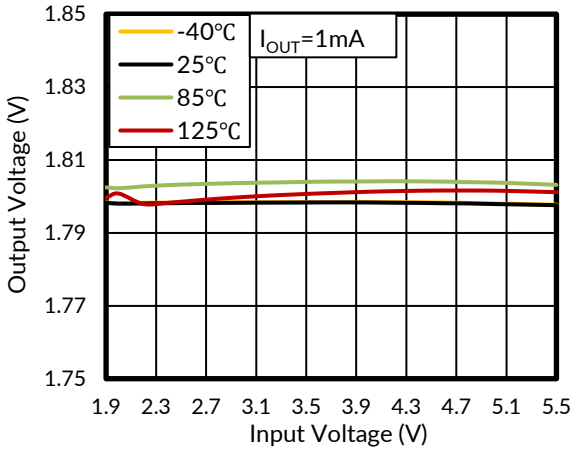


Figure 7. Line Regulation

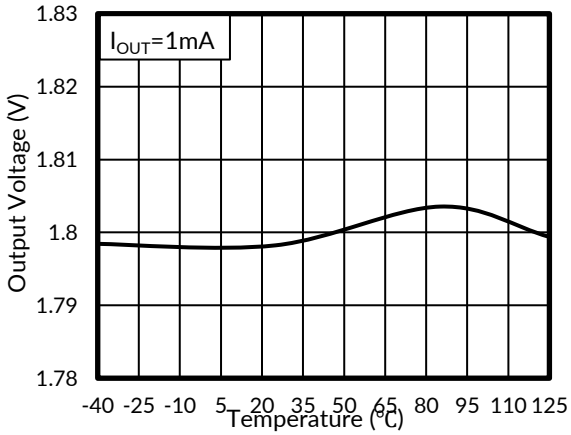


Figure 8. Output Voltage vs Junction Temperature

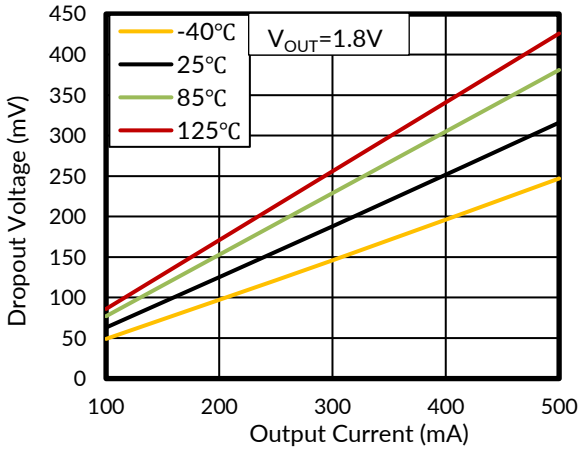


Figure 9. Dropout Voltage vs Output Current

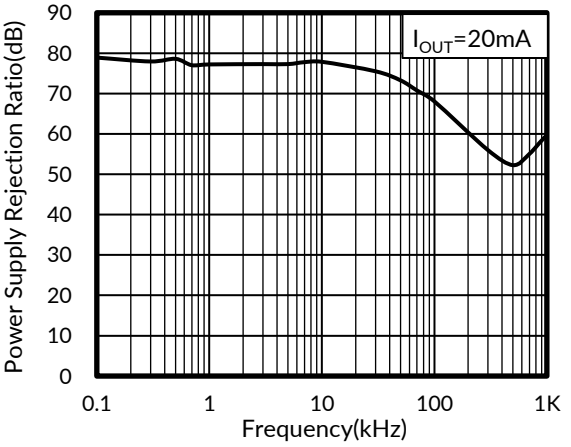


Figure 10. Power Supply Rejection Ratio vs Frequency

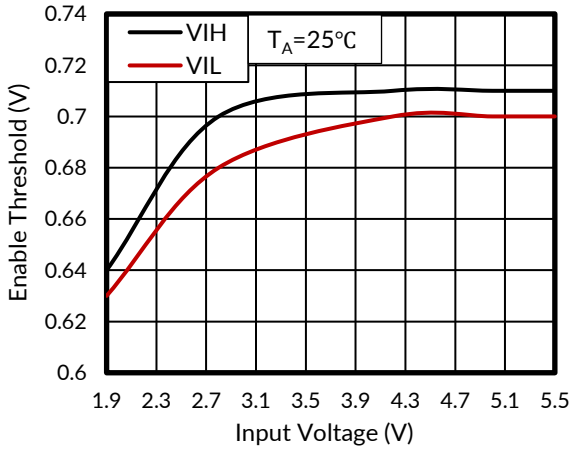


Figure 11. Enable Threshold vs Input Voltage

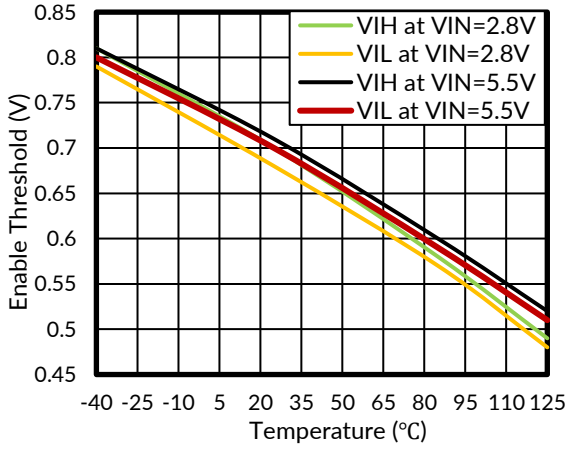


Figure 12. Enable Threshold vs Junction Temperature

Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

V_{IN} = 2.8V, I_{OUT} = 1mA, C_{IN} = Ceramic 1.0µF, C_{OUT} = Ceramic 1.0µF, unless otherwise noted.

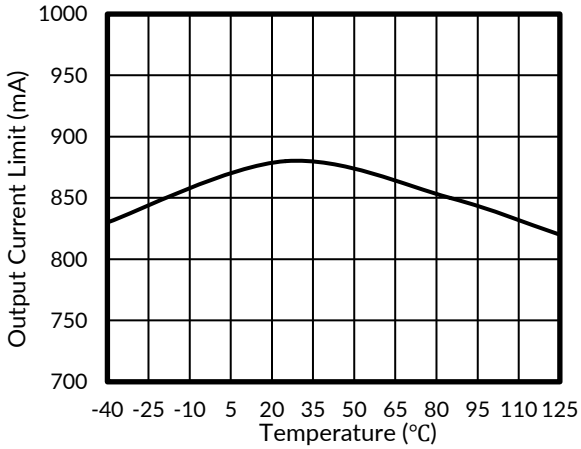


Figure 13. Output Current Limit vs Temperature

Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

V_{IN} = 2.8V, I_{OUT} = 1mA, C_{IN} = Ceramic 1.0μF, C_{OUT} = Ceramic 1.0μF, unless otherwise noted.

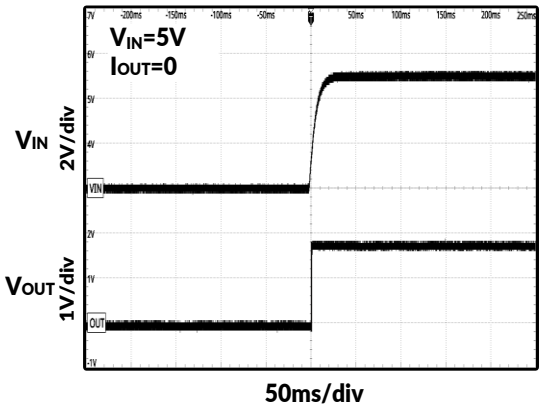


Figure 14. Power On

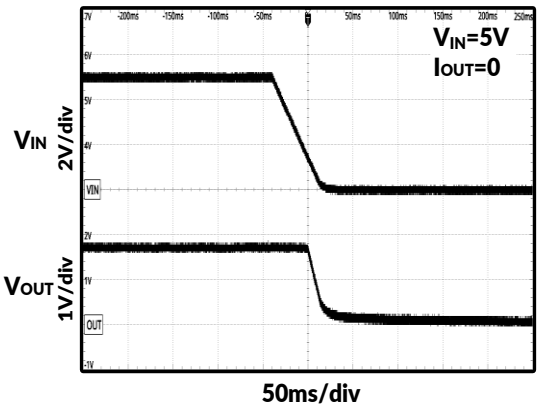


Figure 15. Power Off

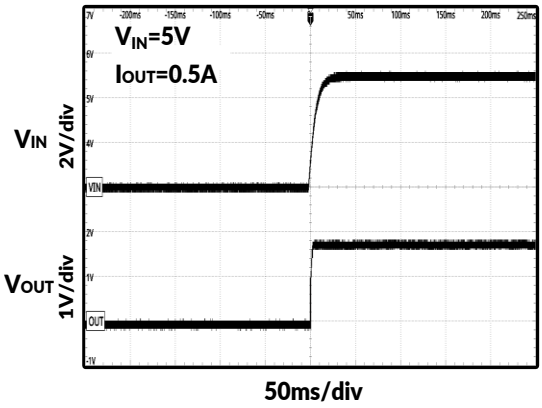


Figure 16. Power On

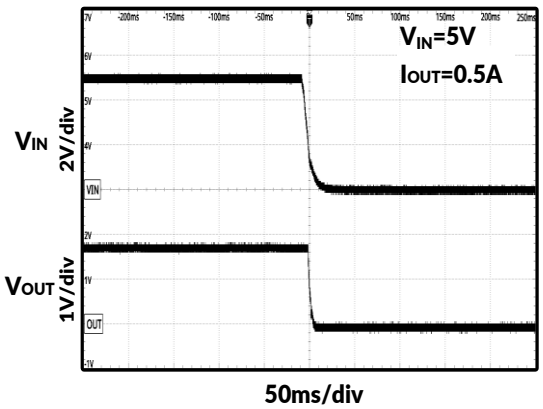


Figure 17. Power Off

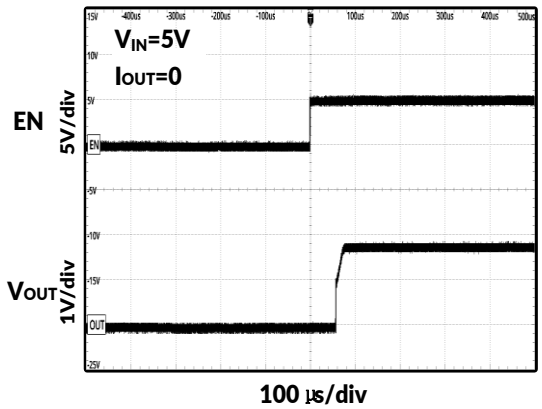


Figure 18. Turn On

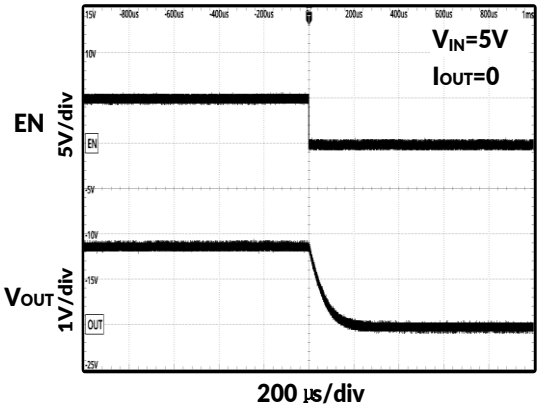


Figure 19. Turn Off

Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

V_{IN} = 2.8V, I_{OUT} = 1mA, C_{IN} = Ceramic 1.0μF, C_{OUT} = Ceramic 1.0μF, unless otherwise noted.

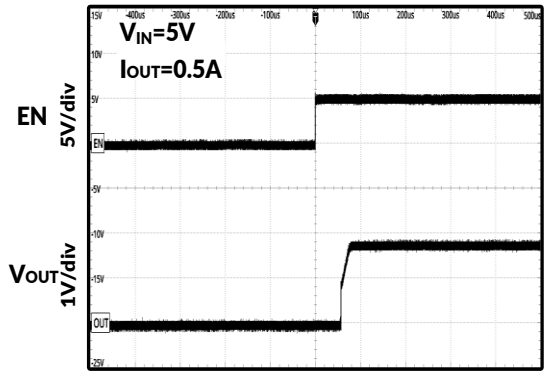


Figure 20. Turn On

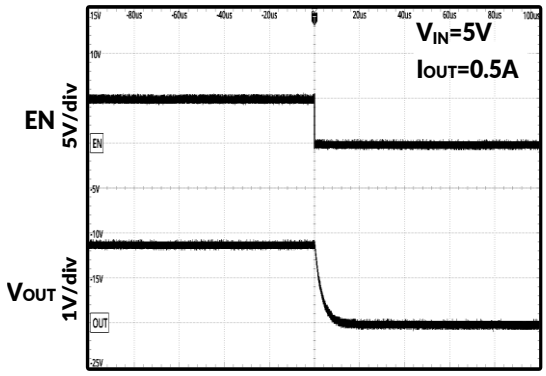


Figure 21. Turn Off

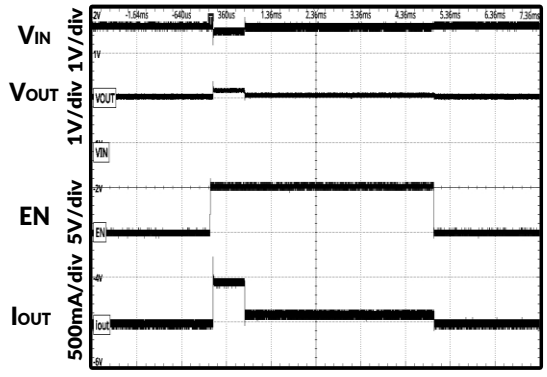


Figure 22. Short Circuit First, Then Turn On

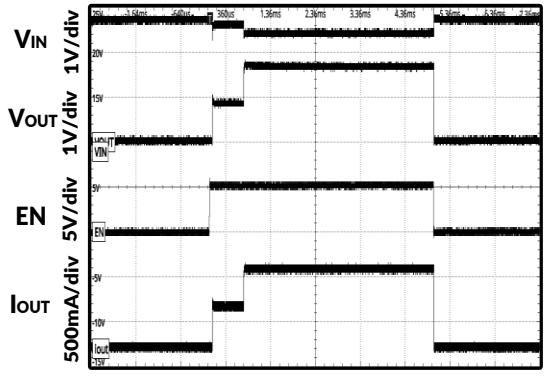


Figure 23. Overload Circuit First, Then Turn On

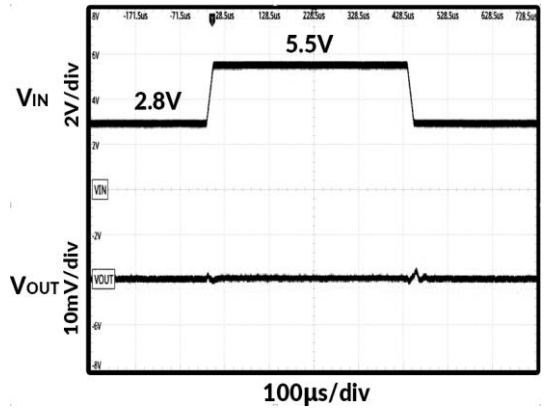


Figure 24. Line Transient Response (I_{OUT}=1mA)

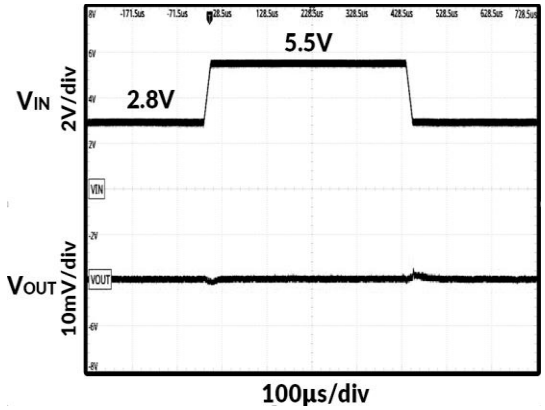


Figure 25. Line Transient Response (I_{OUT}=30mA)

Typical Performance Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

V_{IN} = 2.8V, I_{OUT} = 1mA, C_{IN} = Ceramic 1.0µF, C_{OUT} = Ceramic 1.0µF, unless otherwise noted.

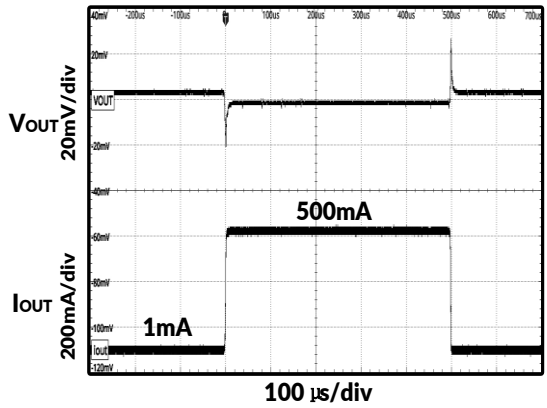


Figure 26. Load Transient Response

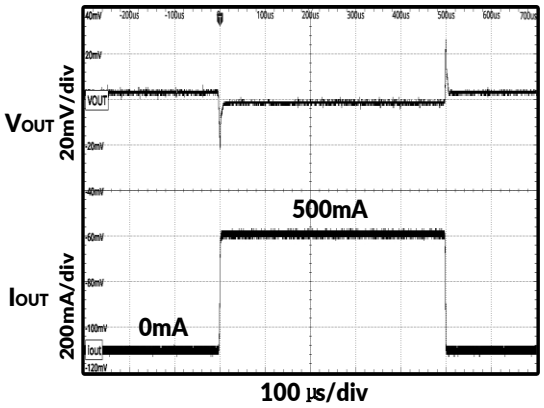


Figure 27. Load Transient Response

9 FEATURE DESCRIPTION

9.1 Overview

The RS3217F is a low-noise LDO that can supply up to 500mA output current. Designed to meet the requirements of RF and analog circuits, the RS3217F device provides low noise, high PSRR, low quiescent current, and low line or load transient response figures.

RS3217F is stable with a 1.0μF ceramic input and output capacitor, Using the new innovative design techniques, the RS3217F offers class-leading noise performance without a noise bypass capacitor。

RS3217F is available with fixed output voltages from 1.2V to 4.2V.

9.2 Shutdown

Enable input. A low voltage (< V_{IL}) on this pin turns the regulator off and discharges the output pin to GND through an internal pulldown resistor. A high voltage (> V_{IH}) on this pin enables the regulator output. The EN pin can be connected to the IN pin if not used. Do not leave floating.

9.3 Output Automatic Discharge

The RS3217F output employs an internal 75Ω (typical) pulldown resistance to discharge the output when the EN pin is low, and the device is disabled.

9.4 Thermal Overload Protection (T_{SD})

Thermal shutdown disables the output when the junction temperature rises to approximately 165°C which allows the device to cool. When the junction temperature cools to approximately 135°C, the output circuitry enables.

Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the RS3217F has been designed to protect against temporary thermal overload conditions. The T_{SD} circuitry was not intended to replace proper heat-sinking. Continuously running the RS3217F device into thermal shutdown may degrade device reliability.

9.5 Current-Limit Protection

The RS3217F monitors the current flowing through the output PMOS and limits the maximum current to prevent load and RS3217F from damages during current overload conditions.

9.6 Short Current-Limit Protection

The short current-limit function reduces the current-limit level down to 105mA(typical) during short circuit conditions.

10 TYPICAL APPLICATION

10.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, connecting a 1μF low-equivalent series resistance (ESR) capacitor across the input supply near the regulator is good analog design practice. This capacitor counteracts reactive input sources and improves transient response and ripple rejection. A higher value capacitor can be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the power source.

The RS3217F family of devices is designed to be stable with standard ceramic output capacitors of values 1μF or larger. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature.

11 POWER SUPPLY RECOMMENDATIONS

The device is designed to operate from an input voltage supply range between 1.9V and 5.5V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise.

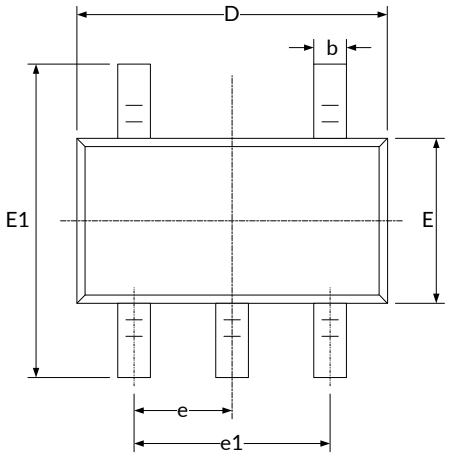
12 LAYOUT

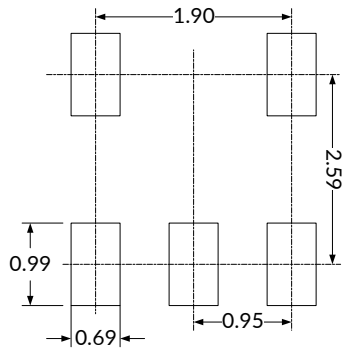
For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO component connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the printed circuit board (PCB) itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shields the LDO from noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the exposed thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

To improve ac performance (such as PSRR, output noise, and transient response), designing the board with separate ground planes for V_{IN} and V_{OUT} is recommended, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

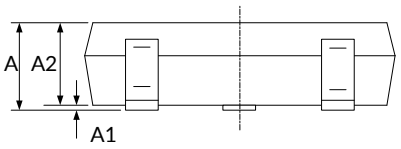
13 PACKAGE OUTLINE DIMENSIONS

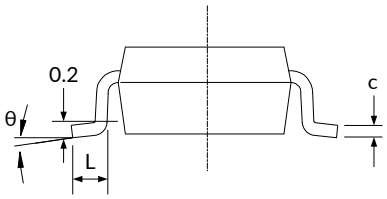
SOT23-5 (3)





RECOMMENDED LAND PATTERN (Unit: mm)



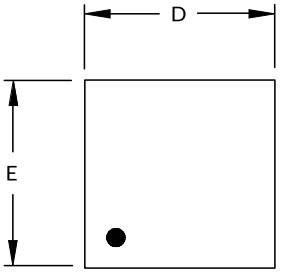


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D (1)	2.820	3.020	0.111	0.119
E (1)	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC) (2)		0.037(BSC) (2)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

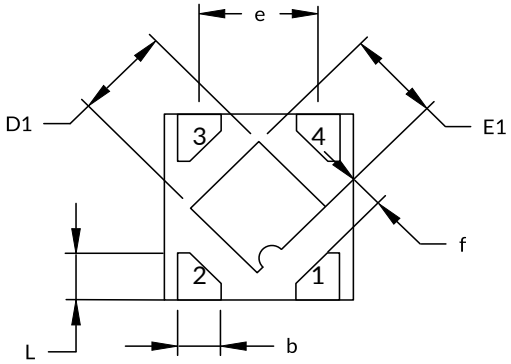
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

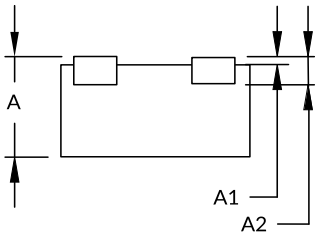
XDFN1X1-4 (3)



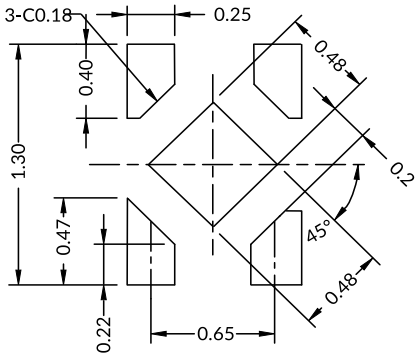
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

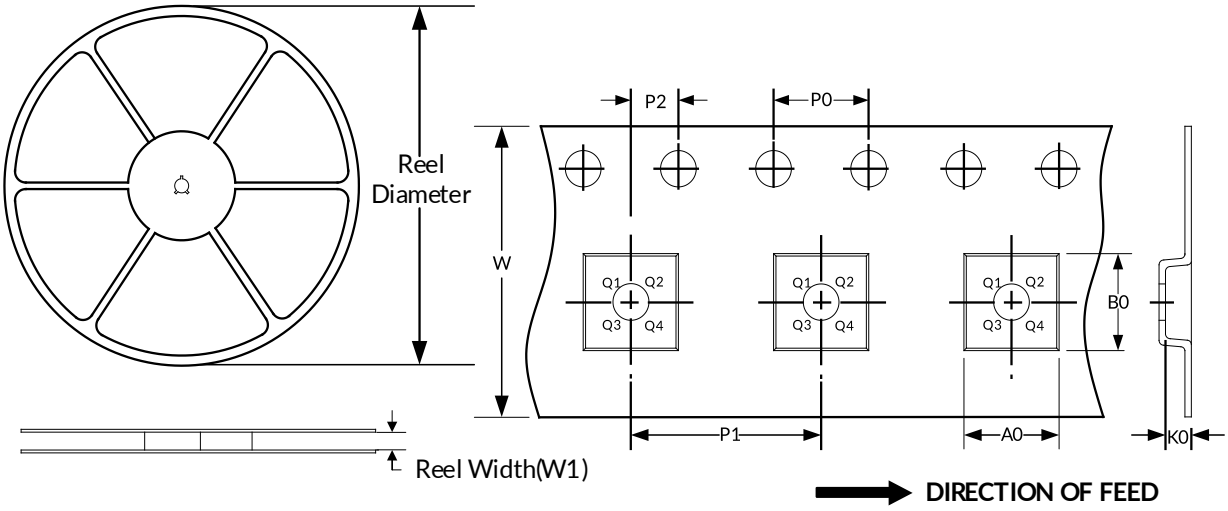
Symbol	Dimensions In Millimeters			Dimensions In Inches		
	MIN	TYP	MAX	MIN	TYP	MAX
A (1)	0.340	0.370	0.400	0.013	0.015	0.016
A1	0.000	0.020	0.050	0.000	0.001	0.002
A2	0.100 REF (2)			0.004 REF (2)		
D (1)	0.950	1.000	1.050	0.037	0.039	0.041
D1	0.430	0.480	0.530	0.017	0.019	0.021
E (1)	0.950	1.000	1.050	0.037	0.039	0.041
E1	0.430	0.480	0.530	0.017	0.019	0.021
b	0.170	0.220	0.270	0.007	0.009	0.011
e	0.600	0.650	0.700	0.024	0.026	0.028
f	0.195 REF (2)			0.008 REF (2)		
L	0.200	0.250	0.300	0.008	0.010	0.012

NOTE:

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. This drawing is subject to change without notice.

14 TAPE AND REEL INFORMATION

REEL DIMENSIONS **TAPE DIMENSION**



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-5	7”	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
XDFN1X1-4	7”	9.5	1.16	1.16	0.5	4.0	4.0	2.0	8.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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