WLCSP 24ball OCTAL SPI PSRAM PCB Layout Guidelines

Introduction

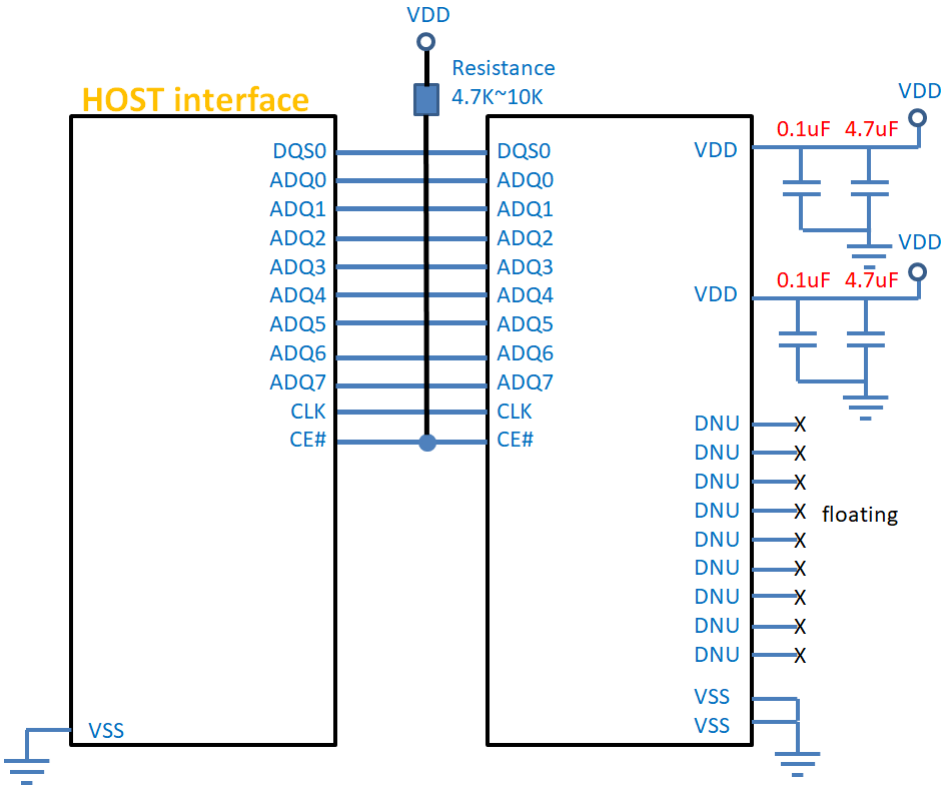
This document provides the information of APM's PSRAM WLCSP 24ball packages, suggested PCB land patterns, layout guide and power supply decoupling notice.

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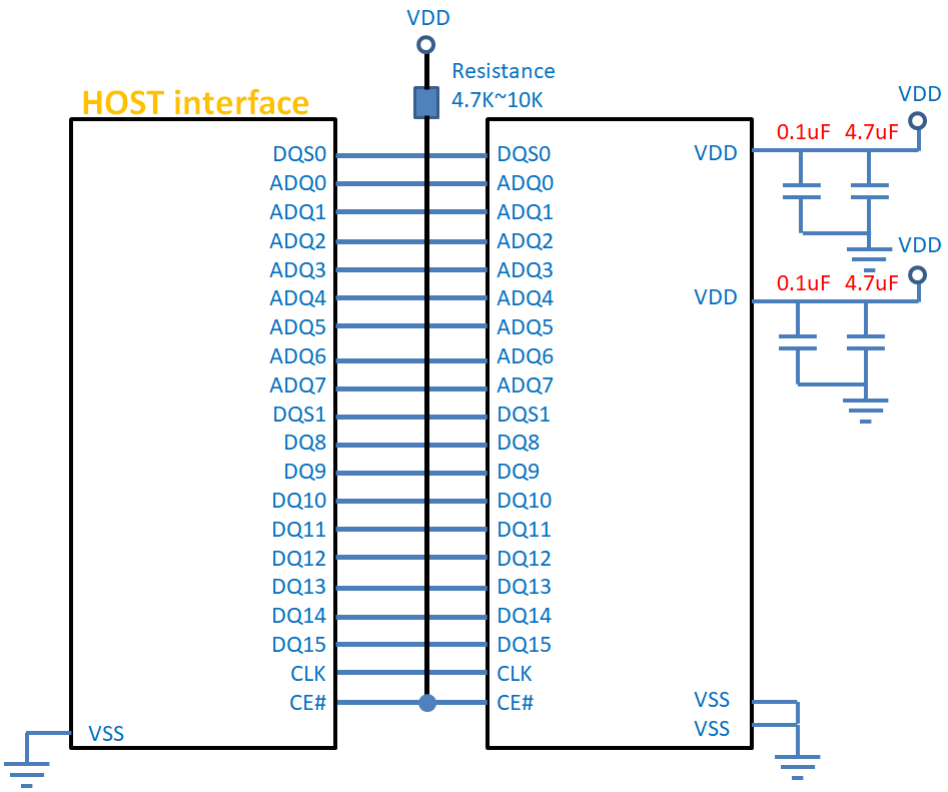
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1 Block diagram and reference circuits



WLCSP 24ball(X8)

Fig. 1.1



WLCSP 24ball(X16)

Fig. 1.2

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2 Package outline and Land Pattern

2.1 WLCSP 24ball, package code WA

Packages for WLCSP 24ball:

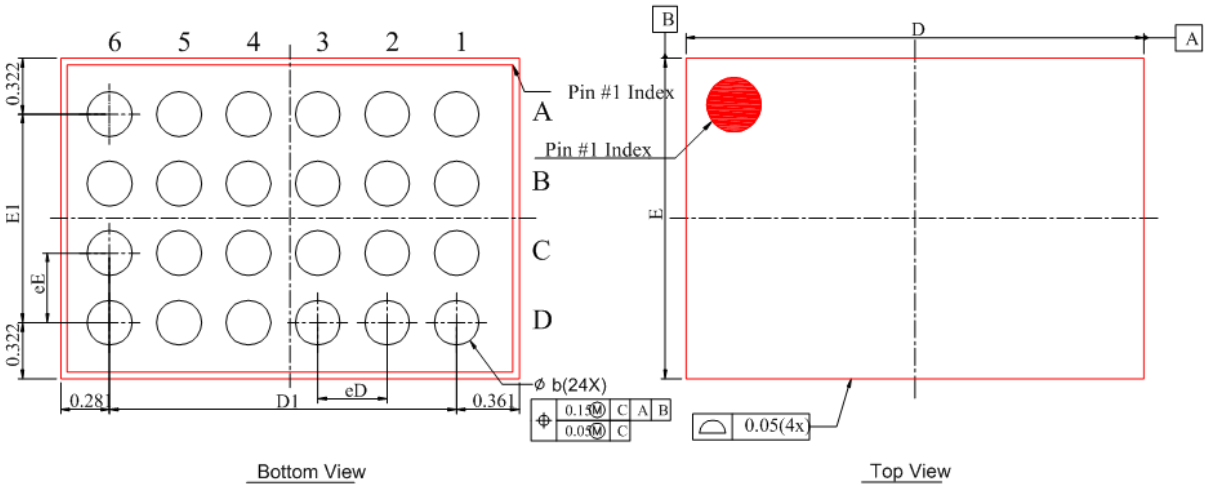


Fig. 2.1 a

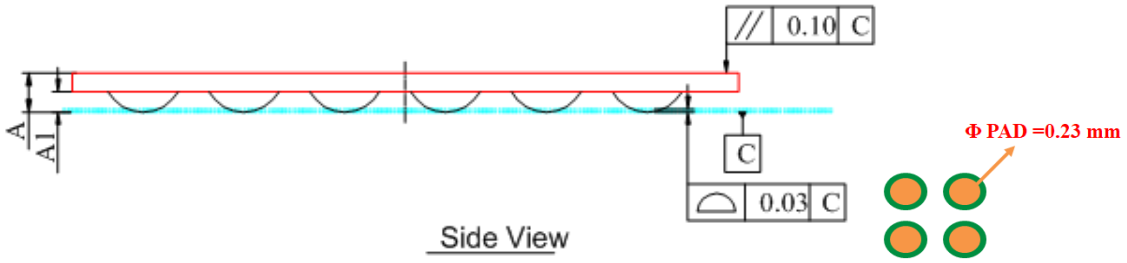


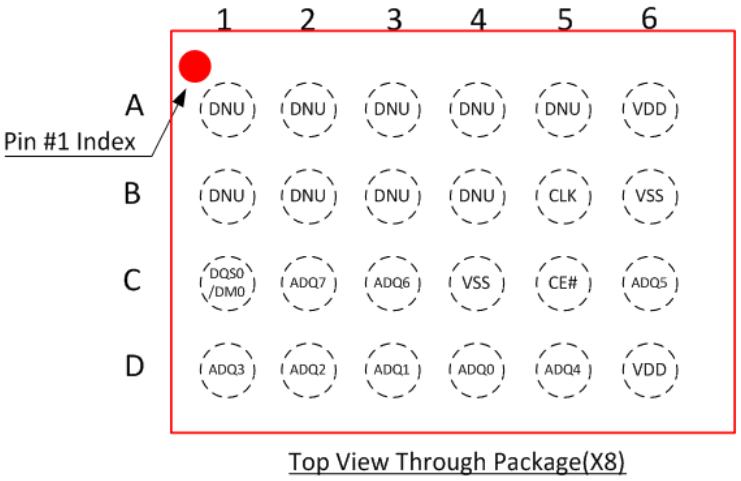
Fig. 2.1 b

Symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	0.511	---
A1	---	0.211	---
D	2.568	---	2.642
D1	2.0 BSC		
E	1.770	---	1.844
E1	1.2 BSC		
b	---	0.258	---
eD	0.4 BSC		
eE	0.4 BSC		

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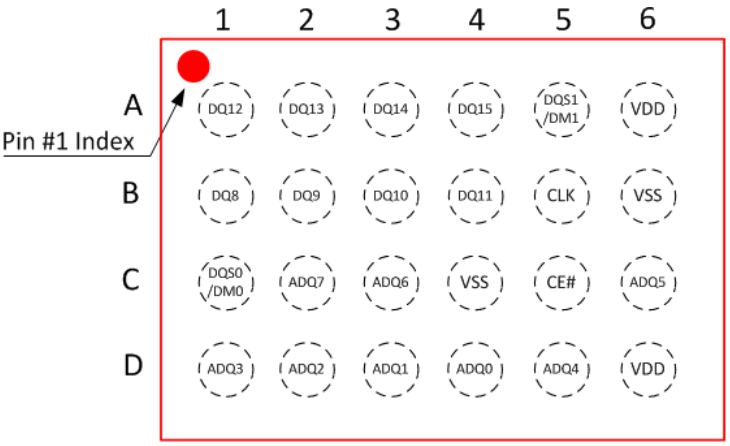
3 Signal group

3.1 Pin Location



Top View Through Package(X8)

Fig. 3.1



Top View Through Package(X16)

Fig. 3.2

3.2 Signals Table

Symbol	***Type***	***Description***	***Comments***
V_{DD}	Power	Core & IO supply 1.8V.	V_{DDQ} short to V_{DD} internally.
V_{SS}	Ground	Core& IO supply ground.	
A/DQ[7:0]	IO	Address/Data bus [7:0].	Used in X8 and X16.
DQ[15:8]	IO	Data bus [15:8].	Used in X16 only.
DQS/DM<0>	IO	DQ strobe clock for DQ[7:0] during all reads, Data mask for DQ[7:0] during memory writes. DM is active high. DM=1 means “do not write”.	Used in X8 and X16.
DQS/DM<1>	IO	DQ strobe clock for DQ[15:8] during memory reads, Data mask for DQ[15:8] during memory writes. DM is active high. DM=1 means “do not write”.	Used in X16 only.
CE#	Input	Chip select, active low. When CE#=1, chip is in standby state.	
CLK	Input	Input clock.	

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4 Layout Guidelines and Recommendation

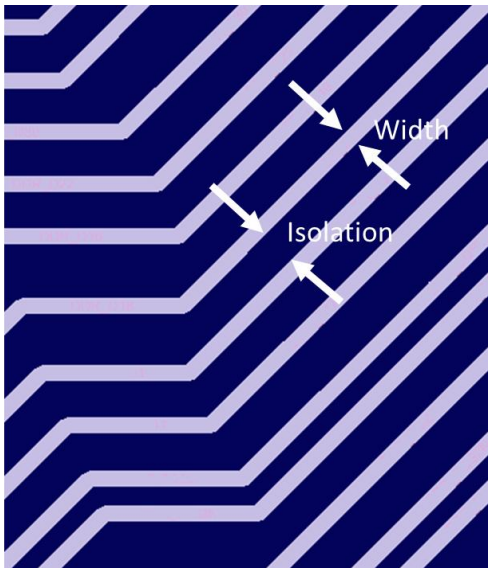
- There are two structures applied to route signal trace, microstrip line and strip line are included

Structure	Description	Note
Microstrip line	1. The thick (H) of dielectric is similar to the width (W) of signal trace. 2. Signal traces are at top or bottom layer. 3. The reference plane is under the signal trace.	4 layers above PCB design
Strip line	1. Signal trace is embedded in dielectric. 2. The ref plane is at up and below layer.	4 layers above PCB design

Summary Trace width, Isolation and Spacing Design table

	Signal	Position	Width (PCB/BGA)	Isolation (PCB/BGA)
Microstrip	A/DQ[7:0],DQ[15:8] DQS/DM<0>,DQS/DM<1> CE#,CLK	Top /Bottom	5/4 mil	>10 / 4 mil
Strip line		Inner	4 mil	>8 / 4 mil

- **The same signal group is recommended to arrange at the same layer**.
- If BGA area space is limited,mini rule of width and isolation can be changed to 4 mil
- Detail design descriptions are shown as below chapter.
-

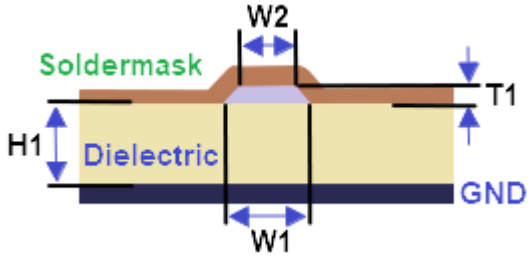


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4.1 Signal trace on 4-layer above PCBA Design

4.1.1 Top/Bottom layer: Microstrip

- The reference plane is under the signal trace, be known as microstrip line.
- H1 is approaching W1
- Signal-ended trace on 4-layers-above PCBA: impedance design is about 50~60 ohms



	Er1	FR4 (~4.2)
Thickness	H1	4 – 5 mil
Trace Width	W1	5 mil
Tuned width	W2	Reserved*

* Reserved for impedance tuning

Fig. 4.1.1 a

Trace	Layer	Width (PCB/BGA)	Isolation (PCB/BGA)	Reference plane
A/DQ[7:0],DQ[15:8] DQS/DM<0>,DQS/DM<1> CE#,CLK	Top & Bot	5 / 4 mil	>10 / 4 mil	GND

- Trace Width is recommended 5 mil and isolation is > 2 x W1 (~10mil)at least.
- If BGA area space is limited,mini rule of width and isolation can be changed to 4mil

PCB area Top view

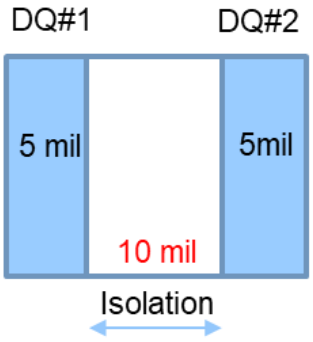


Fig. 4.1.1 b

BGA area Top view

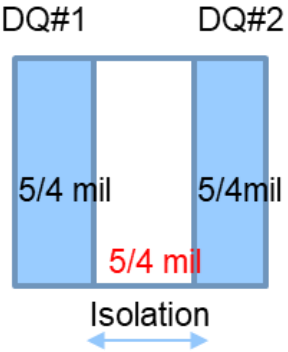
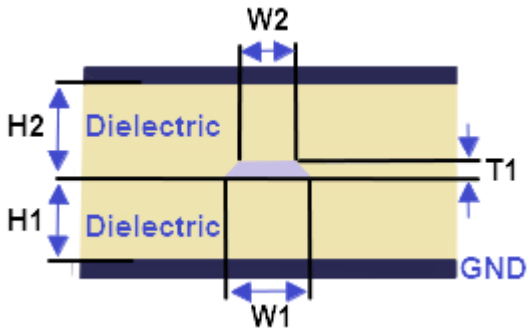


Fig. 4.1.1 c

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4.1.2 Inner layer: Strip line

- The reference plane is at the top and bottom layer of signal trace, be known as strip line.



	Er1	FR4 (~4.2)
Thickness 1	H1	4 – 5 mil
Thickness 2	H2	8 – 10 mil
Trace Width	W1	4 mil
Tuned width	W2	Reserved*

* Reserved for impedance tuning

Fig. 4.1.2 a

Trace	Layer	Width (PCB/BGA)	Isolation (PCB/BGA)	Reference plane
A/DQ[7:0],DQ[15:8] DQS/DM<0>,DQS/DM<1> CE#,CLK	Inner	4 mil	>8 / 4 mil	GND

- Trace Width is recommended 4 mil and isolation is > 2 x W1 (8 mil) at least.
- If BGA area space is limited,mini rule of width and isolation can be changed to 4mil.

PCB area Top view

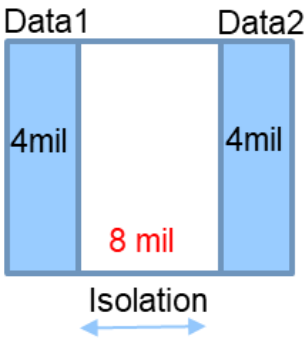


Fig. 4.1.2 b

BGA area Top view

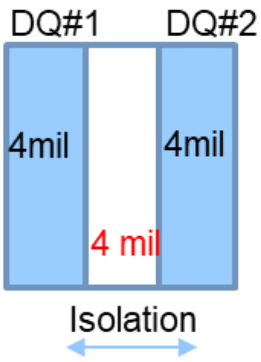


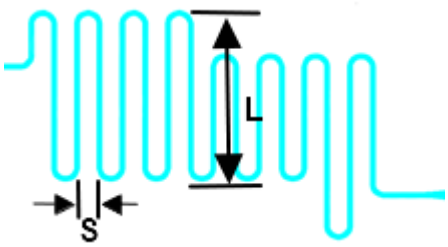
Fig. 4.1.2 c

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4.2 Routing recommendation

Signal Routing

- Signal traces are recommended to route at the same layer.
- Keep traces as straight as possible.
- Avoid big turn and long serpentine routing when need to tune trace length.
- If ‘ S ’ is small and ‘ L ’ is long ,the coupling and self-interference would affect signal integrity.



Worst

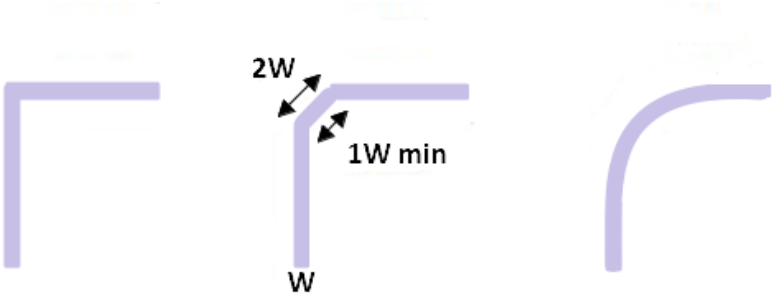
Fig. 4.2 a



Better

Fig. 4.2 b

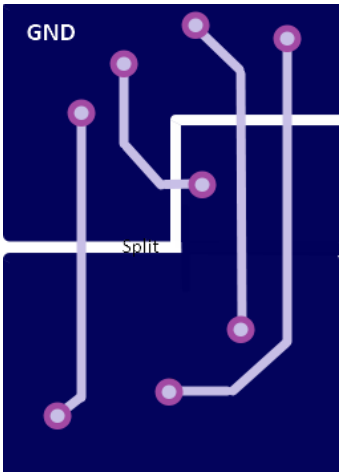
- Avoid routing traces with 90° angle corners.
  - Cut the corner (angle = 45°) or smooth the trace when a trace route needs to change direction.



Worst Better Best

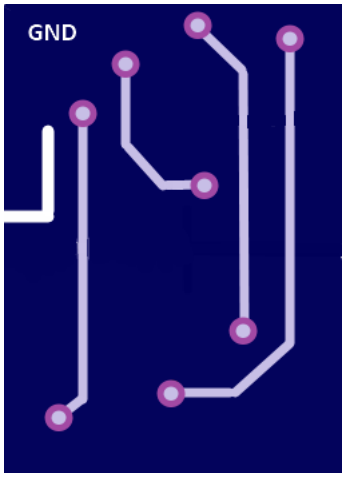
Fig. 4.2 c

- Microstrip line don’t cross split or void plane
  - All signal traces should have a continuous reference plane.



Worst

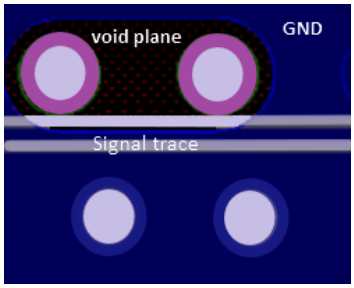
Fig. 4.2 d



Better

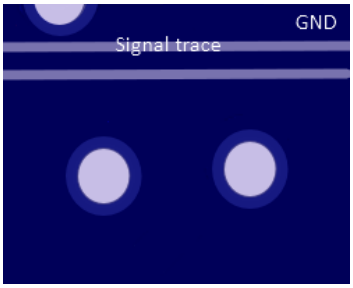
Fig. 4.2 e

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Worst

Fig. 4.2 f



Better

Fig. 4.2 g

- Add a reference via around signal via when signal change to the other layer.
  - Create current return path for signal via.
  - 4-layers example

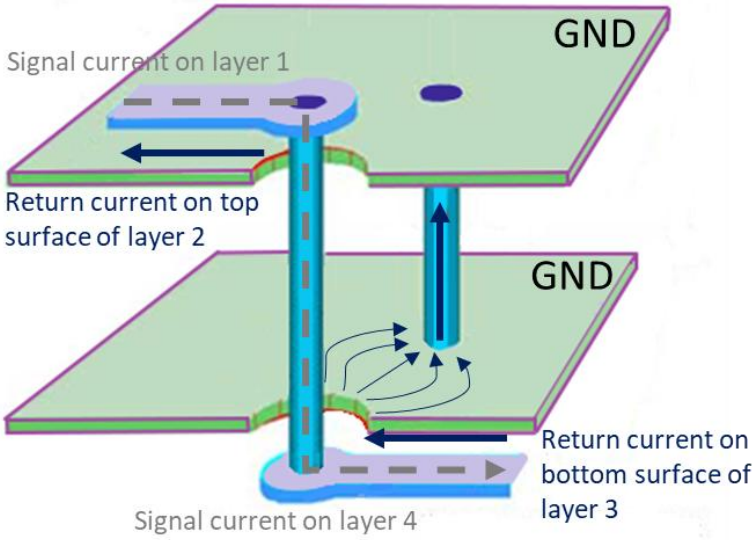


Fig. 4.2 h

Keep the isolation when traces change direction

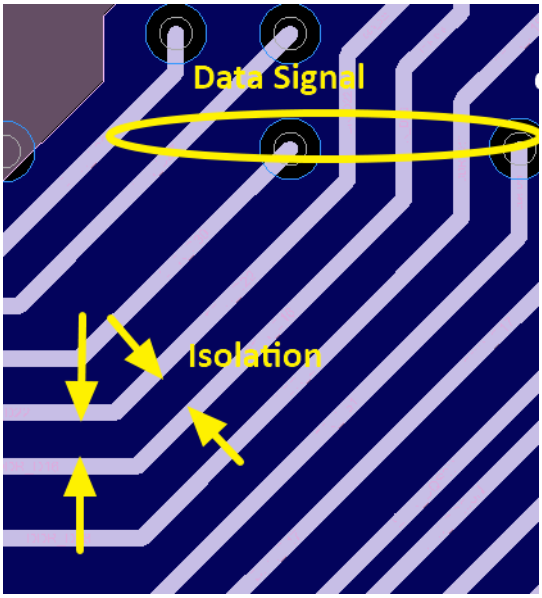


Fig. 4.2 i

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4.3 Length skew and tuning

Length difference @ 3% phase skew

Operation Frequency	200MHz	Note
Period	5ns	1 / 200MHz
Skew from length difference	<150ps	= 5ns x **3%**
Length difference	**< 22.4 mm**	= 150ps(Skew) / 6.7ps (1mm = 6.7ps)

- The time delay of 1mm microstrip line at FR4 is about 6.7 ps
- It is better to tuning trace length when the same signal group trace difference is large.

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5 Power supply decoupling

- De-capacitor is placed between VDD pin and power via, de-cap is close to VDD pin.
- GND via is nearby VSS pin.
- De-capacitors would be required with low ESR capacitor 4.7uF and 0.1uF at least.
- If customer needs half-sleep feature support, its refresh current peaks are large , a 4.7uF or 10uF low ESR capacitor must be installed to ensure power supply integrity.
- Place the lowest valued capacitor as close as possible to the power pin/power trace of the device to minimize the inductive influence of the trace.

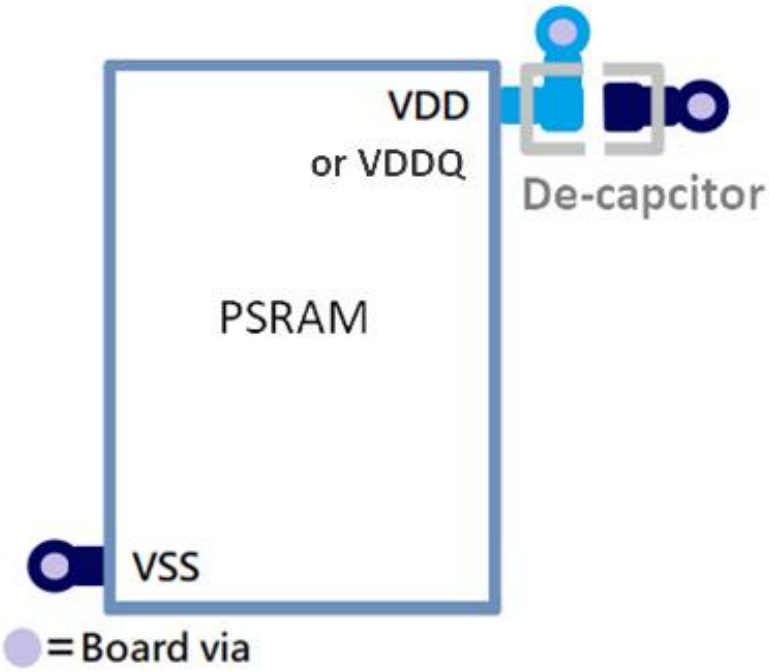


Fig. 5 a

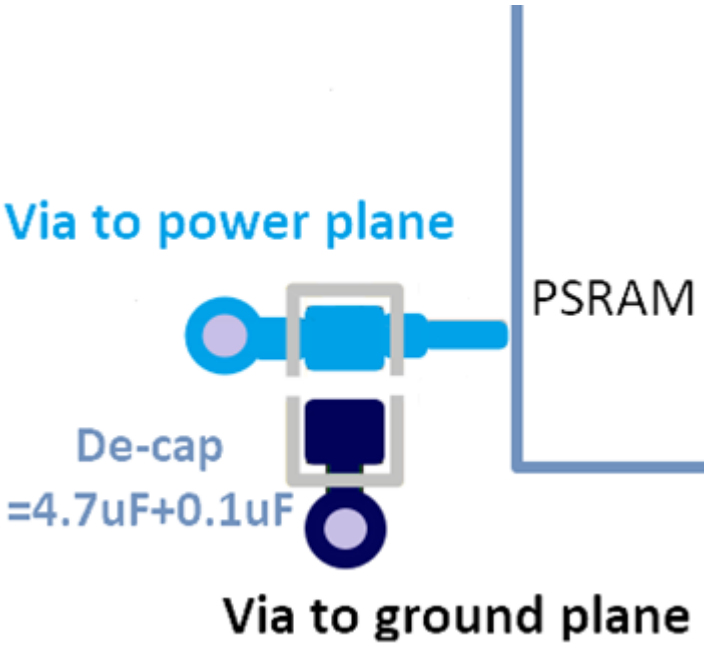
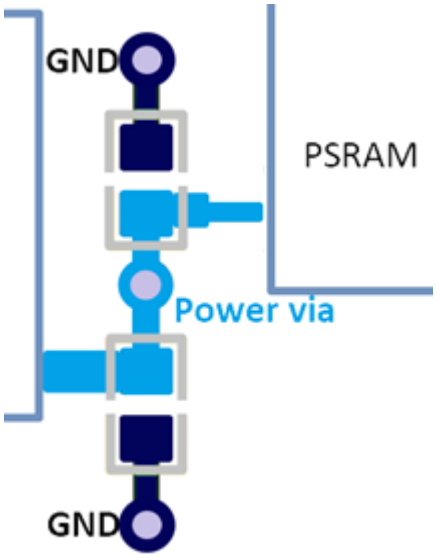


Fig. 5 b

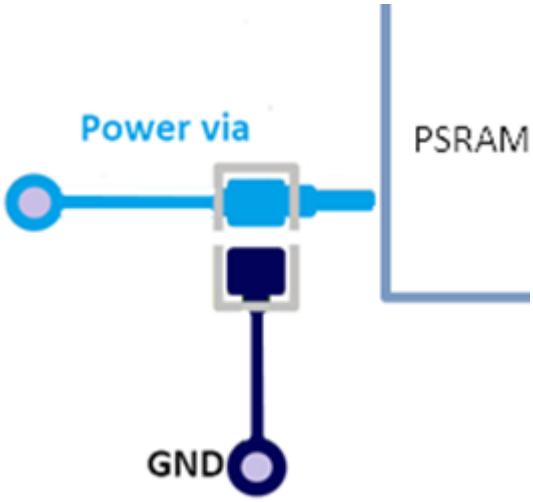
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- Keep power trace width wide and trace lengths short from the package pads to the vias.
- Avoid sharing the same via with two or more decoupling capacitors.



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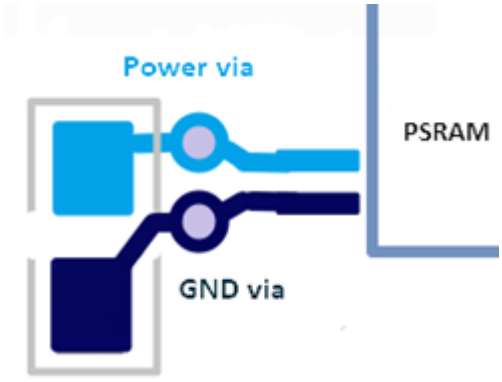
Fig. 5 c avoide sharing the same via.



Worst

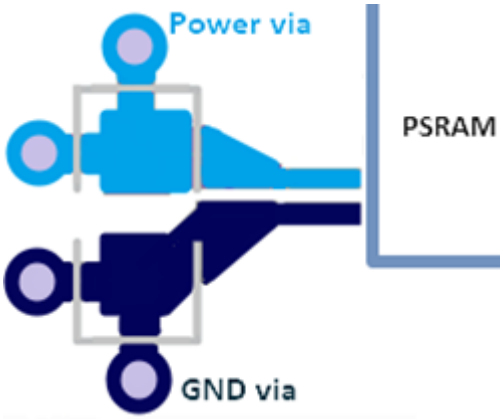
Fig. 5 d avoid Power and GND trace too thin and long.

- Provide appropriate Power via and GND via.
- Use two or three vias to get a low-impedance and inductance connection .
- De-couple capacitor need to be placed on the current flow path.



Worst

Fig. 5 e capacitor is not on the current path,the effect of de-couple capacitor will be decresed.



Better

Fig. 5 f good connection for Low-impedance and Low inductance.

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5.1 WLCSP_24B

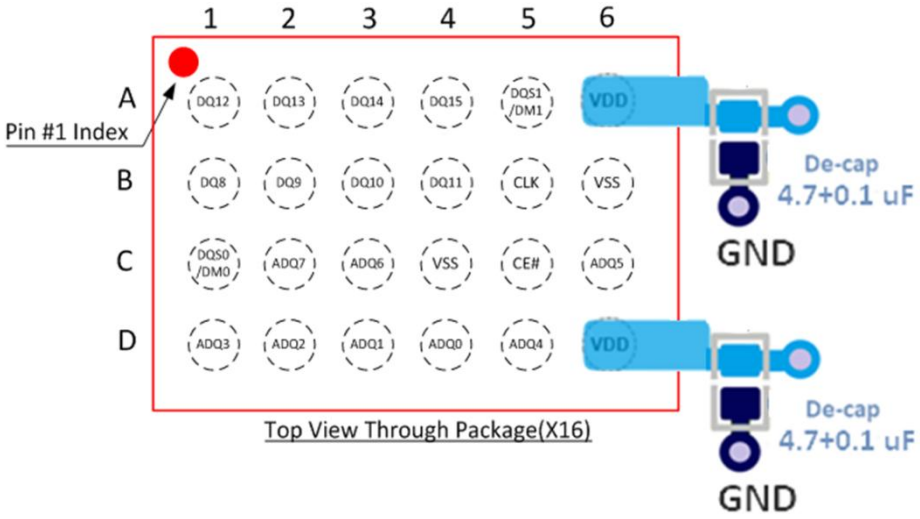


Fig. 5 e

6 Layout Check list

Item	Description	Y/N
1	The clearance of two adjacent signals is 2times of trace width at least	
2	The same signal group is recommended to arrange at the same layer	
3	Symmetric drawing for DQS/CLK differential trace	
4	Tuning trace length when the same signal group trace difference is large	
5	Keep traces as straight as possible.	
6	Avoid big turn and long serpentine routing when need to tune trace length.	
7	Avoid routing traces with 90° angle corners.	
8	Avoid signal trace no reference plane, crossing split or void plane in microstrip line design.	
9	Signal traces always have continuous reference plane.	
10	Add reference via around signal via when signal changes to another layer.	
11	Keep the isolation and Spacing when traces change direction	
12	De-capacitor must be placed close to VDD pin.	
13	Add GND via nearby VSS pin is required	
14	De-capacitors would be required with 4.7uF and 0.1uF at least.	
15	Place the lowest valued capacitor as close as possible to the power pin of the PSRAM	
16	Keep power trace width wide.	
17	Keep power trace lengths short from the package pads to the vias.	
18	Avoid sharing the same via with two or more decoupling capacitors.	
19	Avoid Power and GND trace too thin and long.	
20	De-capacitor must be placed on the current flow path (see Fig. 5 f).	

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Change History			
Rev.#	Who	When	What
1.0	Jacky	2020-02-06	First version of WLCSP OCTAL SPI PSRAM layout guide is released

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