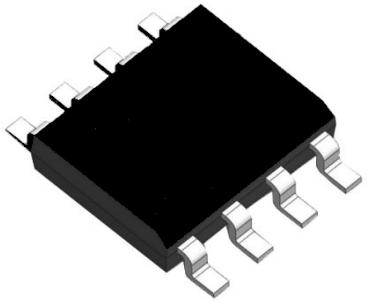
FEATURES

- Fully compatible with the ISO 11898 standard
- Thermally protected
- Input levels compatible with 3.3 V and 5 V devices
- Transmit Data (TXD) dominant time-out function
- Very low-current standby mode with remote wake-up Capability via the bus: 5μA Typical
- Transceiver in unpowered state disengages from the bus (zero load)
- At least 110 nodes can be connected
- High speed (up to 1 MBaud)
- Very low Electro Magnetic Emission (EME)
- Provide DFN3*3-8，Small Outline，Leadless Package



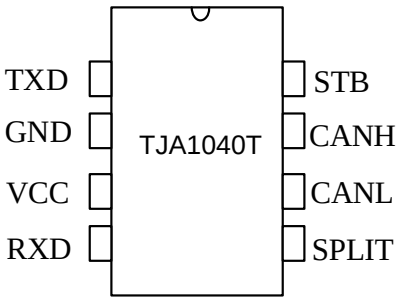
SOP-8

DESCRIPTION

The TJA1040 is the interface between the Controller Area Network (CAN) protocol controller and the physical bus. It is primarily intended for high-speed applications, up to 1 MBaud, in in-vehicle, industry control and other fields. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller.

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Supply voltage	V_{cc}		4.5	5.5	V
Maximum transmission rate	$1/t_{bit}$	Non-return to zero code	1		Mbaud
CANH/CANL input or output voltage	V_{can}		-40	+40	V
Bus differential voltage	V_{diff}		1.5	3.0	V
Ambient temperature	T_{amb}		-40	125	℃
ESD	Vesd	HBM	±8		kV

PIN CONFIGURATION



PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	TXD	transmit data input
2	GND	ground supply
3	VCC	supply voltage
4	RXD	receive data output; reads out data from the bus lines
5	SPLIT	common-mode stabilization output
6	CANL	LOW-level CAN bus line
7	CANH	HIGH-level CAN bus line
8	STB	standby mode control input

LIMITING VALUES

PARAMETER	SYMBOL	VALUE	UNIT
Supply voltage	V_{CC}	-0.3~+6	V
DC voltage on TXD/RXD/STB pins	TXD, RXD, STB	-0.3~VCC+0.3	V
Voltage range at any bus terminal (CANH, CANL, SPLIT)	CANL, CANH, SPLIT	-40~40	V
Transient voltage on pins CANH, CANL and SPLIT see Fig.7	V_{tr}	-200~+200	V
Storage temperature	T_{stg}	-55~150	℃
Ambient temperature	T_{amb}	-40~125	℃
Virtual junction temperature	T_j	-40~150	℃
Welding temperature range		300	℃

DRIVER ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
CANH dominant output voltage	$V_{OH(D)}$	VI=0V, STB=0V, RL=60Ω, Fig.1, Fig.2	2.75	3.5	4.5	V
CANL dominant output voltage	$V_{OL(D)}$		0.5	1.5	2.25	V
Bus recessive output voltage	$V_{O(R)}$	VI=3V, STB=0V, RL=60Ω, Fig.1, Fig.2	2	2.5	3	V
Bus dominant differential output voltage	$V_{OD(D)}$	VI=0V, STB=0V, RL=60Ω, Fig.1, Fig.2	1.5		3	V
Bus recessive differential output voltage	$V_{OD(R)}$	VI=3V, S=0V, Fig.1, Fig.2	-0.012		0.012	V
		VI=3V, STB=0V, NO LOAD	-0. 5		0.05	V
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	$V_{dom(TX)sym}=V_{CC}-V_{CANH}-V_{CANL}$	-400		400	mV
Transmitter voltage symmetry	V_{TXsym}	$V_{TXsym}=V_{CANH}+V_{CANL}$	$0.9V_{CC}$		$1.1V_{CC}$	V
Common-mode output voltage	V_{OC}	STB=0V, Fig.8	2	2.5	3	V
Peak-to-peak Common-mode output voltage	$\triangle V_{OC}$			30		mV
Short-circuit output current	I_{OS}	CANH=-12V, CANL=open, Fig.11	-105	-72		mA
		CANH=12V, CANL=open, Fig.11		0.36	1	mA
		CANL=-12V, CANH=open, Fig.11	-1	0.5		mA
		CANL=12V, CANH=open, Fig.11		71	105	mA
Recessive output current	$I_{O(R)}$	-27V<CANH<32V 0<VCC<5.25V	-2.0		2.5	mA

(V_{CC}=5V±10% and -40°C ≤ T_j ≤ 150°C unless specified otherwise; typical in V_{CC}=+5V and T_{amb}=25°C)

DRIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation delay time, low-to-high-level output	t_{PLH}	STB=0V, Fig.4	25	65	120	ns
Propagation delay time, low-to-high-level output	t_{PHL}		25	45	90	ns
Differential output signal rise time	t_r			25		ns
Differential output signal fall time	t_f			50		ns
Enable time from standby mode to dominant	t_{EN}	Fig.7			10	µs
Bus dominant time-out time	t_{dom}	Fig.10	300	450	700	µs
Bus wake-up filter time	t_{BUS}		0.7		5	µs

(V_{CC}=5V±10% and -40°C ≤ T_j ≤ 150°C unless specified otherwise; typical in V_{CC}=+5V and T_{amb}=25°C)

RECEIVER ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Positive-going input threshold voltage	V_{IT+}	STB=0V, Fig.5		800	900	mV
Negative-going input threshold voltage	V_{IT-}		500	650		mV
Hysteresis voltage (VIT+ – VIT–)	V_{HYS}		100	125		mV
High-level output voltage	V_{OH}	IO=-2mA, Fig.6	4	4.6		V
Low-level output voltage	V_{OL}	IO=2mA, Fig.6		0.2	0.4	V
Power-off bus input current	$I_{(OFF)}$	CANH or CANL=5V, Other pin=0V			5	µA
Input capacitance to ground, (CANH or CANL)	C_I			13		pF
Differential input capacitance	C_{ID}			5		pF

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Input resistance, (CANH or CANL)	R_{IN}	TXD=3V, STB=0V	15	30	40	kΩ
Differential input resistance	R_{ID}		30		80	kΩ
Input resistance matching	RI_{match}	CANH=CANL	-3%		3%	
The range of common-mode voltage	V_{COM}		-12		12	V

(V_{CC}=5V±10% and -40°C ≤ T_j ≤ 150°C unless specified otherwise; typical in V_{CC}=+5V and T_{amb}=25°C)

RECEIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation delay time, high-to-low-level output	t_{PLH}	STB=0V or VCC, Fig.6	60	100	130	ns
Propagation delay time, high-to-low-level output	t_{PHL}		45	70	90	ns
RXD signal rise time	t_r			8		ns
RXD signal fall time	t_f			8		ns

(V_{CC}=5V±10% and -40°C ≤ T_j ≤ 150°C unless specified otherwise; typical in V_{CC}=+5V and T_{amb}=25°C)

DEVICE SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Loop delay1, driver input to receiver output, Recessive to Dominant	$t_{d(LOOP1)}$	STB=0V, Fig.9	90		190	ns
Loop delay 2, driver input to receiver output, Dominant to Recessive	$t_{d(LOOP2)}$		90		190	ns

(V_{CC}=5V±10% and -40°C ≤ T_j ≤ 150°C unless specified otherwise; typical in V_{CC}=+5V and T_{amb}=25°C)

OVER TEMPERATURE PROTECTION

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Shutdown junction temperature	$T_{j(sd)}$			160		°C

TXD-PIN CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input current	I_{IH}(TXD)	VI=VCC	-2		2	μA
LOW-level input current	I_{IL}(TXD)	VI=0	-50		-10	μA
When VCC=0V，current on TXD pin	I_O(off)	VCC=0V，TXD=5V			1	μA
HIGH-level input voltage	V_{IH}		2		VCC+0.3	V
LOW-level input voltage	V_{IL}		-0.3		0.8	V
Open voltage on TXD pin	TXD_O		H			logic

(V_{CC}=5V±10% and -40℃ ≤ T_j ≤ 150℃ unless specified otherwise; typical in V_{CC}=+5V and T_{amb}=25℃)

STB PIN CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input voltage	V_{IH}	S	2.0		VCC+0.3	V
LOW-level input voltage	V_{IL}	S	-0.3		0.8	V
HIGH-level input current	I_{IH}	V_S=VCC		0		μA
LOW-level input current	I_{IL}	V_S=0V	-1	-3	-10	μA

COMMOM-MODE STABILIZATION OUTPUT

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Common-mode stabilization output voltage	V_O	-500μA<I_o<500μA	0.3V_{CC}		0.7V_{CC}	V
Leakage current	$I_{O(stb)}$	STB=2, -12V<V_O<12V	-5		5	μA

(V_{CC}=5V±10% and -40℃ ≤ T_j ≤ 150℃ unless specified otherwise; typical in V_{CC}=+5V and T_{amb}=25℃)

SUPPLY CURRENT

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Standby	I_{CC}	STB=VCC, V_I=VCC		5	12	μA
Dominant		V_I=0V, STB=0V, LOAD=60Ω		50	70	mA
Recessive		V_I=VCC, STB=0V, NO LOAD		6	10	mA

(V_{CC}=5V±10% and -40℃ ≤ T_j ≤ 150℃ unless specified otherwise; typical in V_{CC}=+5V and T_{amb}=25℃)

FUNCTION TABLE

Table1.CAN TRANSCEIVER TRUTH TABLE

V_{CC}	TXD (1)	STB (1)	CANH (1)	CANL (1)	BUS STATE	RXD (1)
4.5V~5.5V	L	L	H	L	Dominate	L
4.5V~5.5V	H or Open	X	0.5V_{CC}	0.5V_{CC}	Recessive	H
4.5V~5.5V	X	H or Open	GND	GND	Recessive	H
0<V_{CC}<4.5V	X	X	0V<V_{CANH}<V_{CC}	0V<V_{CANL}<V_{CC}	Recessive	X

(1) H=high level; L=low level; X=irrelevant

Table 2. RECEIVER FUNCTION TABLE

V_{ID}=CANH-CANL	RXD (1)	Bus State (1)
V_{ID}≥0.9V	L	Dominate
0.5<V_{ID}<0.9V	?	?
V_{ID}≤0.5V	H	Recessive
Open	H	Recessive

(1) H=high-level; L=low-level; ?=uncertain

TEST CIRCUIT

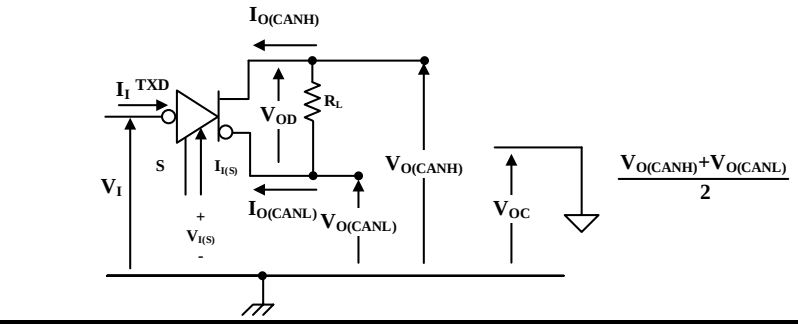


Fig.1 Driver Voltage, Current, and Test Definition

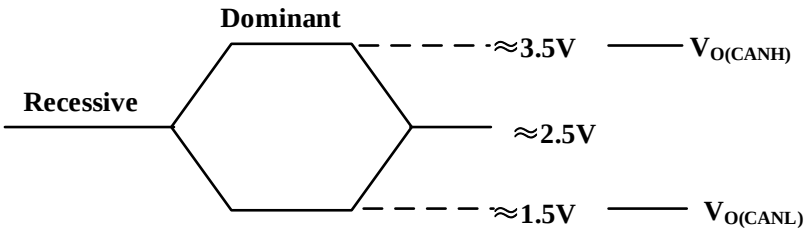


Fig.2 Bus Logic State Voltage Definition

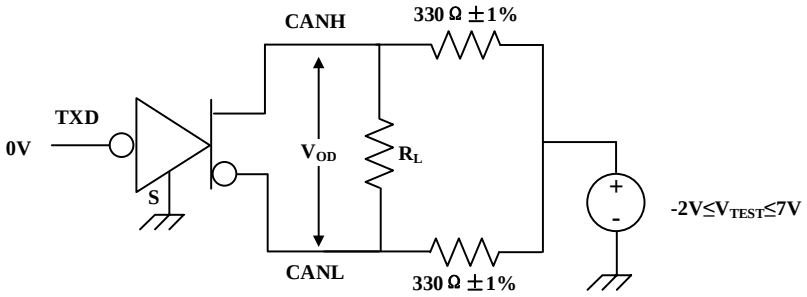


Fig.3 Driver V_{OD} Test Circuit

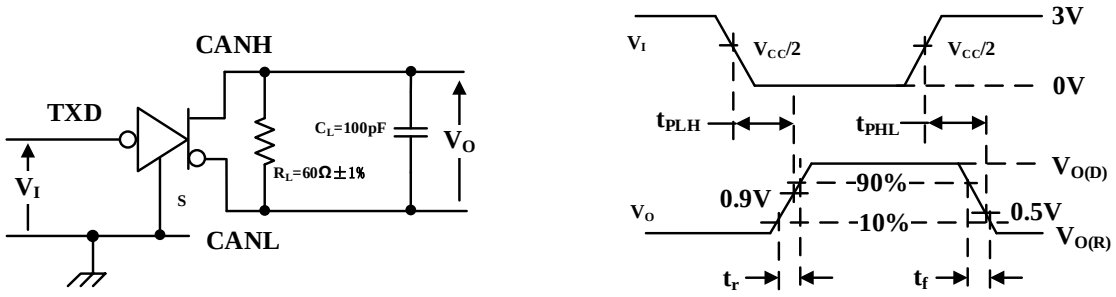


Fig.4 Driver Test Circuit and Waveform

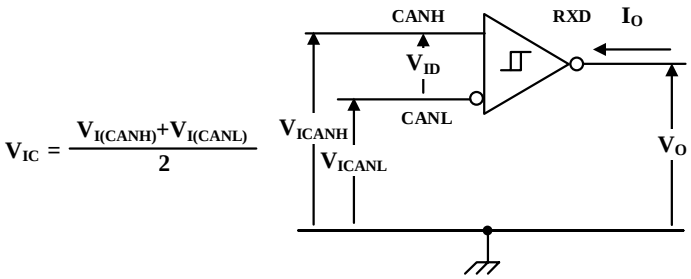
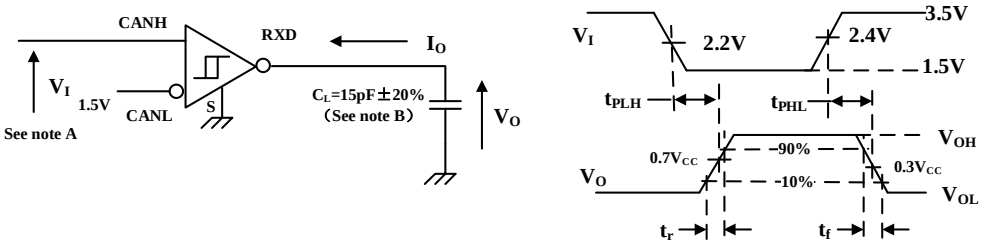


Fig.5 Receiver Voltage and Current Definition



A. The input pulse is supplied by a generator having the following characteristics: PRR≤125kHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ns, Z_O=50Ω.

B. C_L includes instrumentation and fixture capacitance within ±20%.

Fig.6 Receiver Test Circuit and Waveform

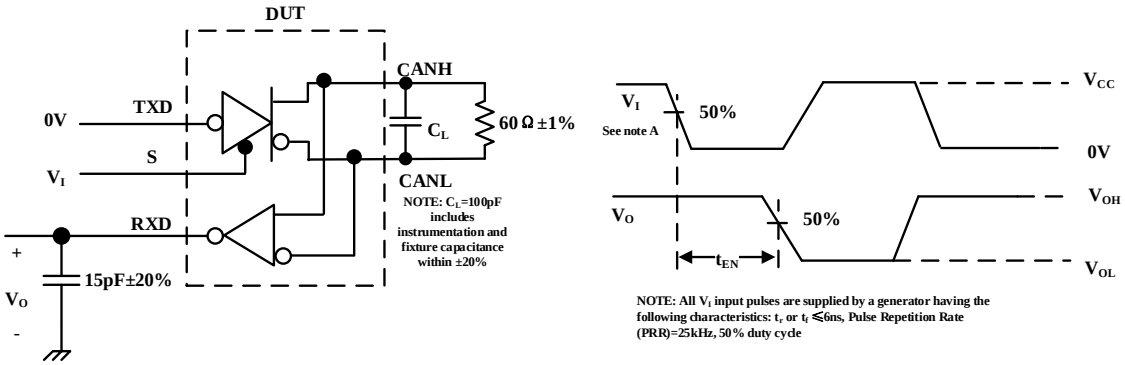
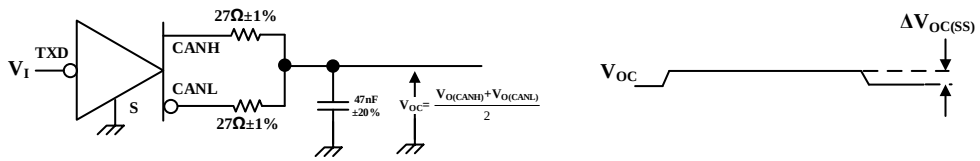


Fig.7 t_{EN} Test Circuit and Waveform



A. All VI input pulses are from 0 V to VCC and supplied by a generator having the following characteristics: t_r or $t_f \leq 6$ns. Pulse Repetition Rate (PRR) =125kHz, 50% duty cycle.

Fig.8 Peak-to-Peak Common Mode Output Voltage Test and Waveform

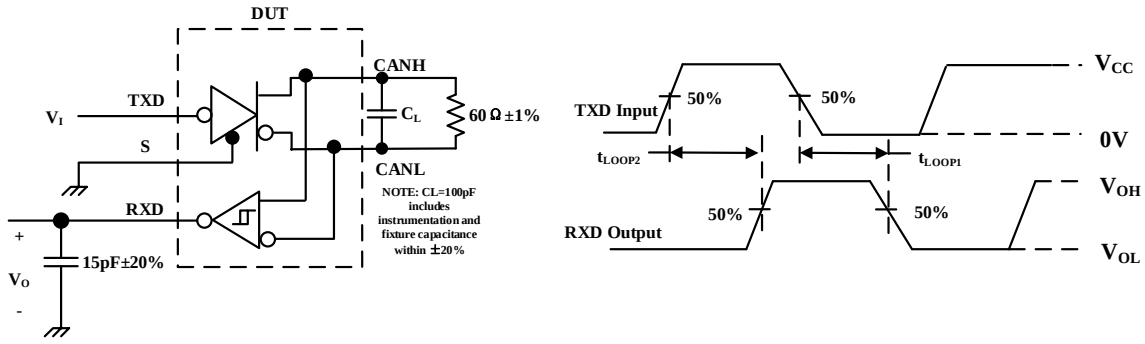


Fig.9 $t_{(LOOP)}$ Test Circuit and Waveform

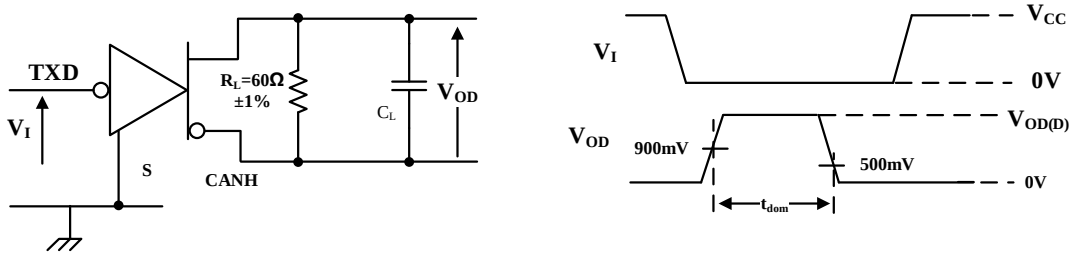


Fig.10 Dominant Time-Out Test Circuit and Waveform

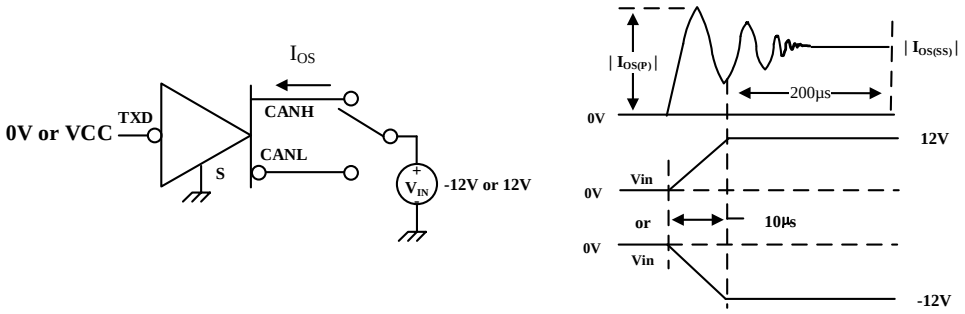


Fig.11 Driver Short-Circuit Current Test Circuit and Waveform

ADDITIONAL DESCRIPTION

1 Sketch

The TJA1040 is the interface between the Controller Area Network (CAN) protocol controller and the physical bus, and can be applied to the fields of in-vehicle and industrial control etc. It is primarily intended for high-speed applications, up to 1 MBaud, in passenger cars. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller, and fully compatible with the ISO 11898 standard.

2 Current protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

3 Fail-safe features

Pin TXD provides a pull-up towards VCC in order to force a recessive level in case pin TXD is unsupplied.
Pin STB provides a pull-up towards VCC in order to force the transceiver into standby mode in case pin STB is unsupplied.
In the case that the VCC is lost, pins TXD, STB and RXD will become floating to prevent reverse supplying conditions via these pins.

4 Over temperature protection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature $T_{j(sd)}$, the output drivers will be disabled until the virtual junction temperature becomes lower than $T_{j(sd)}$ and TXD becomes recessive again.
By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

5 TXD dominant time-out function

A ‘TXD dominant time-out’ timer circuit prevents the bus lines from being driven to a permanent dominant state (blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.
If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{dom}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

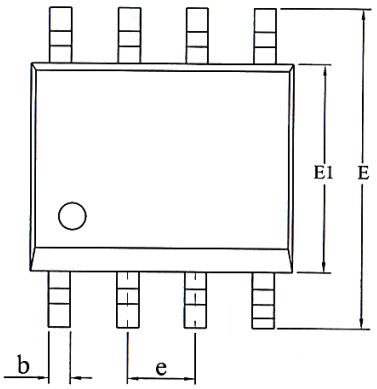
6 Operating modes

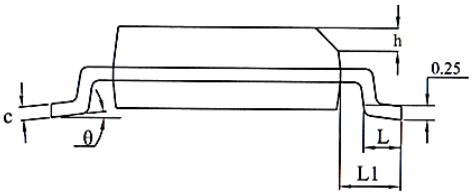
The TJA1040 provides two modes of operation which are selectable via pin STB:
High-speed mode and standby mode.

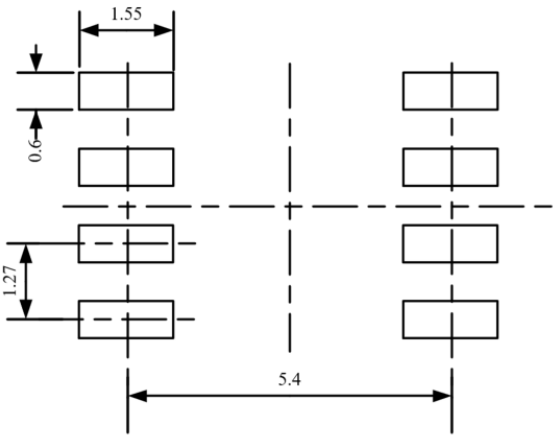
SOP8 DIMENSIONS

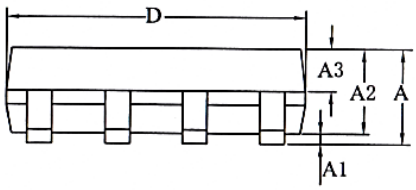
PACKAGE SIZE

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	1.40	-	1.80
A1	0.10	-	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.38	-	0.51
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.40	0.60	0.80
L1	1.05REF		
c	0.20	-	0.25
θ	0°	-	8°







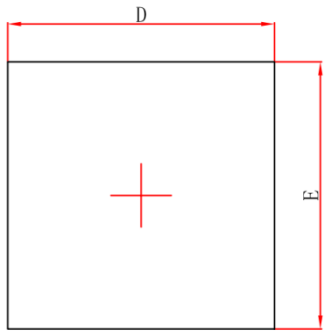


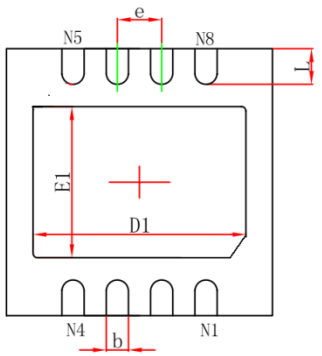
LAND PATTERN EXAMPLE (Unit: mm)

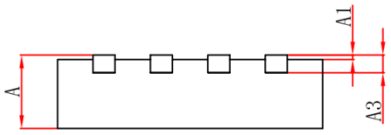
DFN3*3-8 DIMENSIONS

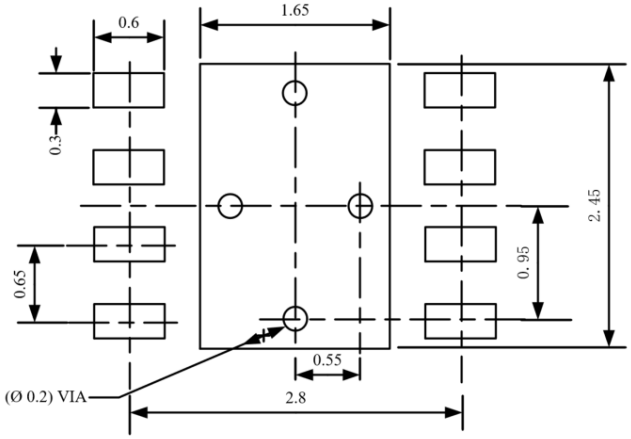
PACKAGE SIZE

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	0.70		0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	2.35	2.3	2.55
E1	1.55	1.65	1.75
b	0.2	0.25	0.33
e	0.65 TYP		
L	0.35		0.45



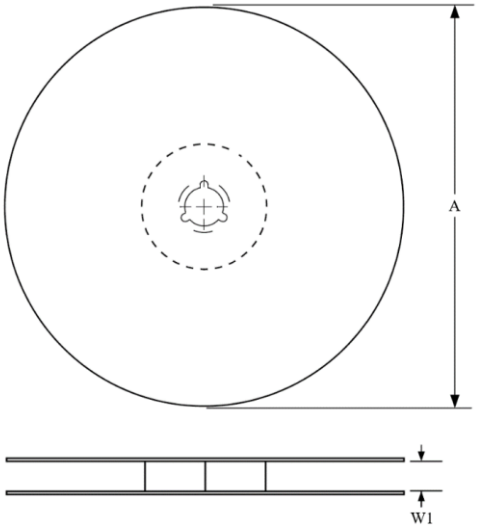




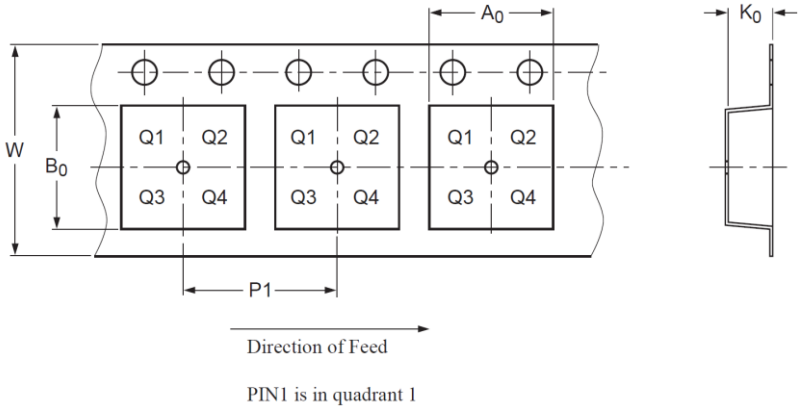


LAND PATTERN EXAMPLE (Unit: mm)

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PIN1 is in quadrant 1

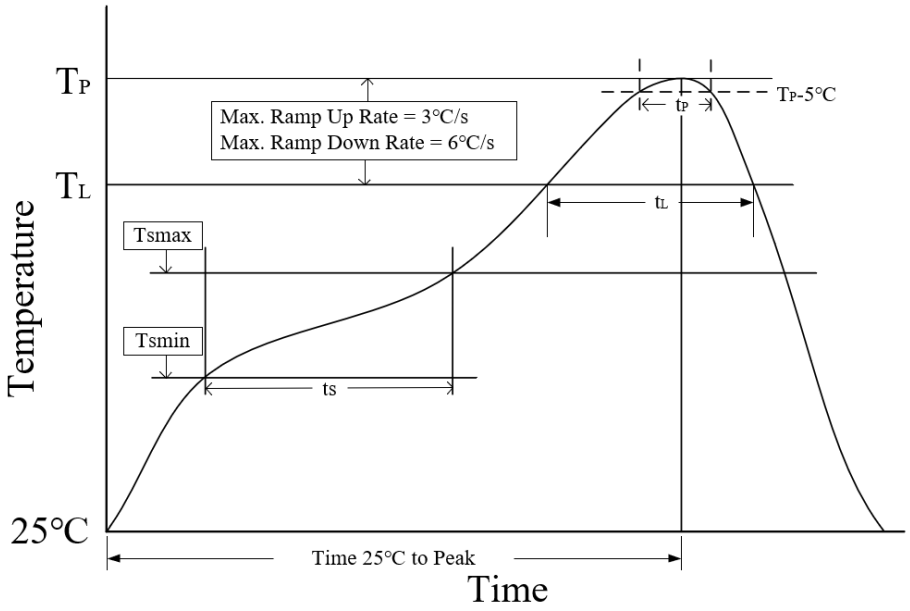
Package Type	Reel Diameter A (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP8	330±1	12.4	6.60±0.1	5.30±0.10	1.90±0.1	8.00±0.1	12.00±0.1
DFN3*3-8	329±1	12.4	3.30±0.1	3.30±0.1	1.10±0.1	8.00±0.1	12.00±0.3

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	PACKING
TJA1040T	SOP8	Tape and reel
TJA1040TK	DFN3*3-8, Small shape, no leads, 8 terminals	Tape and reel

SOP8 package is 2500 pieces/disc. DFN3*3-8 package is 5000 pieces/disc.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L (T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5°C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25°C to peak temperature TP time	8 minutes max