40V Input, 25A GaN Half-Bridge Power Stage

1. Features

- Integrated 4.3mΩ E-mode GaN FETs and driver
- 25A Output Current Capability
- Up to 40V Input Range
- Package optimized for easy PCB Layout
- Integrated BST and V_{CC} capacitors to streamline external components
- Employs internal smart bootstrap circuit to prevent overcharging the bootstrap capacitor
- Single PWM Input with Three PWM Input States: High, Low, and Tri-State
- 4mmx5mmx1.12mm LGA Package

2. Applications

- Half-Bridge and Full-Bridge Converters
- High-Voltage Synchronous DC-DC Converters
- High Frequency, High Power Density Applications
- VCORE and DDR Solutions
- Telecom and Networking Systems

3. Description

The ISG1211 is a 40V Copak product in Innoscience's SolidGaN family. It integrates two 40V enhancement mode GaN devices with a 40V half-bridge gate driver. ISG1211 employs bootstrap technique for high-side driver voltage and can operate up to 50V. The integrated driver eliminates the external clamping circuit. Besides, turn-on and turn-off resistors, bootstrap and VCC decoupling caps are all integrated which makes the external circuit super simple. Due to excellent internal layout, the associated gate loop and power loop parasitic is reduced significantly, with value much less than 1nH. As a result, ultra-low voltage spike on switch nodes can be achieved. The optimized pin layout of ISG1211 optimizes the power flow and simplifies the PCB board layout. ISG1211 has a single input to control high-side and low-side drivers in three states: High, Low, and Tri-State. Independent dead time can be adjusted through external resistors. The ISG1211 is available in a compact 4mmx5mmx1.12mm LGA package.

4. Typical Application

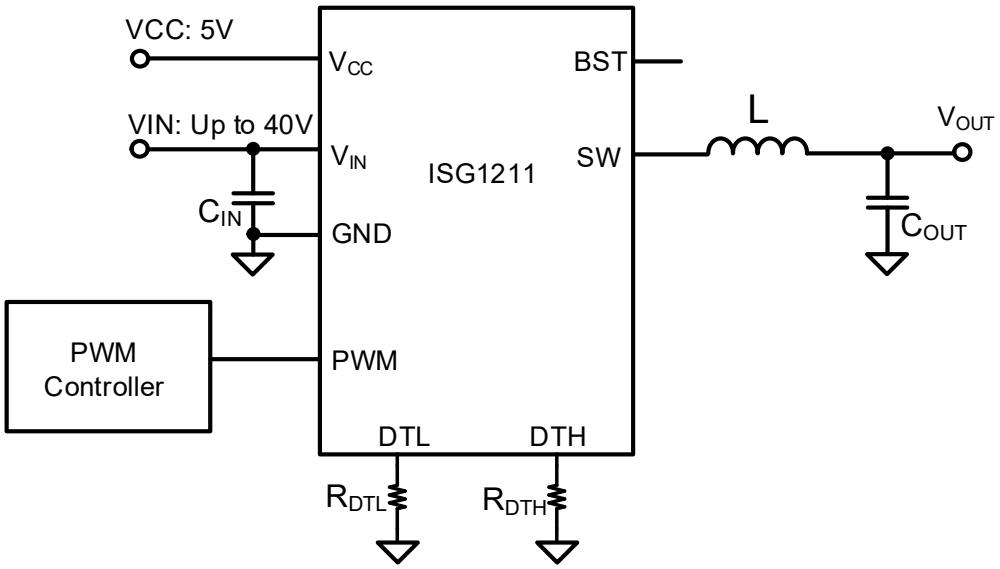


Figure 1. Typical application circuit diagram for a synchronous buck converter

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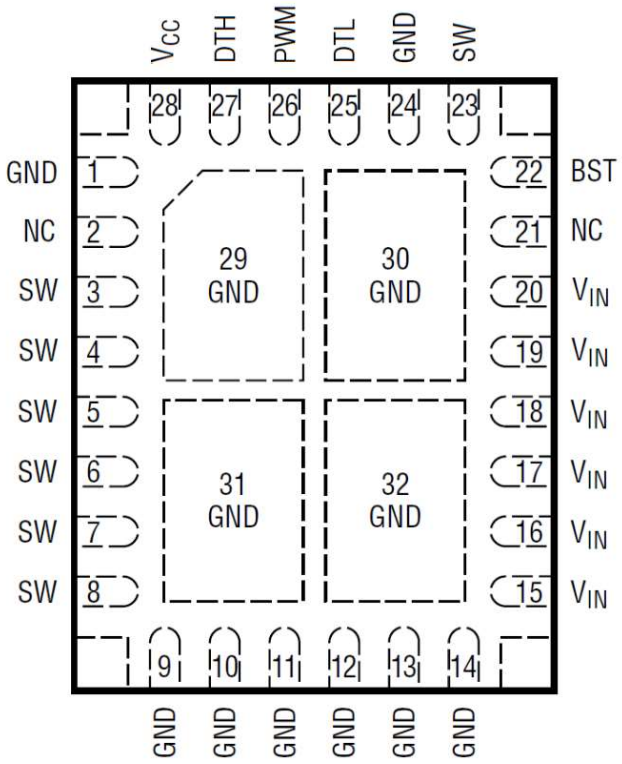
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5. Revision History

Major changes since the last revision

Revision	Date	Description of changes
DS 0.5	2023-11-21	Preliminary datasheet
DS 0.8		Pre-release datasheet
DS 1.0		Final release datasheet

6. Pin Configuration and Functions



28-Lead FCLGA(4mm x 5mm) Package – Top View

Pin Number	Pin Name	Description
1, 9-14, 24, Exposed Pad (29-32)	GND	Power Ground.
2, 21	NC	Not Connected.
3-8, 23	SW	Switching Node.
15-20	V_{IN}	Input Voltage Supply. Add high quality decoupling cap between V_{IN} and GND with minimum loop.
22	BST	High Side Gate Driver Bootstrap Rail.
25	DTL	Dead Time Setting for High-to-Low Transition. Connect a resistor to GND.
26	PWM	PWM Input. This pin receives tri-state input and controls the driver outputs.
27	DTH	Dead Time Setting for Low-to-High Transition. Connect a resistor to GND.
28	V_{CC}	5V Power Supply for Internal Control Circuit and Low-Side Gate Driver.

Absolute Maximum Ratings

All pins are referred to GND pins, unless otherwise specified. Stress beyond the absolute maximum ratings can cause permanent damage or deteriorate device lifetime.

Parameter	Min	Max	Unit

V_{IN} Voltage	-0.3	44	V
SW Voltage	-5	44	V
BST to SW Voltage	-0.3	6	V
PWM, DTL,DTH Voltage	-0.3	6	V
V_{CC} Voltage	-0.3	6	V
Operating Junction Temperature T_J	-40	150	˚C
Storage Temperature	-55	150	˚C

7. ESD Ratings

Parameter	Value	Unit
Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001 (3)	±2000	V
Charged Device Model (CDM), per ANSI/ESDA/JEDEC JS-002 (4)	±1000	V

(3) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(4) JEDEC document JEP155 states that 250V CDM allows safe manufacturing with a standard ESD control process.

8. Recommended Operating Conditions

Parameter	Min	Max	Unit
V_{IN} Voltage	0	40	V
V_{CC} Voltage	4.5	5.5	V
PWM Voltage	4.5	5.5	V
SW Voltage	-4	40	V
Operating Junction Temperature T_J	-40	125	˚C

9. Thermal Information

Symbol	Parameter	ISG1211	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	TBD	˚C/W
$R_{\theta JC(TOP)}$	Thermal Resistance, Junction to Case Top	TBD	˚C/W
$R_{\theta JC(BOT)}$	Thermal Resistance, Junction to Case Bottom	TBD	˚C/W

10. Electrical Characteristics

T_J = 25°C, VCC = 5V, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Supply Input						
VCC undervoltage rising threshold	V_{CC_UVR}	3.9	4.1	4.3	V	
VCC undervoltage hysteresis	V_{CC_UVHYS}		0.3		V	
VCC quiescent current	I_{CC-Q}		360	600	uA	PWM = High-Z, R_{DTH}=R_{DTL}=75kΩ
VCC operating current	I_{CC-OP}		1.5	3	mA	f = 500kHz
BST undervoltage rising threshold	$V_{BST-UVR}$		3.6		V	
BST undervoltage hysteresis	$V_{BST-UVHYS}$		0.5		V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
BST quiescent current	I_{BST-Q}		40	70	uA	PWM = High-Z
BST operating current	I_{BST-OP}		1.5	3	mA	f = 500kHz
PWM Input						
Input high threshold	V_{IH}	2	2.2	2.4	V	PWM rising
Input high hysteresis	V_{IH-HYS}	0.15	0.2	0.25	V	
Input low threshold	V_{IL}	0.8	1	1.2	V	PWM falling
Input low hysteresis	V_{IL-HYS}	0.15	0.2	0.25	V	
Input tri-state voltage	V_{TRI}	1.4	1.6	1.8	V	
Internal pull-up resistor	R_{IUP}		10		kΩ	To internal 3.2V supply
Internal pull-down resistor	R_{IDN}		10		kΩ	
Bootstrap Switch						
Low-current forward voltage			0.01	0.1	V	$I_{VCC-BST}$ = 100uA
High-current forward voltage			0.5		V	$I_{VCC-BST}$ = 100mA
Switch on resistance	$R_{BST(ON)}$		5		Ω	
Power GaN FET						
Top FET RON	$R_{DS(ON)_T}$		3	4.3	mΩ	PWM = 5V, I_{DS} = 15A
Bottom FET RON	$R_{DS(ON)_B}$		3	4.3	mΩ	PWM = 0V, I_{DS} = 15A
Drain-Source Leakage	I_{DSS}			100	uA	V_{GS} = 0 V, V_{DS} = 32 V

11. Switching Characteristics

T_J = 25°C, VCC = 5V, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Minimum input pulse width that changes the output (2)	T_{IPW}		5		ns	
Minimum gate output pulse width (2)	T_{OPW}		55		ns	
Dead time – LG off to HG on (2)	T_{DTH}		2 15		ns ns	R_{DTH} = 30kΩ R_{DTH} = 225kΩ
Dead time – HG off to LG on (2)	T_{DTL}		2 15		ns ns	R_{DTH} = 30kΩ R_{DTH} = 225kΩ
Low-side turn-off propagation delay (2)	T_{PLH}		22		ns	PWM rising to LG falling
High-side turn-off propagation delay (2)	T_{PHL}		22		ns	PWM falling to HG falling

(2) Not 100% tested and guaranteed by design.

12. Typical Characteristics

13. Block Diagram

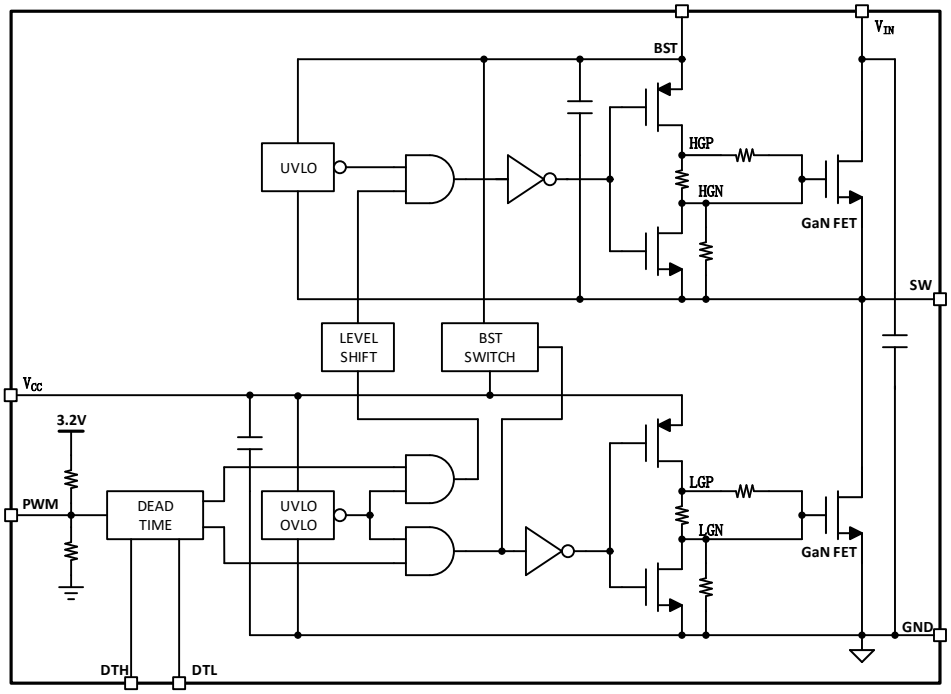


Figure 2. Functional Block Diagram

14. Function Description

The ISG1211 is designed as a fully integrated GaN Half-bridge power stages for multiple applications in Data Center, Server, Super computer, motor drive and class D audio systems. It is one of leading products in Innoscience's SolidGaN families. ISG1211 is small-footprint, easy for design and layout and serve as "drop-in" solution for board power. ISG1211 combines world-class GaN performance from Innoscience with high performance half-bridge driver specifically designed for GaN. Bootstrap capacitor, driving resistors and Vcc decoupling caps are all integrated into ISG1211 which significantly simplifies the application circuit. The optimized pinout structure makes the layout ultra easy while the parasitic is reduced significantly, i.e. gate loop and power loop parasitic. As a result, voltage spike of SW node is very small which enhances the reliability of the system.

PWM Input and Output

The ISG1211 employs a three-state PWM input that can withstand up to 5.5V. The input PWM voltage is monitored to determine whether it is higher than 2.2V, V_{IH}, and lower than 1.0V, V_{IL}, with a hysteresis of 200mV, V_{IL_HYS} and V_{IH_HYS}, and then controls HGP and HGN (HG) and LGP and LGN (LG), respectively. Table 1 illustrate the truth table of input and output. The PWM input is implemented with a 10kΩ pull-down resistor to GND and a 10kΩ pull-up resistor to internal 3.2V supply. Therefore, if the PWM input enters a high-impedance state, the PWM pin voltage goes to a typical value of 1.6V. This causes both HG and LG to go low, turning off both the external GaN FETs.

The PWM input provides the input deglitching delay time of a typical 5ns to prevent any fault triggering condition such as double pulsing during transition. The input with a pulse width shorter than a typical 55ns, but longer than the deglitch delay time, is extended to the minimum output pulse width of a typical 55ns.

Table 1. Input and Output Truth Table

PWM	HG	LG	Comment
L	L	H	Bottom GaN FET On
H	H	L	Top GaN FET On
Tri-state	Open	Open	Both GaN FETs Off

Undervoltage Lockout (UVLO) for Power Supply

The ISG1211 features an undervoltage lockout (UVLO) on both VCC and the floating voltage from BST to SW, (BST-SW). When VCC falls below the falling threshold voltage, typical 3.8V, HGP and HGN are pulled to SW and LGP and LGN are pulled to GND to turn off both the external GaN FETs and both input signals are ignored. When VCC is above the UVLO rising threshold voltage, typical 4.0V, but (BST-SW) is below the falling threshold voltage of typical 3.65V, HGP and HGN are pulled to SW and PWMH is ignored while the LGP and LGN are synchronized with PWML. When both VCC and (BST-SW) are recovered above the rising threshold voltage, typical 4.0V, the ISG1211 will normally operate.

VCC Overvoltage Lockout (OVLO)

To provide the operation under the safe conditions of devices, the ISG1211 contains VCC overvoltage lockout (OVLO) protection. When VCC rises above typical 6V, the HGP and HGN are pulled to SW and LGP and LGN are pulled to GND. VCC OVLO has a typical 200mV hysteresis.

Adjustable Dead Time

To ensure robust shoot-through protection, ISG1211 supports an adjustable dead-time scheme using external resistors, R_{DTH} and R_{DTL}, connected to DTH and DTL, respectively. R_{DTH} and R_{DTL} determine the dead time between LG turning off to HG turning on, $T_{DTH,}$ and the dead time between HG turning off to LG turning on, T_{DTL}, respectively. The relationship between the resistance values of R_{DTH} and R_{DTL} and the dead time of T_{DTH} and T_{DTL} can be estimated by following equation when the resistors are less than 225kΩ:

$$T_{DTH}=\frac{1ns}{15k\Omega}\times R_{DTH} \quad (1)$$

$$T_{DTL}=\frac{1ns}{15k\Omega}\times R_{DTL} \quad (2)$$

Figure 3 shows the relationship between the dead time and resistance values of R_{DTH} and R_{DTL}. The minimum deadtime of the ISG1211, $T_{DT,MIN}$, is determined by the adaptive shoot-through protection, even if RDTH and RDTL are shorted to GND, ensuring robust system operation.

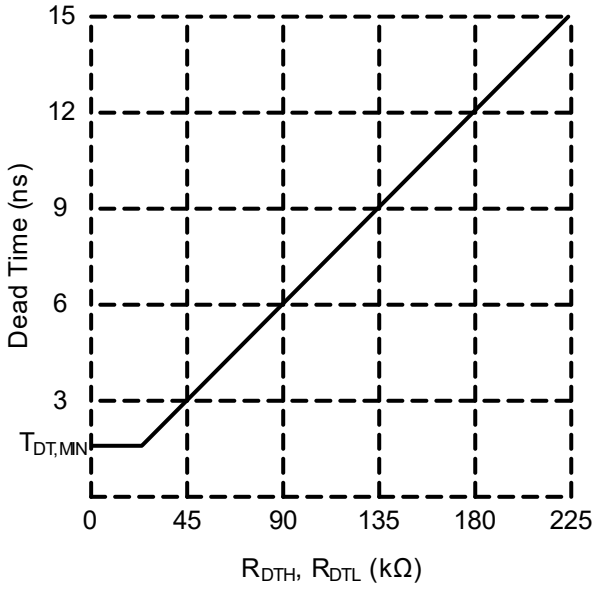


Figure 3. Dead Time vs R_{DTH} and R_{DTL}

High-side Gate-Driver Supply

When the FET is turned off and negative current flows through the FET, the drain-to-source voltage of FET becomes negative voltage. It can be easily observed during the deadtime, T_{DTL} and T_{DTH}, in the half-bridge topology. Due to the intrinsic device characteristics, GaN FET has a larger negative drain-to-source voltage than MOSFET which has a diode forward voltage drop. Therefore, with a traditional bootstrap circuit which has a forward diode path from VCC to BST, the bootstrap capacitor can be excessively overcharged, especially in the application implemented with GaN FETs. The overcharged BST voltage can damage FETs.

To prevent overcharging the bootstrap capacitor, the ISG1211 employs the internal smart bootstrap circuit as shown in Figure 4. The bootstrap switch is turned on when the low-side FET is fully turned on, $T_{BST-CHG}$. Since the smart bootstrap switch is implemented without the forward diode path between VCC and BST, the switch completely disconnects to BST when the low-side FET is turned off. Therefore, the ISG1211 prevents the excessive overcharging of the bootstrap capacitor due to the large negative voltage of SW during the deadtime and provides the safe condition to operate the FETs.

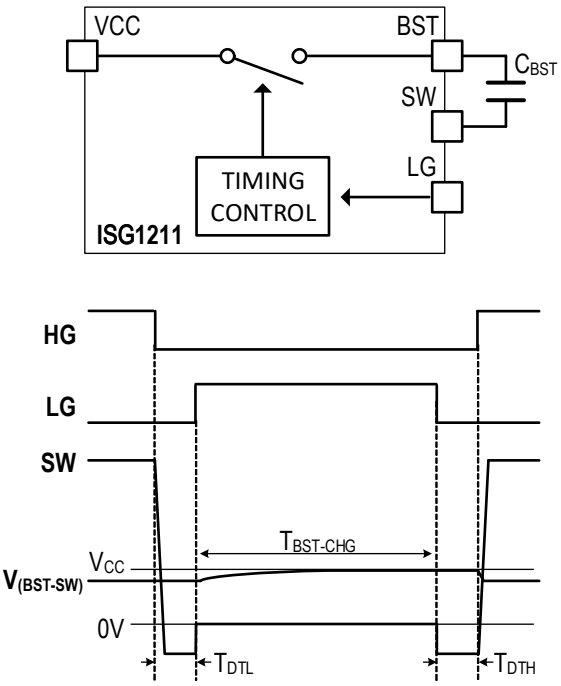


Figure 4. Block and Timing Diagrams of Smart Bootstrap Circuit

PCB Layout Checklist

Follow these PCB layout guidelines for optimal performance.

• Keep the high current traces as short and wide as possible

• Place the input capacitor very near V_{IN} and GND minimizing the loop formed by these connections.

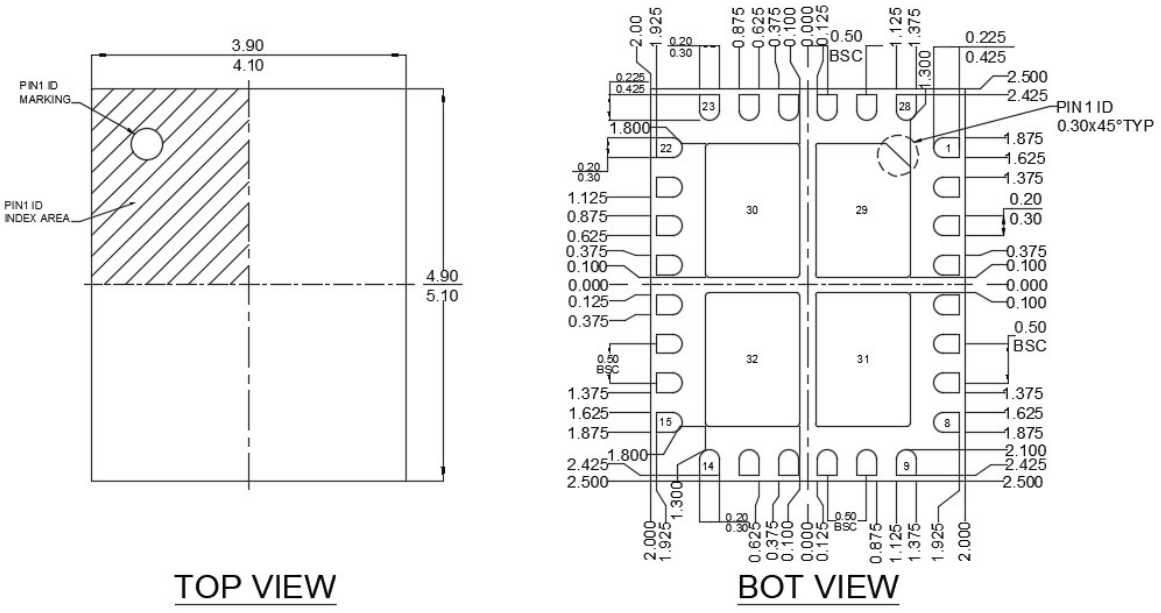
• The SW connection has large voltage swings and fast edges and can easily radiate noise to adjacent components. Keep its area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance. Keep sensitive components away from the SW node or provide ground traces between for shielding, to prevent stray capacitive noise pickup.

• The exposed GND pad should be connected to a large copper area for heat sinking and to minimize noise.

•Provide dedicated wide copper traces for the power path ground between the IC and the input and output capacitor grounds, rather than connecting each of these individually to an internal ground plane.

15. Package Information

FCLGA4X5-28 Package:

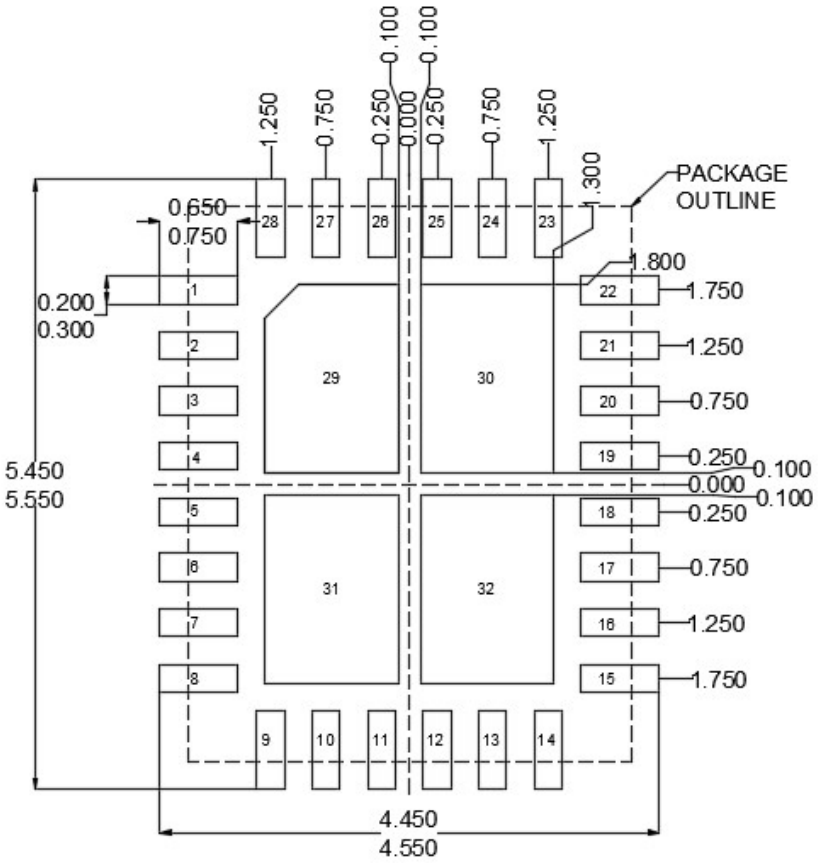


NOTE:
1)ALL DIMENSION ARE IN MILLIMETERS.
2)BOTTOM VIEW IS FT TESTER SIDE VIEW.
3)LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4)COMPLIES WITH JEDEC MO-303.
5)DRAWING IS NOT TO SCALE.

16. Tape and Reel Information

17. Recommended Land Pattern

FCLGA4X5-28 Package:



TOP VIEW

18. Order Information

Ordering Code	Package	Product Code	MSL	Packing (Tape & Reel)

Important Notice

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