FE2.1

USB 2.0 High Speed 7-Port Hub Controller

Data Sheet

Introduction

Terminus FE2.1 is a highly integrated, high-quality, high-performance, low power consumption, yet low-cost USB 2.0 High Speed 7-Port Hub solution.

FE2.1 adopts Multiple Transaction Translator (MTT) architecture to explore the maximum possible throughput. Six non-periodic transaction buffers, instead of two, are used to minimize potential traffic jamming. The whole design is based on state-machine-control to reduce the response delay time; no microcontroller is used in this chip.

To guarantee high quality, the whole chip is covered by *Test Scan Chain* – even on the high speed (480MHz) modules, so that all the logic components could be fully tested before shipping. Special *Built-in Self-Test Mode* is designed to exercise all high, full, and low speed Analog Front End (AFE) components in the packaging and testing stages as well.

Low power consumption is achieved by using a comprehensive power/clock control mechanism. Most parts of the chip will not be clocked unless needed.

Features

- Fully compliant with Universal Serial Bus Specification Revision 2.0 (USB 2.0);
  - Upstream Facing Port supports High-Speed (480MHz) and Full-Speed (12MHz) modes;
  - 7 Downstream Facing Ports support High-Speed (480MHz), Full-Speed (12MHz), and Low-Speed (1.5MHz) modes;
- Integrated USB 2.0 Transceivers;
- Integrated upstream 1.5KΩ pull-up, downstream 15KΩ pull-down, and serial resistors;
- Integrated 5V to 3.3V and Core Power regulator;
- Integrated Power-On-Reset circuit;
- Integrated 12MHz Oscillator with feedback resistor and crystal load capacitor;
- Integrated 12MHz-to-480MHz Phase Lock Loop (PLL);
- Support Self-Power Mode only;
- Multiple Transaction Translators (MTT) –
  - One TT for each downstream port;
  - Alternate Interface 0 for Single-TT, and Alternate Interface 1 for Multiple-TT;
  - Each TT could handle 64 periodic Start-Split transactions, 32 periodic Complete-Split transactions, and 6 non-periodic transactions;

- Board configured options –
  - *Ganged, Multiple Gangs or Individual Power Control Mode* select*;*

    (48-pin Package only supports Multiple Gangs Power Control Mode)
    - *Ganged or Individual Logical Power Switching Mode* select*;*
    - *Global* or *Individual Over-Current Protection Mode* select;
  - *Removable or Non-Removable Downstream Devices* configuration;
  - *Number of Downstream Ports*;
- EEPROM configured options –
  - *Vendor ID*, *Product ID*, & *Device Release Number*;
  - *Removable* or *Non-Removable Downstream Devices* configuration;
  - *Serial Number*; and
  - *Number of Downstream Ports*;
- Comprehensive status Indicators support:
  - Standard downstream port status indicators (Green and Amber LED control for each downstream port);
  - *Hub Active/Suspend* indicator LED.

PACKAGE

- 48-pin LQFP (body size: 7x7 mm)
- 64-pin LQFP (body size: 10x10 mm)

Order Information

P/N-Order Code	Description	Package Type	Packing	Minimum Order Quantity
FE2.1-CQFP48A	USB 2.0 7-Port MTT Hub Controller	48-pin LQFP (7mm x 7mm)	Tray	15000
FE2.1-CQFP48AT(Note 1)		48-pin LQFP (7mm x 7mm)	Tray	2500
FE2.1-CQFP64A		64-pin LQFP (10mm x 10mm)	Tray	9600
FE2.1-CQFP48AB		48-pin LQFP (7mm x 7mm)	Tray	15000
FE2.1-CQFP48ABT(Note 1)		48-pin LQFP (7mm x 7mm)	Tray	2500
FE2.1-CQFP64AB		64-pin LQFP (10mm x 10mm)	Tray	9600

Note 1: Products of order code CQFP48AT and CQFP48ABT are final tested in Room Temperature, 85°C, and -40°C, respectively.

Note 2: All Terminus products are *Halogen Free* and *RoHS Compliant*.

Block Diagram

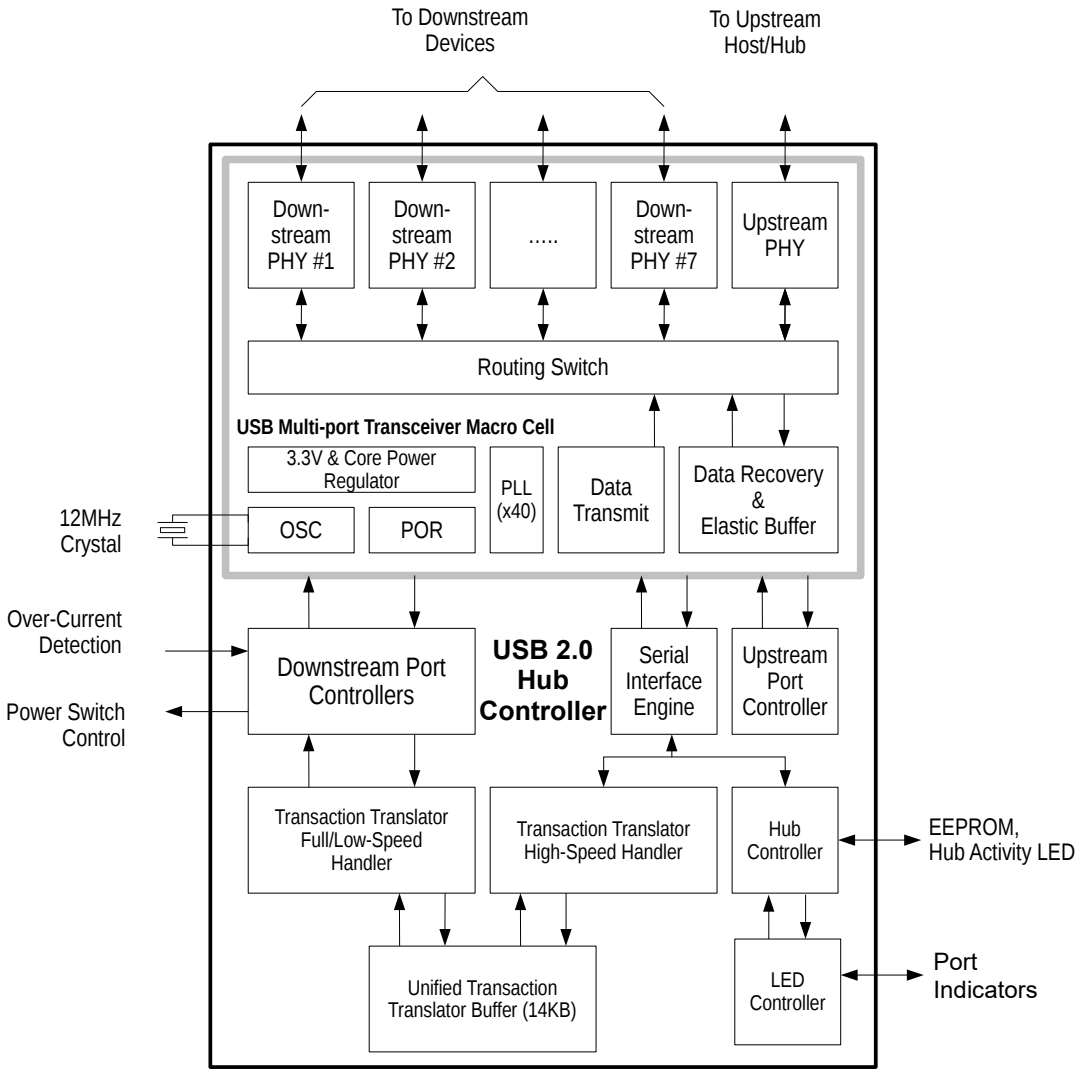


Fig. 1: Block Diagram

PACKAGE I – 64-PIN LQFP

(Body Size: 10 x 10 mm)

PIN ASSIGNMENT

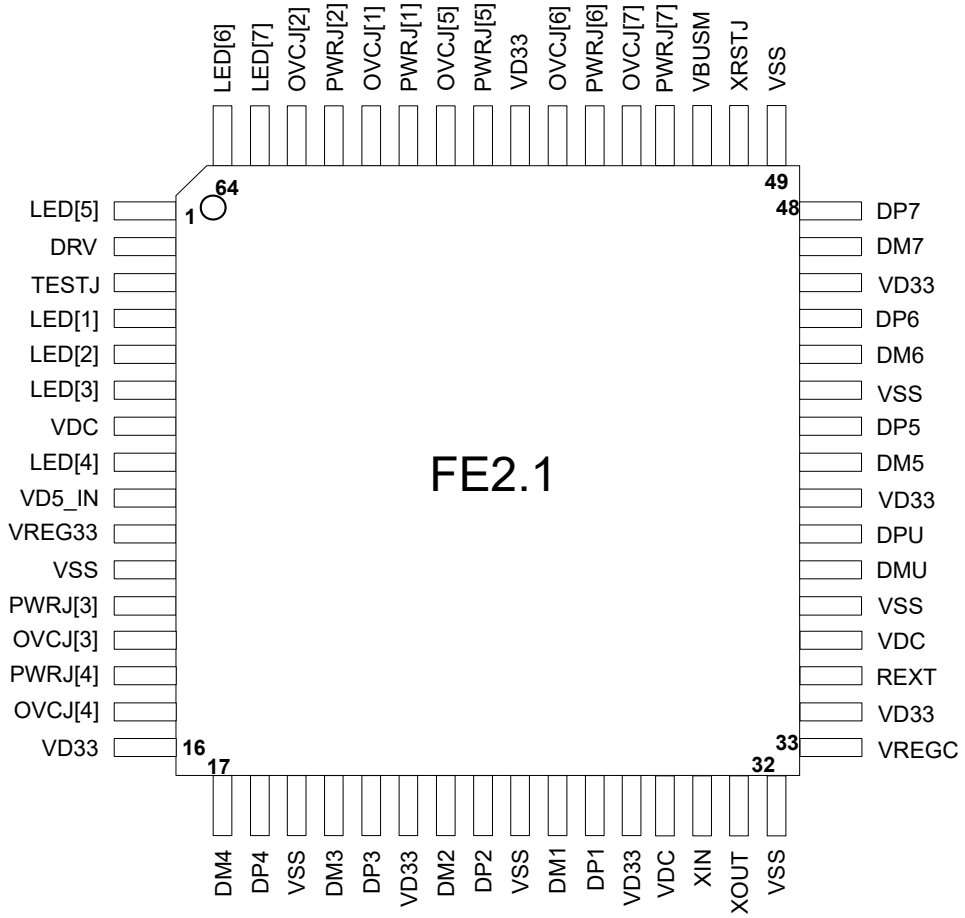


Fig. 2: 64-Pin LQFP Pin Assignment

Package II – 48-pin LQFP
(Body Size: 7 x 7 mm)

Pin Assignment

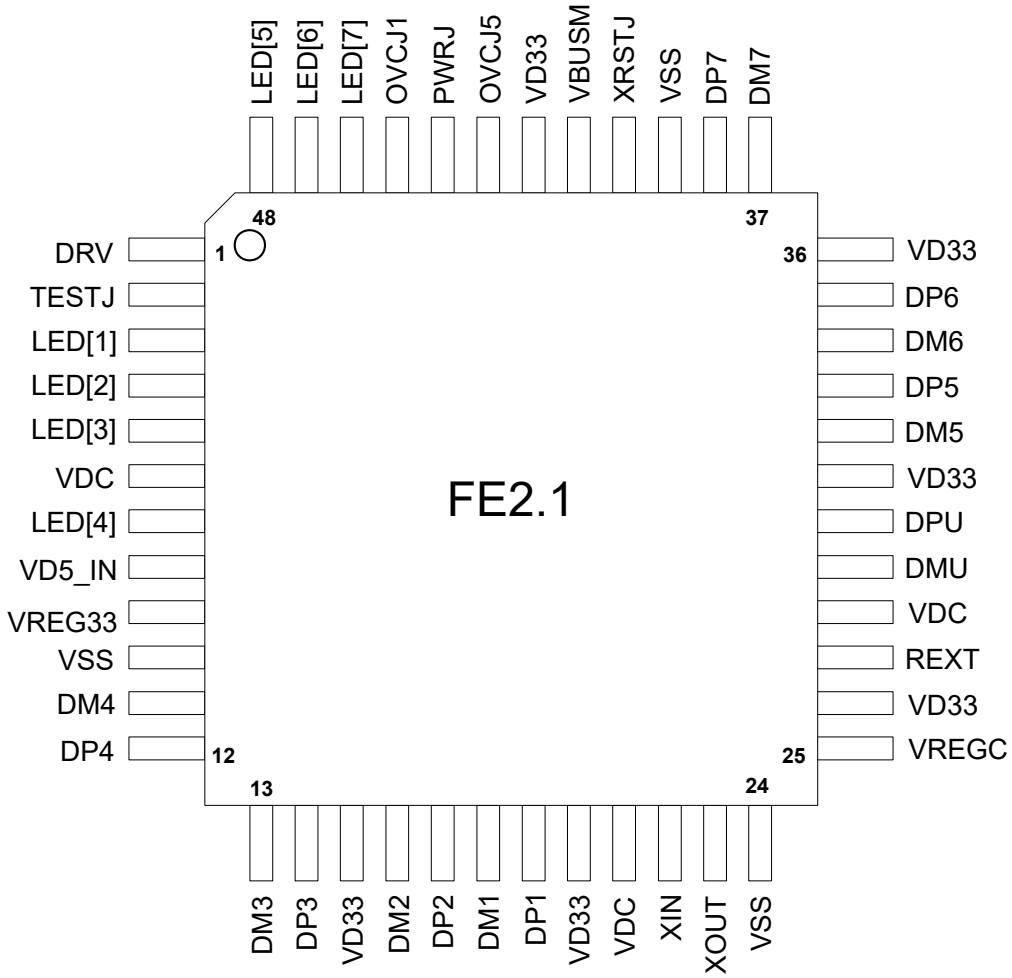


Fig. 3: 48-Pin LQFP Pin Assignment

Pin Description Table

Pin Name	64-pin LQFP Pin No.	48-pin LQFP Pin No.	Type	Function	Note
LED[5]	1	48	O	LED Control for the 5th Downstream Facing Port Status.	
DRV	2	1	O	Driving Control for all LEDs.	
TESTJ	3	2	IO-PU	Test Mode Enable during hardware reset – active low. If it is not under Test Mode, SDA (Serial Data/Address pin) is for external Serial EEPROM. If the external EEPROM is not required, the TESTJ pin should be left floating.	
LED[1]	4	3	O/IO-PU	LED Control for the 1st Downstream Facing Port Status and SCL (Serial Clock pin) for external Serial EEPROM.	5
LED[2]	5	4	O/I-PU	LED Control for the 2nd Downstream Facing Port Status and Non-Removable Device Configuration bit 0.	4
LED[3]	6	5	O/I-PU	LED Control for the 3rd Downstream Facing Port Status and Non-Removable Device Configuration bit 1.	4
VDC	7, 29, 36	6, 21, 28	P	Core Power.	6
LED[4]	8	7	O/I-PU	LED Control for the 4th Downstream Facing Port Status and Non-Removable Device Configuration bit 2.	4
VD5_IN	9	8	P	5V power input for integrated 5V→3.3V regulator.	6
VREG33	10	9	P	5V→3.3V regulator output – a 10µF output ceramic capacitor is required. For internal use only.	6
VSS	11, 19, 25, 32, 37, 43, 49	10, 24, 39	P	Ground.	
PWRJ[3]	12	—	OD	Power Enable for 3rd Downstream Facing Port – active low.	
OVCJ[3]	13	—	I-PU	Over-Current Detect for 3rd Downstream Facing Port – active low.	2
PWRJ[4]	14	—	OD	Power Enable for 4th Downstream Facing Port – active low.	
OVCJ[4]	15	—	I-PU	Over-Current Detect for 4th Downstream Facing Port – active low.	2
VD33	16, 22, 28, 34, 40, 46, 56	15, 20, 26, 31, 36, 42	P	3.3V Power Input.	6
DM4	17	11	UTD	The D- pin of the 4th Downstream Facing Port.	
DP4	18	12	UTD	The D+ pin of the 4th Downstream Facing Port.	
DM3	20	13	UTD	The D- pin of the 3rd Downstream Facing Port.	
DP3	21	14	UTD	The D+ pin of the 3rd Downstream Facing Port.	
DM2	23	16	UTD	The D- pin of the 2nd Downstream Facing Port.	
DP2	24	17	UTD	The D+ pin of the 2nd Downstream Facing Port.	

DM1	26	18	UTD	The D- pin of the 1st Downstream Facing Port.	
DP1	27	19	UTD	The D+ pin of the 1st Downstream Facing Port.	
XIN	30	22	OSC	12 MHz Crystal Oscillator input.	1
XOUT	31	23	OSC	12 MHz Crystal Oscillator output.	1
VREGC	33	25	P	Core Power regulator output – a 10µF output ceramic capacitor is required. For internal use only.	6
REXT	35	27	A	A 2.7KΩ (± 1%) resistor should be connected to VSS to provide internal bias reference.	
DMU	38	29	UTU	The D- pin of the Upstream Facing Port.	
DPU	39	30	UTU	The D+ pin of the Upstream Facing Port.	
DM5	41	32	UTD	The D- pin of the 5th Downstream Facing Port.	
DP5	42	33	UTD	The D+ pin of the 5th Downstream Facing Port.	
DM6	44	34	UTD	The D- pin of the 6th Downstream Facing Port.	
DP6	45	35	UTD	The D+ pin of the 6th Downstream Facing Port.	
DM7	47	37	UTD	The D- pin of the 7th Downstream Facing Port.	
DP7	48	38	UTD	The D+ pin of the 7th Downstream Facing Port.	
XRSTJ	50	40	I	External Reset – active low, it is an optional source of chip reset signal besides the built-in Power-On-Reset. The minimum low pulse width is 10 µs.	
VBUSM	51	41	I	The V_{BUS} Monitor of Upstream Facing Port.	
PWRJ[7]	52	—	OD/I-PU	Power Enable for 7th Downstream Facing Port – active low, and Power Control Mode Configuration bit 1.	3
OVCJ[7]	53	—	I-PU	Over-Current Detect for 7th Downstream Facing Port – active low.	2
PWRJ[6]	54	—	OD/I-PU	Power Enable for 6th Downstream Facing Port – active low, and Power Control Mode Configuration bit 0.	3
OVCJ[6]	55	—	I-PU	Over-Current Detect for 6th Downstream Facing Port – active low.	2
PWRJ[5]	57	—	OD	Power Enable for 5th Downstream Facing Port – active low.	
OVCJ[5]	58	43	I-PU	Over-Current Detect for 5th Downstream Facing Port – active low.	2
PWRJ[1]	59	44	OD	Power Enable for 1st Downstream Facing Port – active low.	
OVCJ[1]	60	45	I	Over-Current Detect for 1st Downstream Facing Port – active low.	2, 4
PWRJ[2]	61	—	OD	Power Enable for 2nd Downstream Facing Port – active low.	
OVCJ[2]	62	—	I-PU	Over-Current Detect for 2nd Downstream Facing Port – active low.	2
LED[7]	63	46	O/I-PU	LED Control for the 7th Downstream Facing Port Status and Number of Ports Configuration bit 1.	4
LED[6]	64	47	O/I-PU	LED Control for the 6th Downstream Facing Port Status and Number of Ports Configuration bit 0.	4

Note –

1. Crystal Requirements
   - Frequency accuracy: 12MHz ± 50ppm
   - Load capacitance: 16pF ~ 20pF
   - Equivalent Series Resistance: 50Ω Max.

2. Pins OVCJ[7:2] are equipped with optional internal pull-up resistors. When a certain OVCJ pin is not required by the currently configured *Over-Current Protection Mode*, its internal pull-up resistor will be applied so that pin can be left as unconnected on the board. Otherwise, when a certain OVCJ pin is used by the currently configured *Over-Current Protection Mode*, its pull-up resistor will be removed so that it can be used to monitor either 3.3V or 5V input from an external application circuit; if there is no external application circuit under such mode, all OVCJ pins must be pulled high if not used.

3. During the power-up configuration stage, pins PWRJ[7:6] are used as inputs with internal pull-up resistors. After this stage, they will be configured as open drain output.

4. During the power-up configuration stage, pins LED[4:2] and LED[7:6] are used as inputs with internal pull-up resistors. After this stage, they will be configured as CMOS output.

5. During the power-up configuration stage, pin LED[1] is used as CMOS tristate I/O to work with the external EEPROM as serial clock. After this stage, it is used as CMOS output.

6. Power Source
   The power source for FE2.1 could be either fed in from VD5_IN or VD33, but not both. The core power (VDC) of FE2.1 must be served by the built-in 3.3V-to-core-power regulator to maintain the performance of its Phase Lock Loop (PLL).

   Using 5V power source, the power is fed in VD5_IN, passed through the 5V-to-3.3V regulator, and outputs 3.3V to VREG33. The output capability of VREG33 is designed for FE2.1 use only. No other device should source its power from this pin. VREG33 should connect with a 10µF output ceramic capacitor, then to all the VD33 pins. VREGC is the output for 3.3V-to-core power regulator. With a 10µF output ceramic capacitor, it should connect to all VDC pins of FE2.1.

When external 3.3V power source is selected, all VD33 pins of FE2.1 will be served by external 3.3V source of the system. VREGC is the output for 3.3V-to-core power regulator. With a 10µF output ceramic capacitor, it should connect to all VDC pins of FE2.1.

It is highly recommended that FE2.1 use the same 3.3V power source as the other interconnected components when 3.3V power is available in the system. Under this scheme, both VD5_IN and VREG33 should be left unconnected.

Type Abbreviation –

I: Schmitt Trigger Input, 5V-Tolerant;
I-PU: Input with Controllable Internal Pull-Up, 5V-Tolerant when pull-up resistor is disabled;
IO-PU: CMOS tristate Output with Input and Internal Pull-Up;
OD: Open Drain Output;
O: CMOS Output;
A: Analog I/O;
P: Power/Ground;
OSC: Crystal Oscillator with internal feedback resistor and load capacitor;
UTU: USB High-Speed and Full-Speed Transceiver;
UTD: USB High-Speed, Full-Speed, and Low-Speed Transceiver.

Configurable Options

FE2.1 is a highly versatile design that can be easily configured to meet many implementation requirements. Its behavior can be configured by using either board design selected options or through the contents of external EEPROM.

LED Indicators, Number of Downstream Facing Ports, and Non-Removable Devices

According to the USB 2.0 Specification, the status of each downstream port is shown by two LED indicators – the Green and Amber LEDs. FE2.1 supports the full function specified by DRV and LED[7:1] pins. *Figure 4* illustrates how these port status indicators, together with the external EEPROM and the *Hub Active Indicator* (the Red LED), are connected.

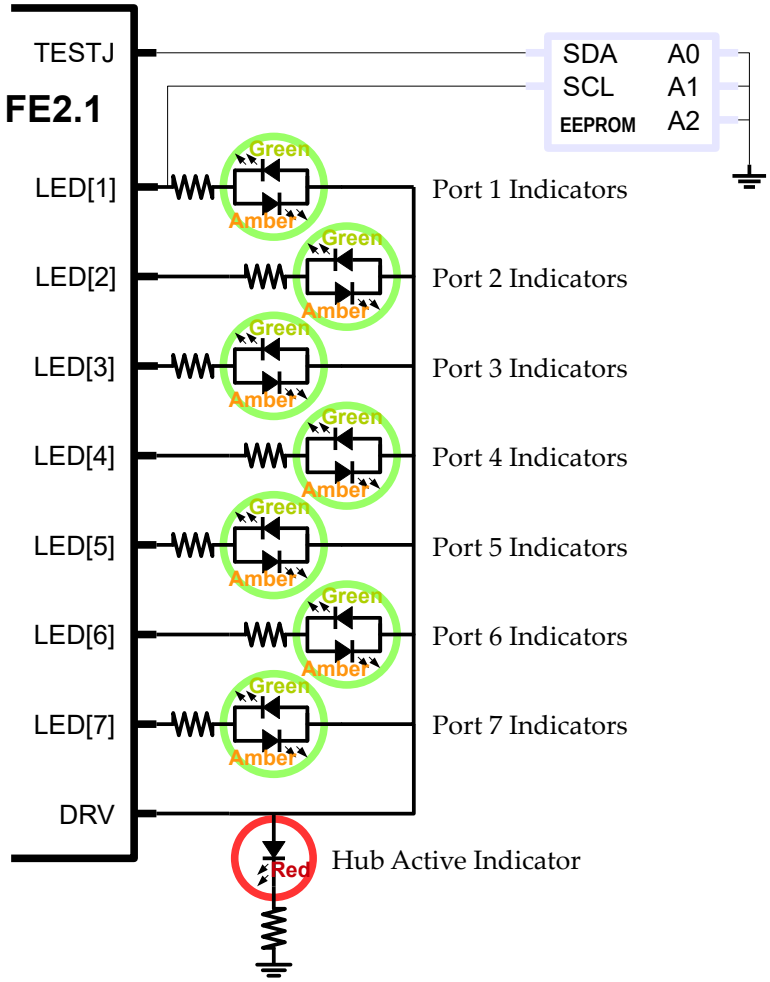


Fig. 4: LED and EEPROM Connections

The optional Hub Active Indicator is only turned on when the hub is configured by the host and turned off when the hub is set to suspend mode, disconnected, or powered off by the host. Any of these fifteen LEDs can be removed without affecting the normal function of the hub.

The LED[7:1] pins can also be used to configure the number of Downstream Facing Ports and Non-Removable downstream devices. These option selections are sampled and loaded each time after chip reset. If a different configuration is intended, the corresponding pins should be tied to ground as shown in the following table. Otherwise, as indicated by 'Normal', they can be left floating or connected to the LEDs (*Figure 4*).

Usable Downstream Facing Port	LED[7] Number of Ports Configuration bit 1	LED[6] Number of Ports Configuration bit 0
4, 3, 2, 1	Tied-to-Ground	Tied-to-Ground
5, 4, 3, 2, 1	Normal	Tied-to-Ground
6, 5, 4, 3, 2, 1	Tied-to-Ground	Normal
7, 6, 5, 4, 3, 2, 1	Normal	Normal

Setting the number of Downstream Facing Ports by tying any of LED[7:6] to ground will change the bNbrPorts field (3rd byte) of *Hub Descriptor* and the *Hub Descriptor* will respond to the host's GetHubDescriptor request. Hence, the ports beyond the specified number will not be recognized nor activated by the host.

Non-Removable Downstream Facing Port	LED[4] Non-Removable Device Configuration bit 2	LED[3] Non-Removable Device Configuration bit 1	LED[2] Non-Removable Device Configuration bit 0
None	Normal	Normal	Normal
2	Normal	Normal	Tied-to-Ground
3, 2	Normal	Tied-to-Ground	Normal
3, 2, 1	Normal	Tied-to-Ground	Tied-to-Ground
4, 3, 2, 1	Tied-to-Ground	Normal	Normal
5, 4, 3, 2, 1	Tied-to-Ground	Normal	Tied-to-Ground
6, 5, 4, 3, 2, 1	Tied-to-Ground	Tied-to-Ground	Normal
7, 6, 5, 4, 3, 2, 1	Tied-to-Ground	Tied-to-Ground	Tied-to-Ground

The Non-Removable Downstream Facing Port settings are written in the bit-map of DeviceRemovable field of *Hub Descriptor* and the *Hub Descriptor* will respond to the host's GetHubDescriptor request.

When a Downstream Facing Port is configured as unusable or Non-Removable, its corresponding LED pin will be disabled. In other words, those LED pins should be either tied to ground based on the selected configuration or left floating. The only exception is LED[1], which would still be used as SCL (Serial Clock pin) for external EEPROM if it exists.

Figure 5 illustrates an example of enabling only 5 Downstream Facing Ports, with port 3 and 2 as Non-Removable devices. As shown, LED[4] is connected to the LED, LED[2] left floating, and LED[3] tied to ground, so that FE2.1 would recognize that port 3 and 2 are Non-Removable devices. LED[6] is tied to ground and LED[7] left floating, thus FE2.1 will report to system that only 5 ports are available in this hub.

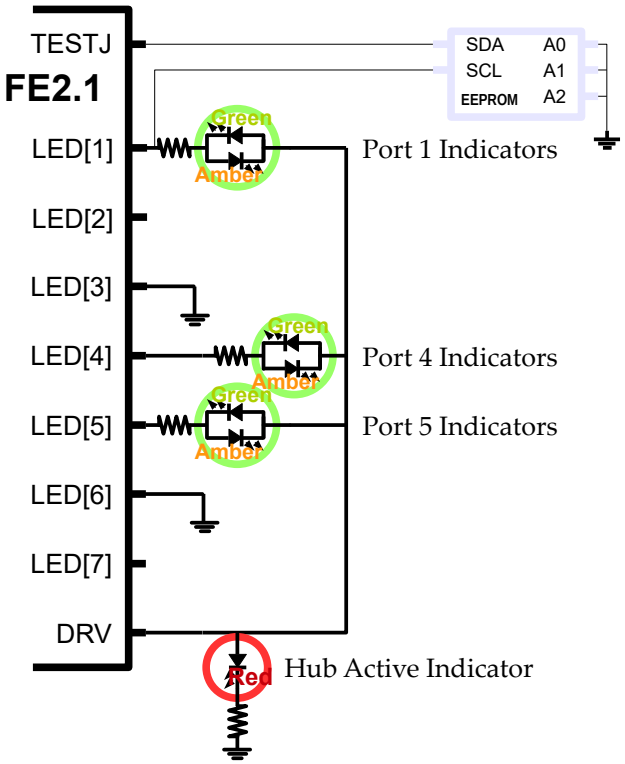


Fig. 5: LED Board Configuration Example

If the external EEPROM is not required, the TESTJ pin should be left floating. If the Hub Active Indicator is not required, the LED and its serial resistor should be removed together. If the port status LEDs are not required, LED[5:4] and LED[1] should be left floating with all their related Green/Amber LEDs and resistors removed.

Power Control and Over-Current Protection

FE2.1 supports optional power switches that control the power delivery of Downstream Facing Ports by PWRJ[7:1] (active low, open drain, control pins). With 5V or 3.3V external pull-up resistors, system designers can choose from a wide variety of circuits to implement the power switches.

As a self-powered hub, over-current protection is a must for safety reasons. FE2.1 provides a set of input pins – OVCJ[7:1] – to monitor the status of the external over-current detection circuit. The over-current status will then be reported to the host hub driver by FE2.1. Depending on the power control mode selected, the unused OVCJ pins will be internally pull-up and left unconnected.

FE2.1 supports three types of power control modes: *Individual Mode*, *Multiple Gangs Mode*, and *Ganged Mode*. These modes could be configured by tying either or both PWRJ[7:6] to ground according to the following table.

Power Control Mode	PWRJ[7] Power Control Mode Configuration bit 1	PWRJ[6] Power Control Mode Configuration bit 0	wHubCharacteristics		PWRJ [N]	PWRJ [N]	Availability
			D1..D0	D4..D3			
Individual Mode	Normal	Normal	01	01	1, 2, 3, 4, 5, 6, 7	1, 2, 3, 4, 5, 6, 7	LQFP-64
Multiple Gangs Mode	Tied-to-Ground	Normal	00	01	1	1, 5	LQFP-64, LQFP-48
Ganged Mode	Tied-to-Ground	Tied-to-Ground	00	00	1	1	LQFP-64

In the *Individual Mode*, the power switch of each port is controlled individually, and the over-current status is reported on a per-port basis. That is, for each port *N*, the power switch is controlled by PWRJ[*N*], and the over-current status is monitored by OVCJ[*N*].

Figure 6 illustrates a LQFP-64 implementation of *Individual Mode* design with dual-channel power distribution switches. In this case, 3.3V pull-ups are used for PWRJ/Enable pins to meet the requirements of the specific switches used.

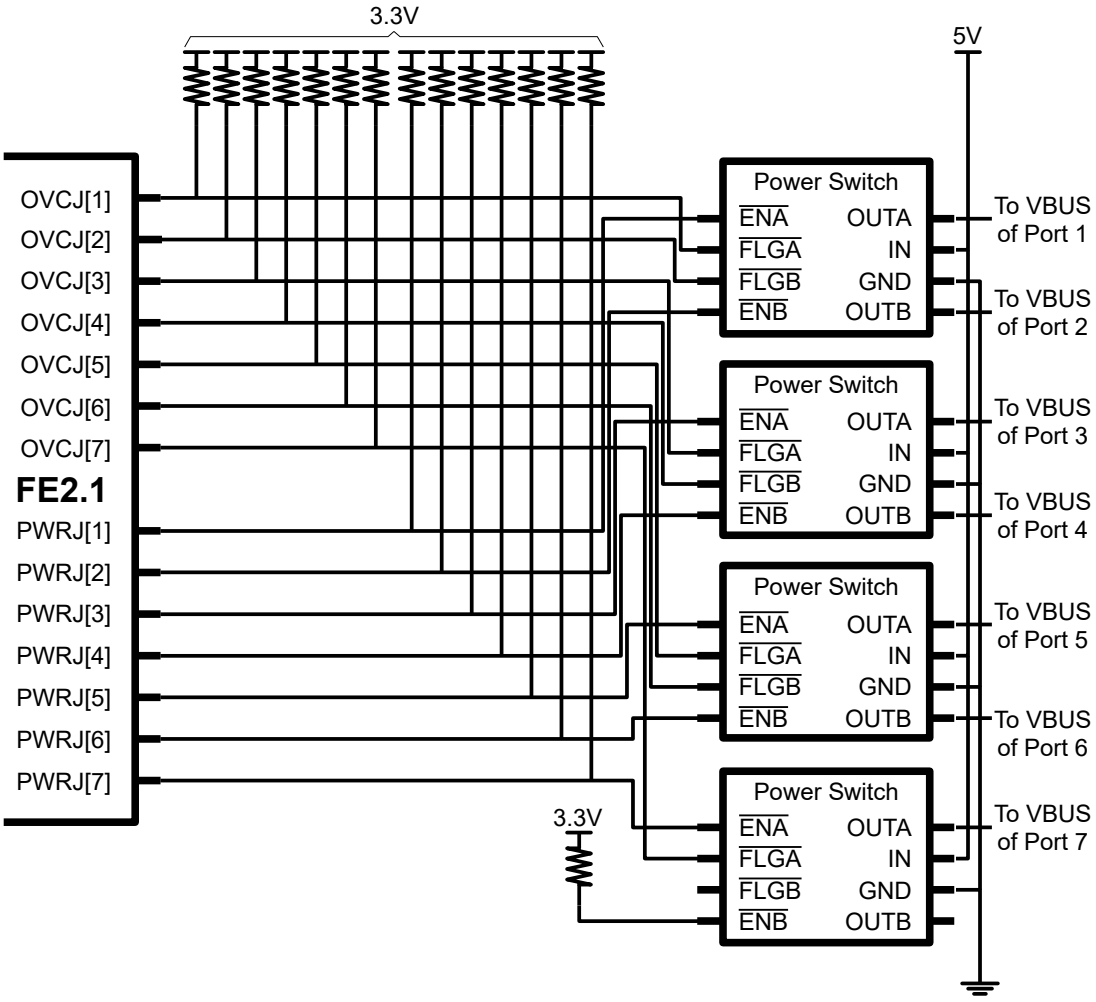


Fig. 6: LQFP-64 Individual Power Control Mode Example

In the *Ganged Mode*, the power switch to all ports is controlled by one single PWRJ[1], and the over-current is monitored by OVCJ[1]. Therefore, when the host issues SetPortFeature(PORT_POWER) to any of the Downstream Facing Ports, PWRJ[1] will become

active. PWRJ[1] will become inactive only when all ports are in powered-off state. Since there is only one OVCJ input, all Downstream Facing Ports will be marked as over-current simultaneously and set to powered-off state.

The *Multiple Gangs Mode* has one more over-current status pin, OVCJ[5], compared to the *Ganged Mode*. If OVCJ[1] goes low, Downstream Facing Port 1, 2, 3, and 4 would be marked as over-current. If OVCJ[5] goes low, Downstream Facing Port 5, 6, and 7 would be marked as over-current. Since there is only one PWRJ pin, all ports will be switched to powered-off state at once. This is the only mode supported by LQFP-48 package of FE2.1.

The power control mode selection is reported to the host software through the wHubCharacteristics field (the 4th and 5th byte) of Hub Descriptor, which describes the hub's operational characteristics. The two bits in this field will affect “D1..D0” for *Logical Power Switching Mode*, and another two bits will affect “D4..D3” for *Over-Current Protection Mode*. In “D1..D0”, 00 represents ganged power switching (all ports' power at the once) and 01 represents individual port power switching. In “D4..D3”, 00 represents global over-current protection and 01 represents individual port over-current protection.

Figure 7 and *Figure 8* illustrate LQFP-64 implementations of *Ganged Mode* and *Multiple Gangs Mode* with power switches.

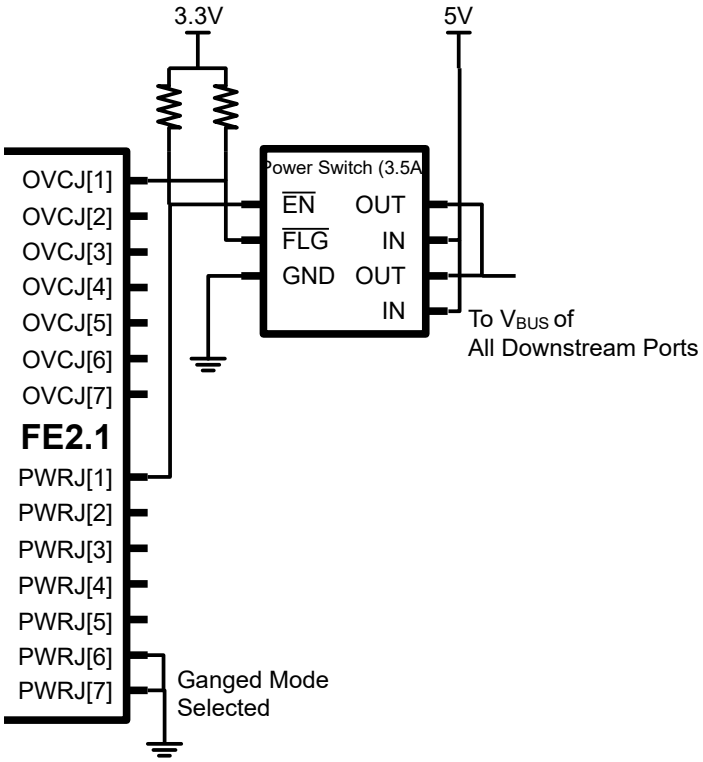


Fig. 7: LQFP-64 Ganged Power Control Mode Example

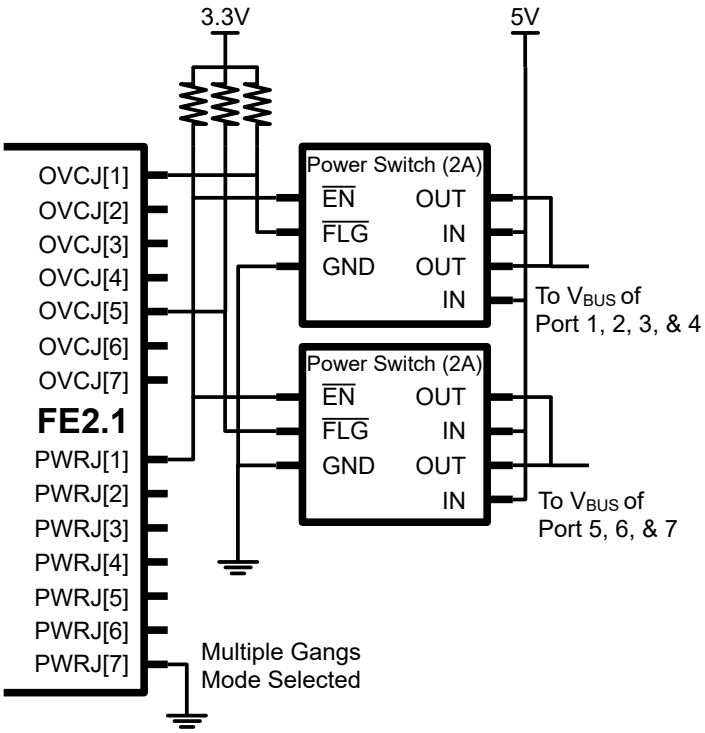


Fig. 8: LQFP-64 Multiple Gangs Power Control Mode Example

And *Figure 9* illustrates LQFP-48 implementation of *Multiple Gangs Mode* – the only mode supported by LQFP-48 package.

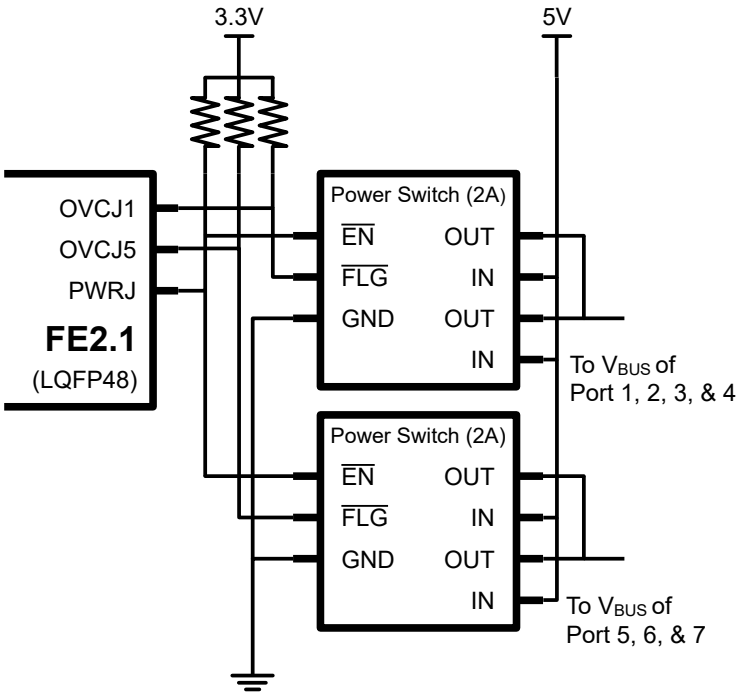


Fig. 9: LQFP-48 Multiple Gangs Power Control Mode Example

EEPROM Contents

Address	Contents	Note
0x00	0x40	Constant – low byte of check code.
0x01	0x1A	Constant – high byte of check code.
0x02	Vendor ID (Low)	Low byte of Vendor ID – idVendor field of *Standard Device Descriptor.*
0x03	Vendor ID (High)	High byte of Vendor ID – idVendor field of *Standard Device Descriptor.*
0x04	Product ID (Low)	Low byte of Product ID – idProduct field of *Standard Device Descriptor.*
0x05	Product ID (High)	High Byte of Product ID – idProduct field of *Standard Device Descriptor.*
0x06	Device Release (Low)	Low byte of Device Release Number – bcdDevice field of *Standard Device Descriptor* (must be Binary Coded Decimal).
0x07	Device Release (High)	High byte of Device Release Number – bcdDevice field of *Standard Device Descriptor* (must be Binary Coded Decimal).
0x08 ~0x17	Device Serial Number	Device's Serial Number – the contents of string descriptor describing the device's serial number.
0x18	Length of Serial Number	Length of effective "Device Serial Number" stored in 0x08 to 0x17.
0x19	Filling	0x00
0x1A	Port Number	Number of Downstream Ports – bNbrPorts field of *Hub Descriptor.*
0x1B	Filling	0x00
0x1C	Device Removable	*DeviceRemovable* field of Hub Descriptor – indicates if a port has a removable device attached. If bit *N* is set to 1, then the device on Downstream Facing Port N is Non-Removable. Otherwise, it is removable. Bit 0 is reserved and should be 0.
0x1D	Filling	0x00
0x1E	Device Attributes	Bit 0: Port Indicators Support, bit 7 of *wHubCharacteristics* field of Hub Descriptor – 0: Port Indicators are not supported on its Downstream Facing Ports and PORT_INDICATOR request has no effect. 1: Port Indicators are supported on its Downstream Facing Ports and PORT_INDICATOR request controls the indicators. Bit 1: Identifies a Compound Device, bit 2 of *wHubCharacteristics* field of Hub Descriptor – 0: Hub is not part of a compound device. 1: Hub is part of a compound device. Bit 2: Maximum current requirements of the Hub Controller electronics, *bHubContrCurrent* field of Hub Descriptor – 0: 200mA. 1: 500mA. Bit 3 to 7 are reserved, must be 0s.
0x1F	Check Sum	The 8-bit sum of all values from 0x00 to 0x1E.

The first two bytes are the check code for the existence of EEPROM; their value must be 0x1A40. Other values will cause FE2.1's EEPROM loading mechanism to conclude that the contents of this EEPROM are unusable and FE2.1 will use default values instead.

The string descriptor for device's serial number can be defined by *Device Serial Number* and *Length of Serial Number* fields of the EEPROM – address 0x08 to 0x18. Length of Serial Number field – address 0x18 – defines the number of digits, while Device Serial Number field – address 0x08 to 0x17 – specifies the serial number in ASCII code. The space after the specified number of digits should be filled with Null – 0x00. For example, if the serial number is "A090108F4", then the EEPROM should be:

0x08	0x41 (A)	0x30 (0)	0x39 (9)	0x30 (0)	0x31 (1)	0x30 (0)	0x38 (8)	0x46 (F)
0x10	0x34 (4)	0x00 (Null)	0x00 (Null)	0x00 (Null)	0x00 (Null)	0x00 (Null)	0x00 (Null)	0x00 (Null)
0x18	0x09							

The last byte – address 0x1F – is a checksum made up of the sum of all values from 0x00 to 0x1E. The values of checksum must match with FE2.1's data from EEPROM for the contents of the EEPROM to be usable. Otherwise, FE2.1's loading mechanism will discard the values from EEPROM and FE2.1 will use default values instead.

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	TS	-55	+150	°C
5V Power Supply Voltage	VD5	0	+5.5	V
3.3V Power Supply Voltage	VD33	0	+3.6	V
ESD Human Body Mode		-2000	2000	V
ESD Charged Device Mode		-500	500	V
Latch Up		-200	200	mA

Note1: This is the rated value that MUST NOT be exceeded, even for a moment, to maintain life and reliability.
Note2: If power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off, clamp circuit is advised.

Recommended Operating Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	TA	0		70	°C
Operating voltage (5V power supply)	VD5	4.5	5.0	5.5	V
Operating voltage (3.3V power supply)	VD33	3.0	3.3	3.6	V
Power Ramp Up (10% ~ 90%)	TRUP	0.2		10	ms
LOW level voltage of digital input	VIL	-0.3		0.8	V
HIGH level voltage of digital input	VIH	2.0		5.5	V
LOW level voltage of digital output@4mA	VOL			0.4	V
HIGH level voltage of digital output@4mA	VOH	2.4			V
XIN input capacitance	Cin		32		pF

Note1: Operating temperature TA is measured in still air.

Extended Operating Ranges

Products with order code of CQFP48AT and CQFP48ABT are Final Tested (FT) at *Room Temperature, 85°C,* and *-40°C*.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature	TA	-40	25	85	°C

Note1: Operating temperature TA is measured in still air.

Power Consumption

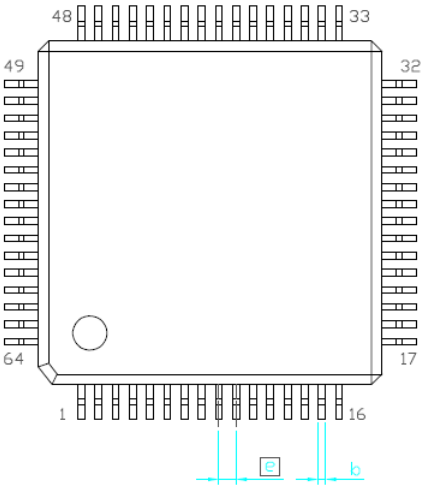
DC Supply Current

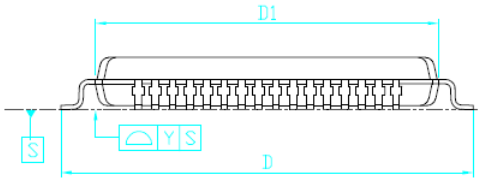
Symbol	Condition			Typical	Unit
	Active	Host	Devices		
I_suspend	Suspend			600	uA
Icc	7	Full-Speed	7x Full-Speed	39	mA
		High-Speed	7x High-Speed	158	mA
		High-Speed	7x Full-Speed	55	mA
	6	Full-Speed	6x Full-Speed	39	mA
		High-Speed	6x High-Speed	144	mA
		High-Speed	6x Full-Speed	55	mA
	5	Full-Speed	5x Full-Speed	39	mA
		High-Speed	5x High-Speed	129	mA
		High-Speed	5x Full-Speed	55	mA
	4	Full-Speed	4x Full-Speed	39	mA
		High-Speed	4x High-Speed	114	mA
		High-Speed	4x Full-Speed	55	mA
	3	Full-Speed	3x Full-Speed	39	mA
		High-Speed	3x High-Speed	99	mA
		High-Speed	3x Full-Speed	55	mA
	2	Full-Speed	2x Full-Speed	39	mA
		High-Speed	2x High-Speed	84	mA
		High-Speed	2x Full-Speed	54	mA
	1	Full-Speed	1x Full-Speed	39	mA
		High-Speed	1x High-Speed	69	mA
		High-Speed	1x Full-Speed	54	mA
	No active	Full-Speed	None	39	mA
		High-Speed	None	54	mA

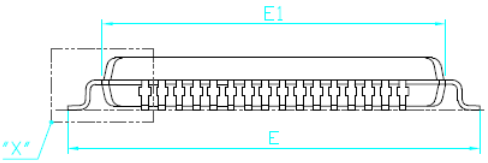
Note1: The power consumption is measured when the bus is in IDLE state – there are no activities other than the Start-Of-Frame (SOF) and INTERRUPT-IN packets for the hub itself on the bus. The peak power consumption varies depending on the system configuration, type of operations, and overall bus utilization.

PACKAGE DRAWING I – 64-PIN LQFP

(Body Size: 10 x 10 mm)

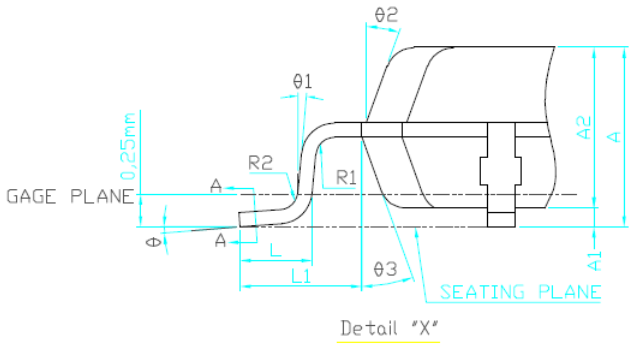


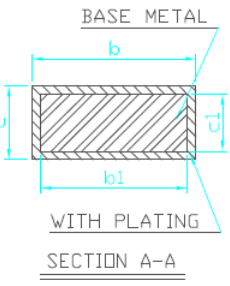




	SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
		MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
	A			1.60			63.0
3	A1	0.05	0.10	0.15	2.0	3.9	5.9
	A2	1.35	1.40	1.45	53.1	55.1	57.1
	b	0.17	0.22	0.27	6.7	8.7	10.6
	b1	0.17	0.20	0.23	6.7	7.9	9.1
	c	0.09		0.20	3.5		7.9
	c1	0.09		0.16	3.5		6.3
3,2	D	11.85	12.00	12.15	466.5	472.4	478.3
2	D1	9.90	10.00	10.10	389.8	393.7	397.6
3,2	E	11.85	12.00	12.15	466.5	472.4	478.3
2	E1	9.90	10.00	10.10	389.8	393.7	397.6
3	e	0.45	0.50	0.55	17.7	19.7	21.7
	L	0.45	0.60	0.75	17.7	23.6	29.5
3	L1	0.85	1.00	1.15	33.5	39.4	45.3
	R1	0.08			3.1		
	R2	0.08		0.20	3.1		7.9
4	Y			0.08			3.1
	θ	0°	3.5°	7°	0°	3.5°	7°
	θ1	0°			0°		
	θ2	11°	12°	13°	11°	12°	13°
	θ3	11°	12°	13°	11°	12°	13°

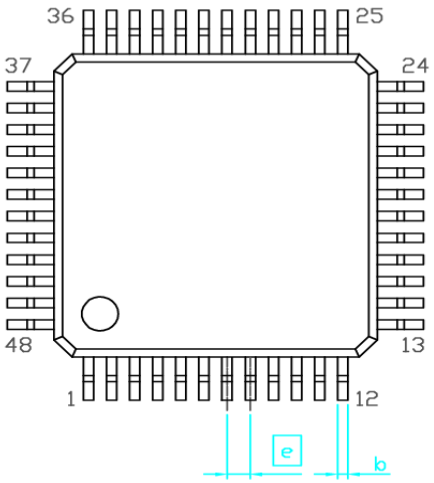
NOTES:
1.REFER TO JEDEC MS-026 (ISSUE D) / BCD
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE
MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED
THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.



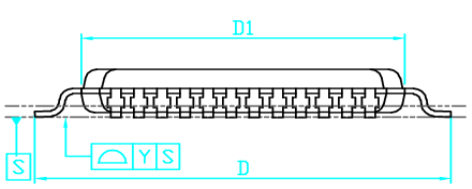


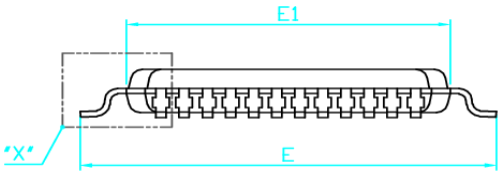
Package Drawing II – 48-pin LQFP

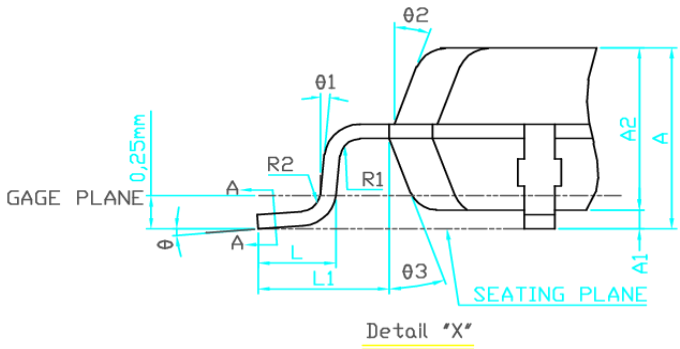
(Body Size: 7 x 7 mm)

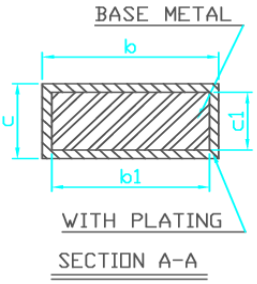


SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63.0
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	1.35	1.40	1.45	53.1	55.1	57.1
b	0.17	0.22	0.27	6.7	8.7	10.6
b1	0.17	0.20	0.23	6.7	7.9	9.1
c	0.09		0.20	3.5		7.9
c1	0.09		0.16	3.5		6.3
D	8.90	9.00	9.10	350.4	354.3	358.3
D1	6.90	7.00	7.10	271.7	275.6	279.5
E	8.90	9.00	9.10	350.4	354.3	358.3
E1	6.90	7.00	7.10	271.7	275.6	279.5
e	0.45	0.50	0.55	17.7	19.7	21.7
L	0.50	0.60	0.70	19.7	23.6	27.6
L1	0.85	1.00	1.15	33.5	39.4	45.3
R1	0.08			3.1		
R2	0.08		0.20	3.1		7.9
Y			0.08			3.1
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°









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