UMW FDS8949

Dual 40V N-Channel MOSFET

1.Features

These N-channel Logic Level MOSFETS has been especially tailoredto minimize the on-state resistance and yet maintainsuperior switching.

2.1 Features

- $V_{DS\ (V)}$=40V
- I_D=6A
- $R_{DS(ON)}$＜29mΩ(V_{GS}=10V)
- $R_{DS(ON)}$＜36mΩ(V_{GS}=4.5V)

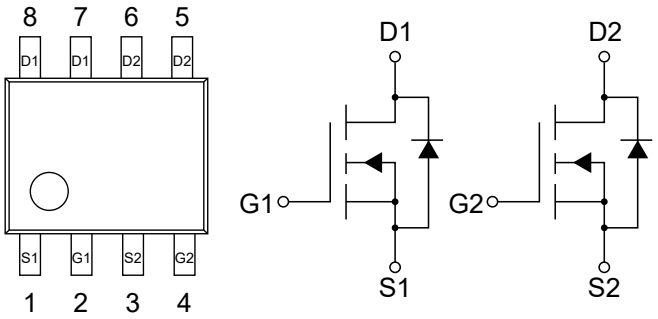
2.2 Features

- High power and current handling capability
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low gate charge
- RoHS compliant

3.Pinning Information

Pin	Symbol	Description
2,4	G1,G2	GATE
1,3	S1,S2	SOURCE
5,6,7,8	D1,D2	DRAIN

SOP-8



4.Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Value	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current – Continuous	(Note 1a)	I_D	6	A
– Pulsed			20	
Drain-Source Avalanche Energy	(Note 3)	E_{AS}	26	W
Power Dissipation for Dual Operation		P_D	2	W
Power Dissipation for Single Operation	(Note 1a)		1.6	W
	(Note 1b)		0.9	mJ
Storage Junction Temperature Range		T_J, T_{STG}	-55 to 150	°C

5.Thermal Characteristics

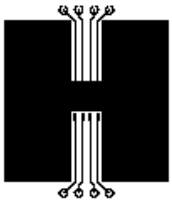
Parameter	Symbol	Rating	Units
Thermal Resistance, Junction-to-Ambient (Note 1a)	$R_{\theta JA}$	81	°C/W
Thermal Resistance, Junction-to-Case (Note 1b)	$R_{\theta JA}$	135	°C/W
Thermal Resistance, Junction-to-Case (Note 1)	$R_{\theta JC}$	40	°C/W

6.Electrical Characteristics (T_A=25°C unless otherwise noted)

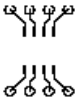
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	40			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D=250μA Referenced to 25°C		33		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=32V, V_{GS}=0V			1	μA
		T_J=55°C			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1	1.9	3	V
Gate to Source Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D=250μA Referenced to 25°C		-4.6		mV/°C
Drain to Source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=6A		21	29	mΩ
		V_{GS}=4.5V, I_D=4.5A		26	36	mΩ
Forward Transconductance	g_{FS}	V_{DS}=10, I_D=6V		22		S
Input Capacitance	C_{iss}	V_{DS}=20V,V_{GS}=0V,f =1MHz		715	955	pF
Output Capacitance	C_{oss}			105	140	pF
Reverse Transfer Capacitance	C_{rss}			60	90	pF
Gate Resistance	R_G	f =1MHz		1.1		Ω
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=20V, I_D=1A V_{GS}=10V, R_{GEN}=6Ω		9	18	ns
Rise Time	t_r			5	10	ns
Turn-Off DelayTime	$t_{D(off)}$			23	37	ns
Fall Time	t_f			3	6	ns
Total Gate Charge	Q_g	V_{DS}=20V, I_D=6A V_{GS}=5V		7.7	11	nC
Gate to Source Charge	Q_{gs}			2.4		nC
Gate to Drain “Miller” Charge	Q_{gd}			2.8		nC
Source to Drain Diode Forward Voltage	V_{SD}			0.8	1.2	V
Reverse Recovery Time (note 3)	t_{rr}	V_{GS}=0V, I_S=6A (Note 2)		17	26	ns
Reverse Recovery Charge	Q_{rr}	I_F=6A, di_F/d_t=100A/μs		7	11	nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 81°C/W when mounted on a $1in^2$ pad of 2 oz copper



b) 135°C/W when mounted on a minimum pad

2 Test: Pulse Width < 300μs, Duty Cycle < 2.0%

3 Starting T_J =25°C, L=1mH, I_{AS}=7.3A, V_{DD}=40V, V_{GS}=10V

7.1Typical Characteristics

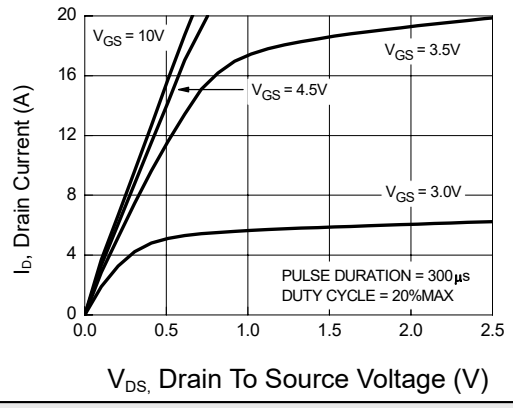


Figure 1: On-Region Characteristics

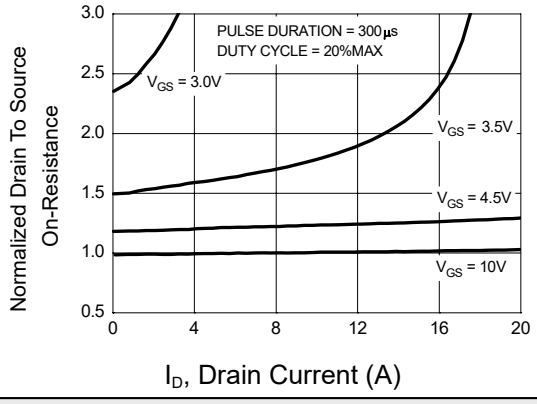


Figure 2: Normalized On-Resistance vs Drain Current and Gate Voltage

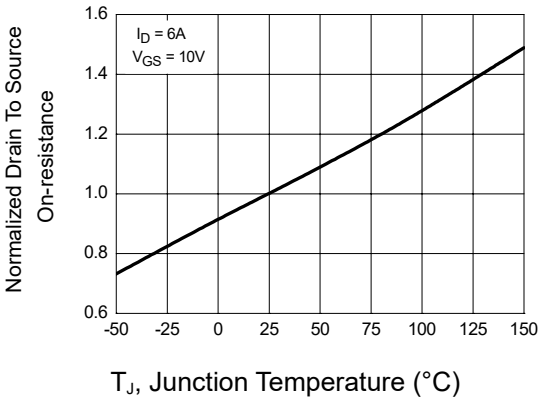


Figure 3: Normalized On Resistance vs Junction Temperature

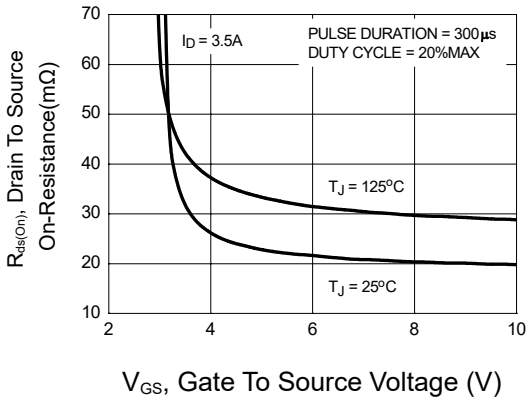


Figure 4: On-Resistance vs Gate to Source Voltage

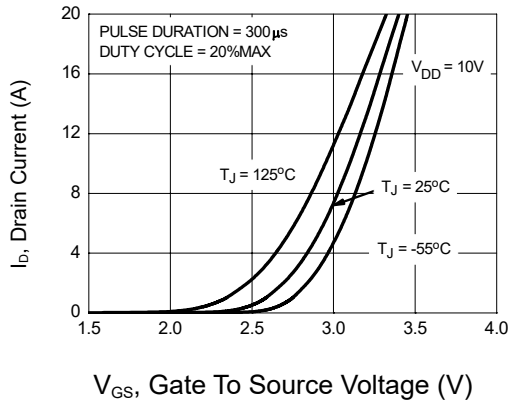


Figure 5: Transfer Characteristics

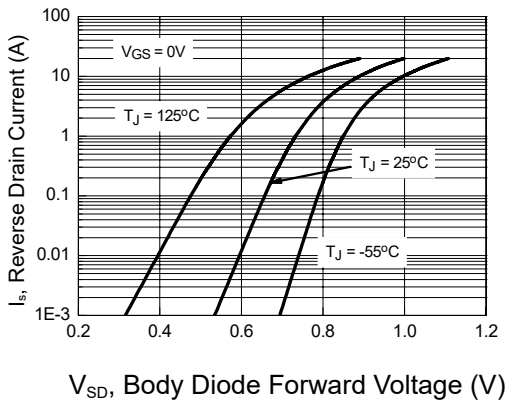


Figure 6: Source to Drain Diode Forward Voltage vs Source Current

7.2Typical Characteristics

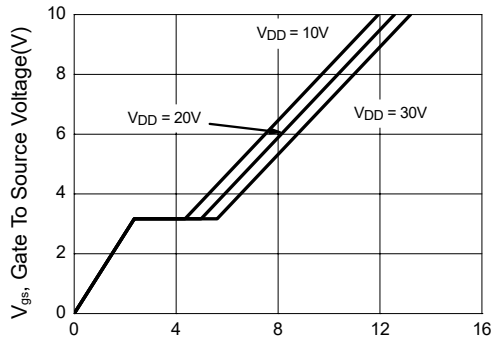


Figure 7: Gate Charge Characteristics

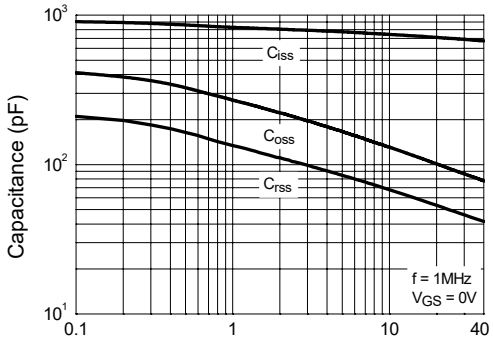


Figure 8: Capacitance vs Drain to Source Voltage

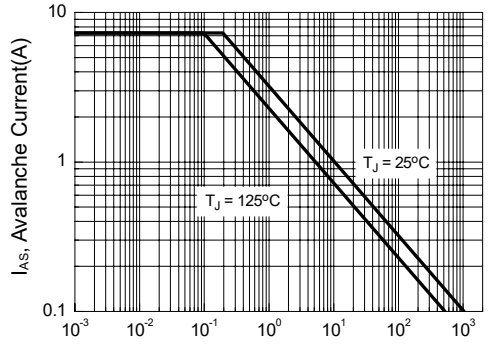


Figure 9: Unclamped Inductive Switching Capability

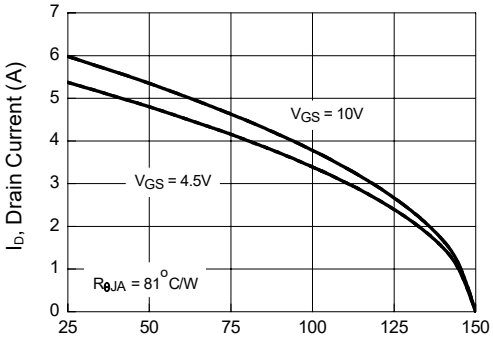


Figure 10: Maximum Continuous Drain Current vs Case Temperature

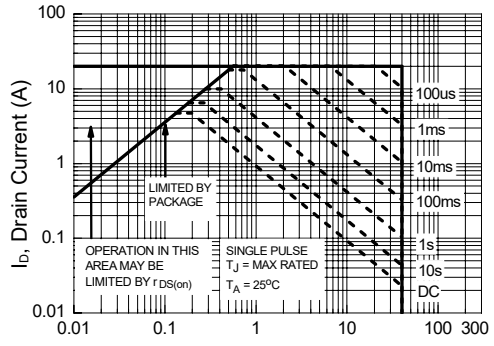


Figure 11: Forward Bias Safe Operating Area

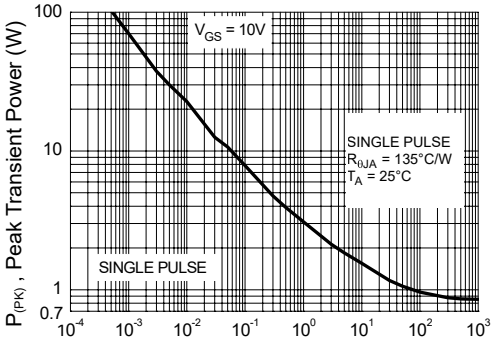


Figure 12: Single Pulse Maximum Power Dissipation

7.3Typical Characteristics

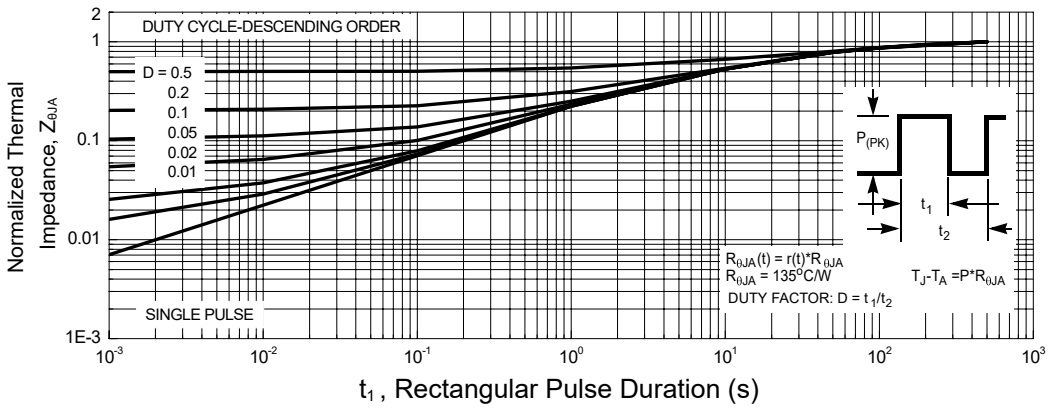
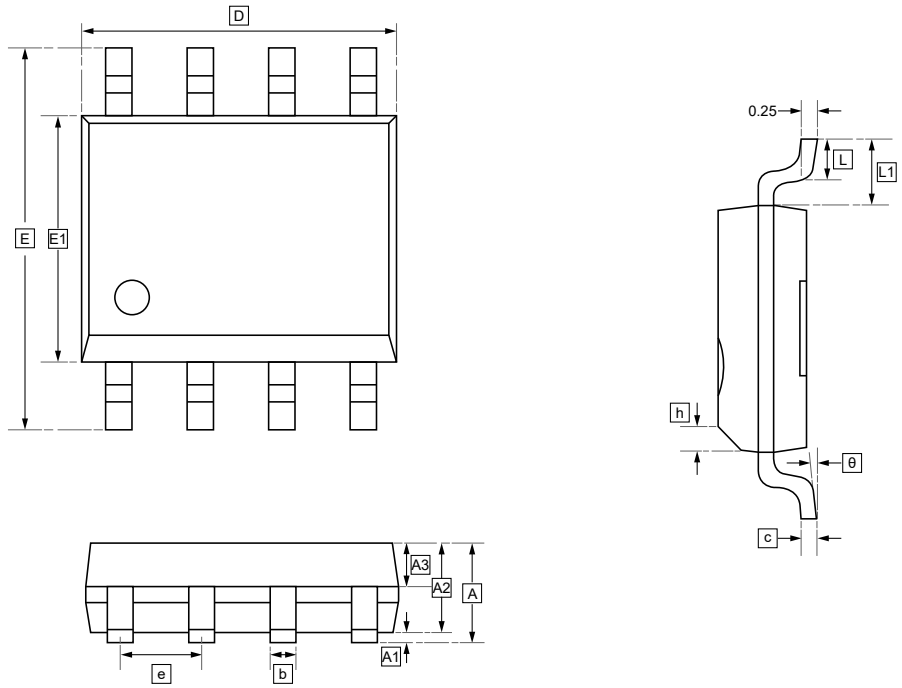


Figure 13: Transient Thermal Response Curve

8.SOP-8 Package Outline Dimensions

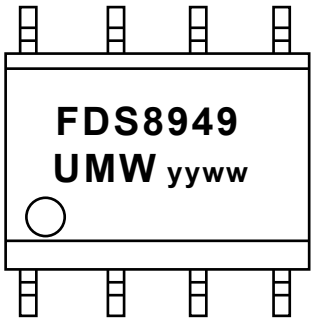


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.70	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.10	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDS8949	SOP-8	3000	Tape and reel

10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.