UMW FDS8978

30V N-Channel MOSFET

1.Features

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

2.1Features

- $V_{DS\ (V)}$=30V
- I_D=7.5A
- $R_{DS(ON)}$<18mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<21mΩ(V_{GS}=4.5V)
- Low Gate Charge

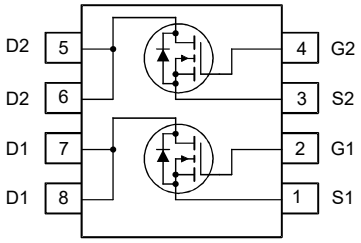
2.2Features

- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- High Power and Current Handling Capability

3.Pinning information

Pin	Symbol	Description
1,3	S	SOURCE
2,4	G	GATE
5,6,7,8	D	DRAIN

SOP-8



4.Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GS}	±20	
Drain Current Continuous (T_A=25°C, V_{GS}=10V, $R_{\theta JA}$=50°C/W)	I_D	7.5	A
Continuous (T_A=25°C, V_{GS}=4.5V, $R_{\theta JA}$=50°C/W)		6.9	
Pulsed		49	
Single Pulse Avalanche Energy (Note 1)	E_{AS}	57	mJ
Power Dissipation	P_D	1.6	W
Derate above 25°C		13	mW/°C
Storage Temperature	T_J,T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Resistance, Junction to Case (Note 2)	$R_{\theta JC}$	40	°C/W
Thermal Resistance, Junction to Ambient (Note 2a)	$R_{\theta JA}$	78	°C/W
Thermal Resistance, Junction to Ambient (Note 2b)	$R_{\theta JA}$	135	°C/W

Notes:

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Starting T_J=25°C, L=1mH, I_{AS}=7.5A, V_{DD}=30V, V_{GS}=10V.

2. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.

$R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

a. 78°C/W when mounted on a 0.5 in^2 pad of 2 oz copper.

b. 125°C/W when mounted on a 0.02 in^2 pad of 2 oz copper.

c. 135°C/W when mounted on a minimum pad.

6.Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V, V_{GS}=0V			1	μA
		V_{DS}=24V, V_{GS}=0V, T_J=150°C			250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V			±100	nA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.2		2.5	V
Drain to Source On Resistance	$R_{DS(ON)}$	I_D=7.5A, V_{GS}=10V		14	18	mΩ
		I_D=6.9A, V_{GS}=4.5V		17	21	mΩ
		I_D=7.5A, V_{GS}=10V, T_C=150°C		22	29	mΩ
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V, f=1MHz		907	1270	pF
Output Capacitance	C_{oss}			191		pF
Reverse Transfer Capacitance	C_{rss}			112		pF
Gate Resistance	R_g	V_{GS}=0.5V, f=1MHz		1.2	4	Ω
Total Gate Charge at 10V	$Q_{g(TOT)}$	V_{GS}=0V to 10V, V_{DD}=15V		17	26	nC
Total Gate Charge at 5V	$Q_{g(5)}$	V_{GS}=0V to 5V, I_D=7.5A		9	14	nC
Gate to Source Gate Charge	Q_{gs}	V_{DD}=15V, I_D=7.5A		2.3		nC
Gate Charge Threshold to Plateau	Q_{gs2}			1.5		nC
Gate to Drain “Miller” Charge	Q_{gd}			3.3		nC
Turn-On Time	t_{on}	V_{DD}=15V, I_D=7.5A, V_{GS}=10V, R_{GS}=16Ω		44	66	ns
Turn-On Delay Time	$t_{D(on)}$			7	10.5	ns
Rise Time	t_r			37	55.5	ns
Turn-Off Delay Time	$t_{D(off)}$			48	72	ns
Fall Time	t_f			24	36	ns
Turn-Off Time	t_{off}			72	108	ns

Source to Drain Diode Voltage	V_{SD}	I_{SD}=7.5A			1.25	V
		I_{SD}=2.1A			1	V
Reverse Recovery Time	t_{rr}	I_{SD}=7.5A, dI_{SD}/dt=100A/μs		19	25	ns
Reverse Recovered Charge	Q_{rr}	I_{SD}=7.5A, dI_{SD}/dt=100A/μs		10	13	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7.1Typical Characteristics

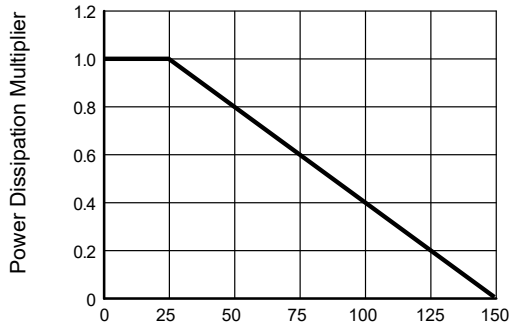


Figure 1: Normalized Power Dissipation vs Ambient Temperature

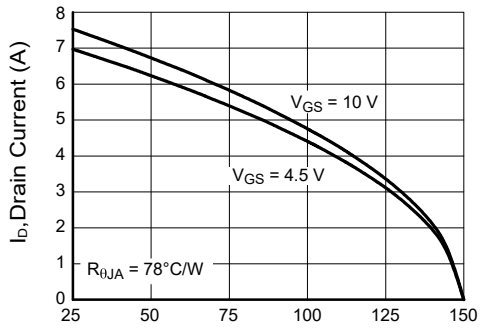


Figure 2: Maximum Continuous Drain Current vs Ambient Temperature



Figure 3: Normalized Maximum Transient Thermal Impedance

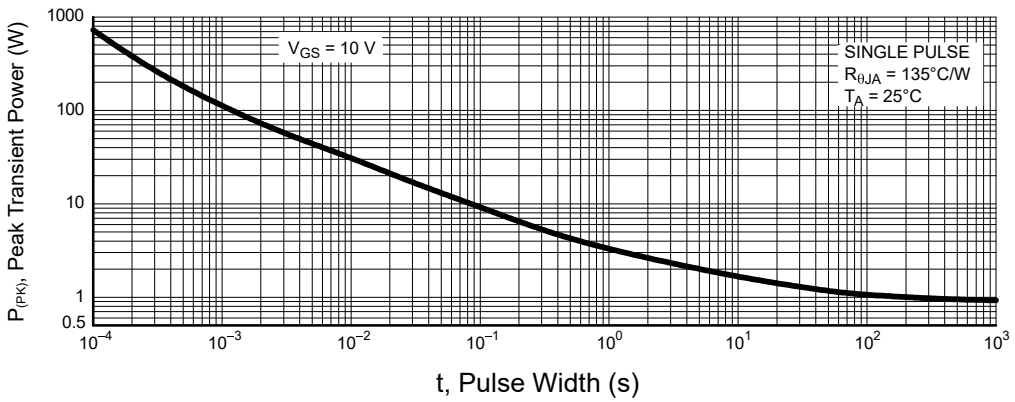
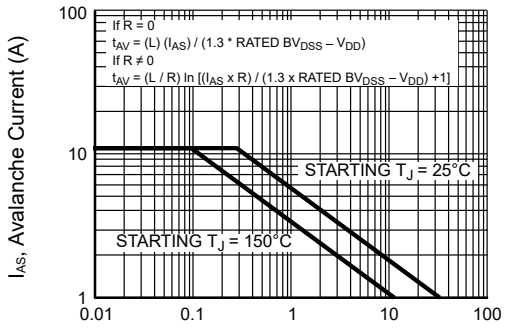


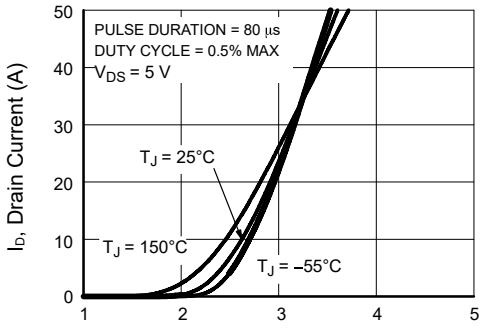
Figure 4: Single Pulse Maximum Power Dissipation

7.2Typical Characteristics



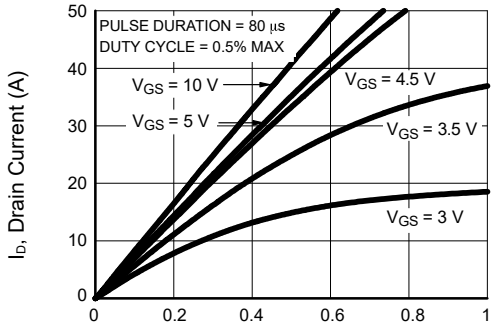
t_{AV}, Time In Avalanche(ms)

Figure 5: Unclamped Inductive Switching Capability



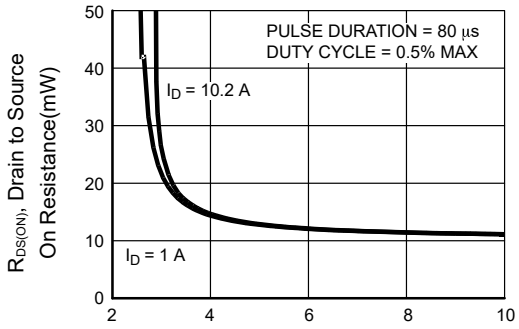
V_{DS},Drain to Source Voltage (V)

Figure 6: Transfer Characteristics



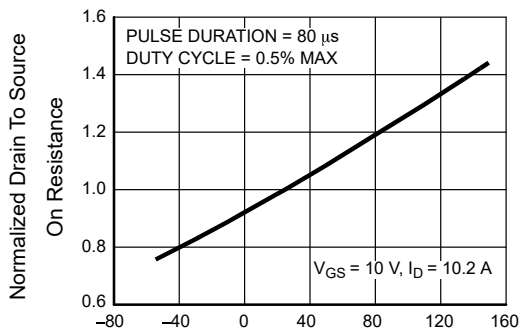
V_{DS},Drain to Source Voltage (V)

Figure 7: Saturation Characteristics



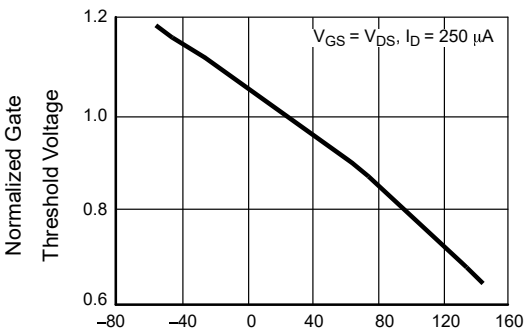
V_{GS},Gate to Source Voltage (V)

Figure 8: Drain to Source On Resistance vs Gate Voltage and Drain Current



T_J,Junction Temperature (°C)

Figure 9: Normalized Drain to Source On Resistance vs Junction Temperature



T_J,Junction Temperature (°C)

Figure 10: Normalized Gate Threshold Voltage vs Junction Temperature

7.3Typical Characteristics

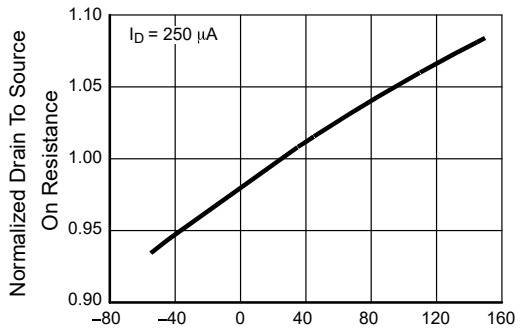


Figure 11: Normalized Drain to Source Breakdown Voltage vs Junction Temperature

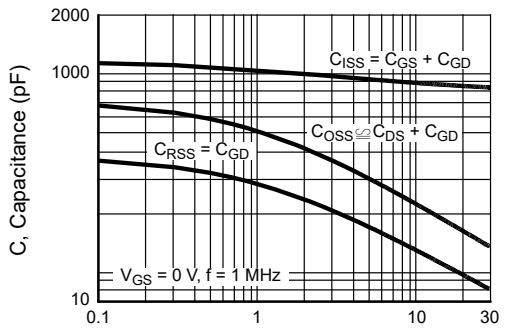


Figure 12: Capacitance vs Drain to Source Voltage

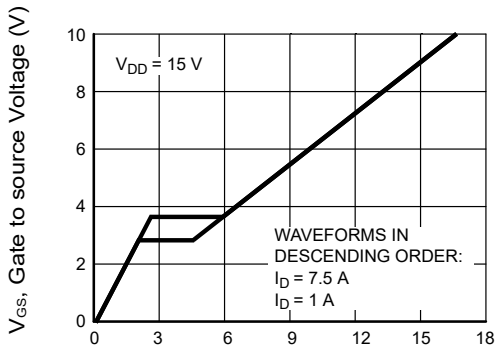


Figure 13: Gate Charge Waveforms for Constant Gate Currents

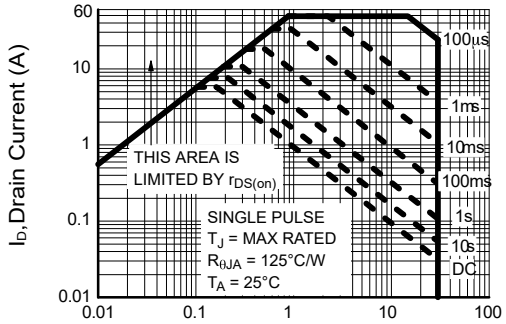
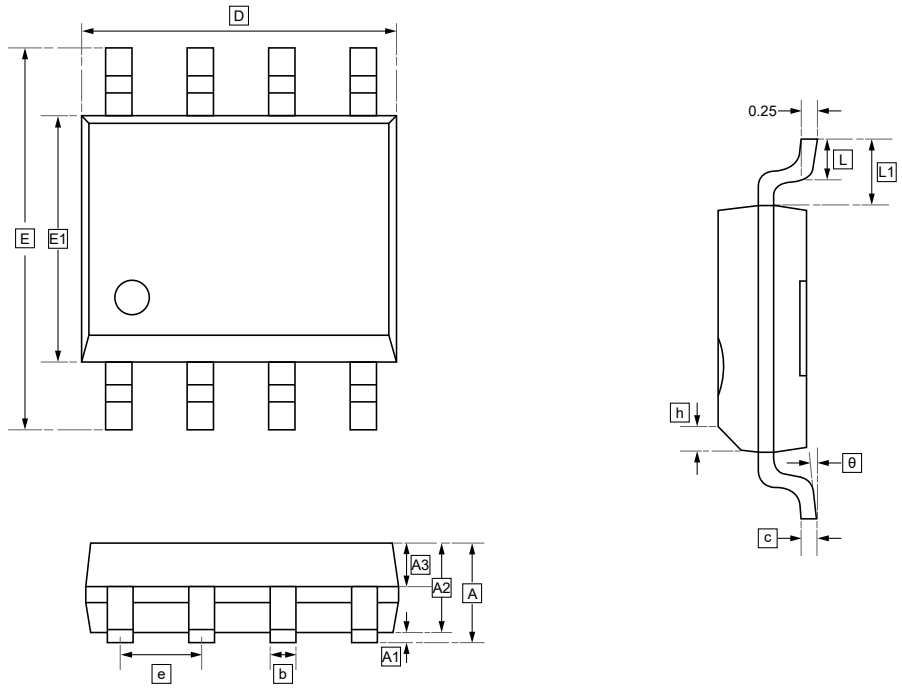


Figure 14: Forward Bias Safe Operating Area

8.SOP-8 Package Outline Dimensions

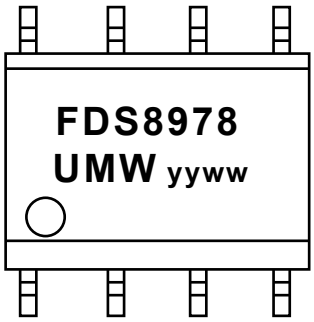


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.70	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.10	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDS8978	SOP-8	3000	Tape and reel

10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

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