Features

- 2.3V to 24V Input Voltage
- Up to 24V Output Voltage
- Integrated 80mΩ Power MOSFET
- 1MHz Fixed Switching Frequency
- Internal 4A Switch Current Limit
- Power Save Operation Mode at Light Load
- Internal 1.5mS Soft Start Time
- Up to 85% Efficiency@3.6V Input 12V Output
- Output Short Circuit Protection
- Output Over-Voltage Protection
- Thermal Shutdown Protection
- Output Adjustable from Input, Reference 0.6V
- -40°C to +85°C Temperature Range
- Available in SOT23-6 Package

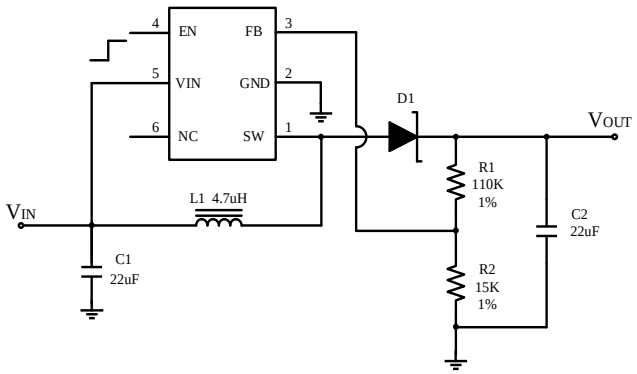
General Description

The ASP3710Z4 is a constant frequency, current mode step-up converter intended for small, low power applications. The ASP3710Z4 switches at 1MHz and allows the use of tiny, low-cost capacitors and inductors 2mm or less in height. Internal soft-start results in small inrush current and extends battery life.The ASP3710Z4 includes under-voltage lockout, current limiting, and thermal overload protection to prevent damage in the event of an output overload. The ASP3710Z4 is available in a small 6-pin SOT-23 package.

Applications

- Digital Set-top Box (STB)
- Tablet Personal Computer
- LCD Bias Supply
- Battery-Powered Equipment
- Portable Media Player (PMP)
- General Purposes

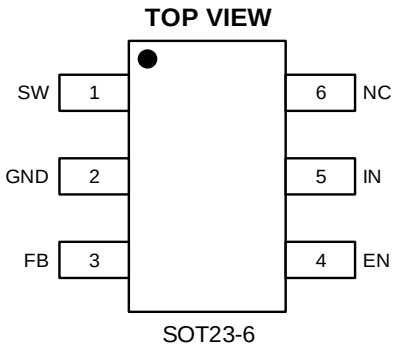
Typical Application Circuit



Typical Application Circuit

Package and Pin Description

Pin Configuration



Top Marking: CDWxx (device code: CDW, xx= lot number code)

Pin Description

Pin	Name	Function
1	SW	Power Switch Output. SW is the drain of the internal MOSFET switch. Connect the power inductor and output rectifier to SW
2	GND	Ground Pin
3	FB	Feedback Input. The FB voltage is 0.6V. Connect a resistor divider to FB
4	EN	Regulator On/Off Control Input. A high input at EN turns on the converter, and a low input turns it off. When not used, connect EN to the input supply for automatic startup
5	IN	Input Supply Pin
6	NC	Not Connection

Order Information (1)

Device Name	Package	Mark ID	Description	T/R Qty
ASP3710Z4-R	SOT23-6	CDWxx	ASP3710Z4 Boost, VIN=2.3-24V, VOUT=VIN->24V,1MHz,VFB=0.6V,SOT23-6.	3000PCS

Note (1): All ASDsemi parts are Pb-Free and adhere to the RoHS directive.

Specifications

Absolute Maximum Ratings (1) (2)

Item	Min	Max	Unit
V_{IN} EN voltage	-0.3	30	V
SW voltage	-0.3	V_{IN}+1.0	V
SW voltage (10ns transient)	-5	V_{IN}+2.0	V
All Other Pins	–0.3	6	V
Power dissipation (3)	Internally Limited		
Operating junction temperature, T_J	-40	150	°C
Storage temperature, T_{stg}	–65	150	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D\,(MAX)} = (T_{J(MAX)} - T_A)/R_{\theta JA}$. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=160°C (typical) and disengages at T_J= 130°C (typical).

ESD Ratings

Item	Description	Value	Unit
$V_{(ESD\text{-}HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
$V_{(ESD\text{-}CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±200	V
$I_{LATCH\text{-}UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±150	mA

Recommended Operating Conditions

Item	Min	Max	Unit
Operating junction temperature (1)	–40	125	°C
Operating temperature range	-40	85	°C
Input voltage V_{IN}	2.3	24	V
Output voltage V_{OUT}		24	V
Typical Output Current I_{OUT}	0	1	A

Note (1): All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard

Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Thermal Information

Item	Description	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)(2)	105	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.5	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board

Electrical Characteristics (1) (2)

V_{IN}=5V, T_A=25°C, unless otherwise specified.

Parameter	Test Conditions	Min	Typ.	Max	Unit
Input voltage range		2.3		24	V
Output voltage range				24	V
Supply Current (Quiescent)	V_{FB} =110%		150	200	μA
Supply Current (Shutdown)	V_{EN} =0 or EN = GND		0.1	1	μA
Feedback Voltage		588	600	612	mV
SW On Resistance			80	150	mΩ
Current Limit	Duty cycle=50%		4		A
Switching Frequency			1		MHz
Maximum Duty Cycle	V_{FB}=90%		90		%
Minimum On-Time			100		nS
EN Rising Threshold		1.1			V
EN Falling Threshold				0.9	V
EN Threshold Hysteresis			100		mV
Under-Voltage Lockout Threshold	Wake up V_{IN} Voltage			2.3	V
	Shutdown V_{IN} Voltage	1.5			V
	Hysteresis V_{IN} voltage		200		mV
Soft Start			1.5		mS
Thermal Shutdown			160		℃
Thermal Hysteresis			30		℃

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

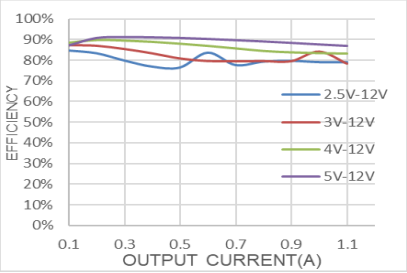
Typical Performance Characteristics (1) (2)

Note (1): Performance waveforms are tested on the evaluation board.

Note (2): V_{IN} =5V, V_{OUT}=12V, T_A = +25ºC, unless otherwise noted.

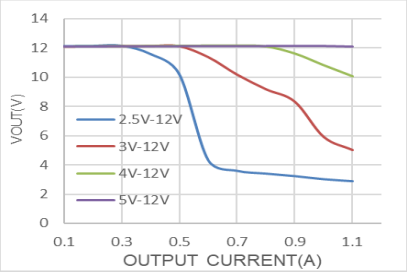
Efficiency vs. Load Current

V_{OUT}=12V



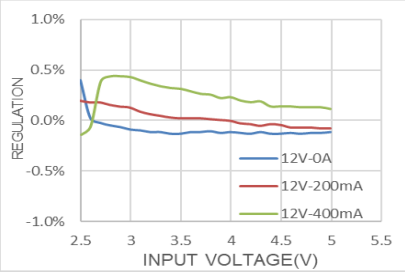
Load Regulation

V_{OUT}=12V



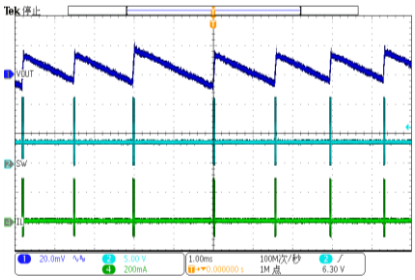
Line Regulation

V_{OUT}=12V



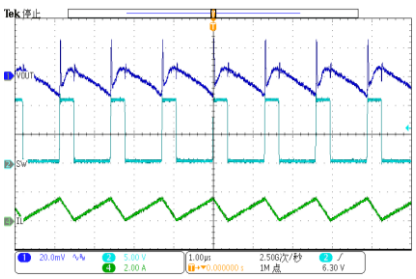
Output Ripple Voltage

V_{IN}=5V, V_{OUT}=12V, I_{OUT}=0A



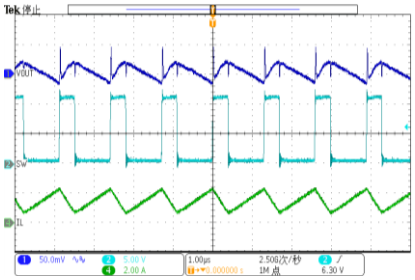
Output Ripple Voltage

V_{IN}=5V, V_{OUT}=12V, I_{OUT}=200mA



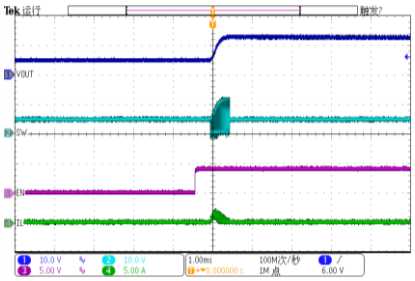
Output Ripple Voltage

V_{IN}=5V, V_{OUT}=12V, I_{OUT}=400mA



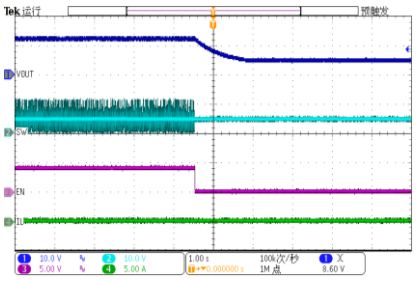
Enable Startup at No Load

V_{IN}=5V, V_{OUT}=12V



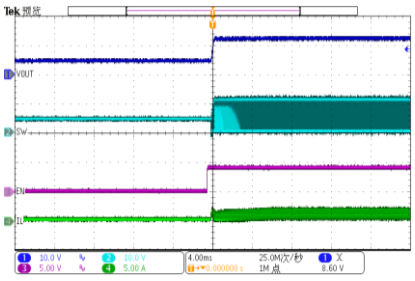
Enable Shutdown at No Load

V_{IN}=5V, V_{OUT}=12V



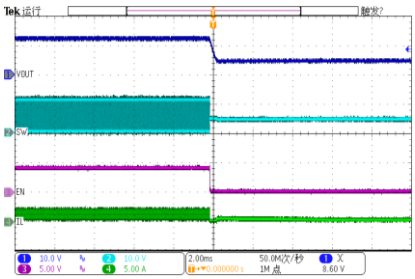
Enable Startup at Heavy Load

V_{IN}=5V, V_{OUT}=12V, I_{OUT}=400mA



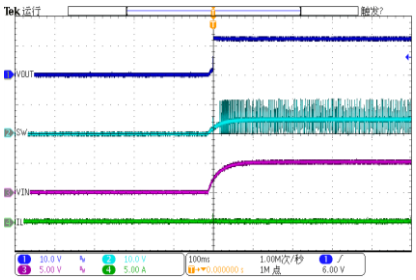
Enable Shutdown at Heavy Load

V_{IN}=5V, V_{OUT}=12V, I_{OUT}=400mA



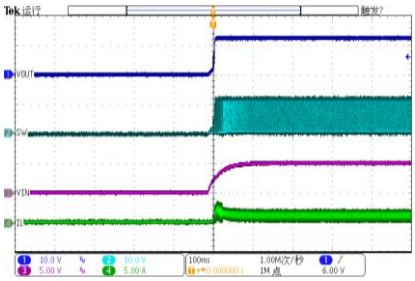
Power Up at No Load

V_{IN}=5V, V_{OUT}=12V, I_{OUT}=0A

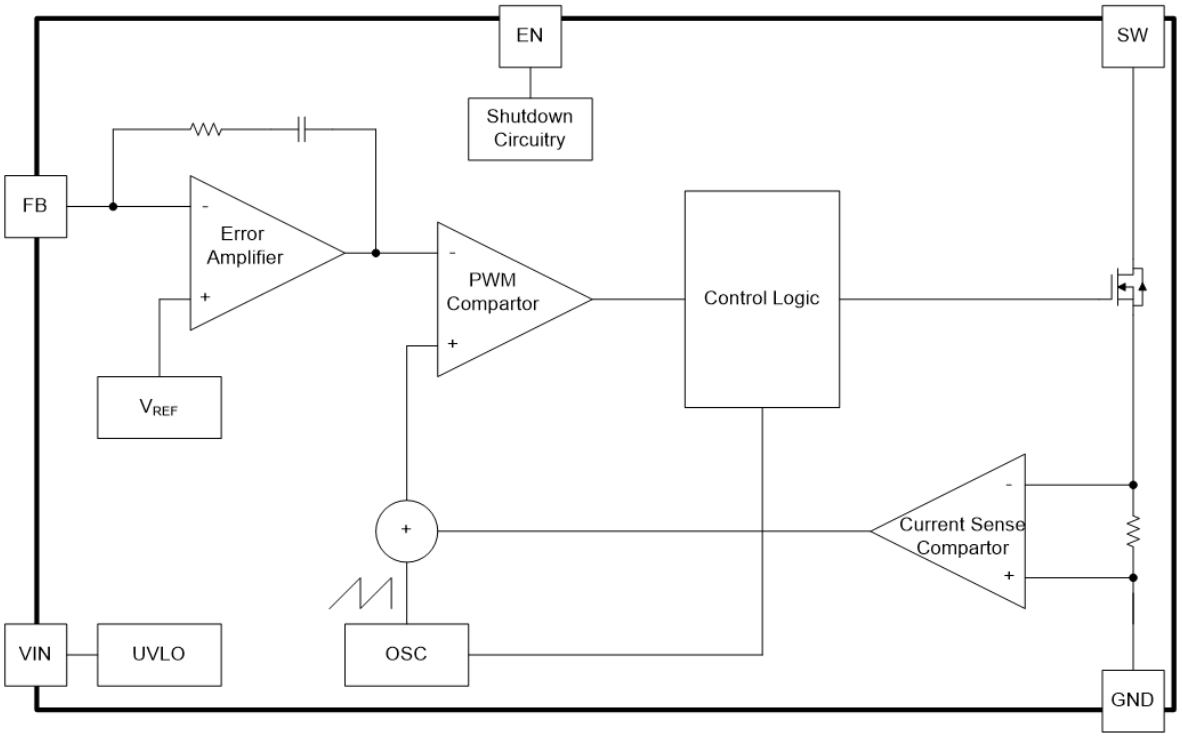


Power Up at Heavy Load

V_{IN}=5V, V_{OUT}=12V, I_{OUT}=400mA



Functional Block Diagram



Block Diagram

Functions Description

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

Enable and Disable

When the input voltage is above maximal UVLO rising threshold and the EN pin is pulled high, the ASP3710Z4 is enabled. When the EN pin is pulled low, the ASP3710Z4 goes into shutdown mode. In shutdown mode, less than 1μA input current is consumed.

Soft-Start

The ASP3710Z4 begins soft start when the EN pin is pulled high. at the beginning of the soft start period, the isolation FET is turned on slowly to charge the output capacitor. After the pre-charge phase, the ASP3710Z4 starts switching. This is called switching soft start phase. An internal soft start circuit limits the peak inductor current according to the output voltage. The switching soft start phase is about 1.5ms typically. The soft start function reduces the inrush current during startup.

Output Short Circuit Protection

When the VOUT pin is shorted to ground, the ASP3710Z4 stop switching. This function protects the device from being damaged when the output is shorted to ground.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, it shuts down the whole chip. When the temperature falls below its lower threshold (Typ. 130°C) the chip is enabled again.

PWM Mode

The ASP3710Z4 uses a quasi-constant 1MHz frequency pulse width modulation (PWM) at moderate to heavy load current. Based on the input voltage to output voltage ratio, a circuit predicts the required off-time. At the beginning of the switching cycle, the NMOS switching FET, shown in the functional block diagram, is turned on. The input voltage is applied across the inductor and the inductor current ramps up. In this phase, the output capacitor is discharged by the load current. When the inductor current hits the current threshold that is set by the output of the error amplifier, the PWM switch is turned off, and the power diode is forward-biased. The inductor transfers its stored energy to replenish the output capacitor and supply the load. When the off-time is expired, the next switching cycle starts again. The error amplifier compares the FB pin voltage with an internal reference voltage, and its output determines the inductor peak current.

The ASP3710Z4 has a built-in compensation circuit that can accommodate a wide range of input voltage, output voltage, inductor value and output capacitor value for stable operation.

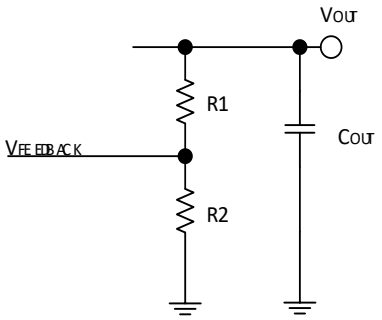
Power Save Mode

The ASP3710Z4 integrates a power save mode with pulse frequency modulation (PFM) to improve efficiency at light load. When the load current decreases, the inductor peak current set by the output of the error amplifier declines to regulate the output voltage. When the FB voltage hits the PFM reference voltage, the ASP3710Z4 goes into the power save mode. In the power save mode, when the FB voltage rises and hits the PFM reference voltage, the device continuous switching for several cycles because of the delay time of the internal comparator. Then it stops switching. The load is supplied by the output capacitor and the output voltage declines. When the FB voltage falls below the PFM reference voltage, after the delay time of the comparator, the device starts switching again to ramp up the output voltage.

Applications Information

Setting the Output Voltage

ASP3710Z4 are internally compensated and do not require external components to achieve stable operation. The output voltage can be programmed by resistor divider, as shown in Equation $V_{OUT} = V_{FB} \times \frac{R1+R2}{R2}$.



Inductor Selection

Because the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications, inductor value, saturation current, and dc resistance (DCR).

The ASP3710Z4 is designed to work with inductor values between 2.2μH and 22μH. Follow the Equation below to calculate the inductor's peak current for the application. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To have enough design margin, choose the inductor value with -30% tolerance, and a low power-conversion efficiency for the calculation. In a boost regulator, the inductor dc current can be calculated with Equation:

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}$$

Where

- V_{OUT} = output voltage
- I_{OUT} = output current
- V_{IN} = input voltage
- η = power conversion efficiency, use 80% for most applications

The inductor ripple current is calculated with the Equation 3 for an asynchronous boost converter in continuous conduction mode (CCM).

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times (V_{OUT} + V_{DIODE} - V_{IN})}{L \times F_S \times (V_{OUT} + V_{DIODE})}$$

Where

- $\Delta I_{L(P-P)}$ = inductor ripple current
- L = inductor value

- V_{IN} = input voltage
- V_{OUT} = output voltage
- V_{DIODE} = output diode forward voltage
- F_S = switching frequency, Hertz

Therefore, the inductor peak current is calculated with Equation:

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2}$$

Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. Bit in the same way, load transient response time is increased.

Because the ASP3710Z4 is for relatively small output current application, the inductor peak-to-peak current could be as high as 200% of the average current with a small inductor value, which means the ASP3710Z4 always works in DCM mode.

Input and Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{F_S \times V_{RIPPLE}}$$

Where

- D_{MAX} = maximum switching duty cycle
- I_{RIPPLE} = peak to peak output voltage ripple

The ESR impact on the output ripple must be considered if tantalum or aluminum electrolytic capacitors are used. Care must be taken when evaluating a ceramic capacitor's derating under dc bias, aging, and ac signal. For example, the dc bias can significantly reduce capacitance. A ceramic capacitor can lose more than 50% of its capacitance at its rated voltage. Therefore, always leave margin on the voltage rating to ensure adequate capacitance at the required output voltage.

It is recommended to use the output capacitor with effective capacitance in the range of 10μF to 22μF. The output capacitor affects the small signal control loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable. Increasing the output capacitor makes the output voltage ripple smaller in PWM mode.

For input capacitor, a ceramic capacitor with more than 1.0μF is enough for most applications.

Diode Selection

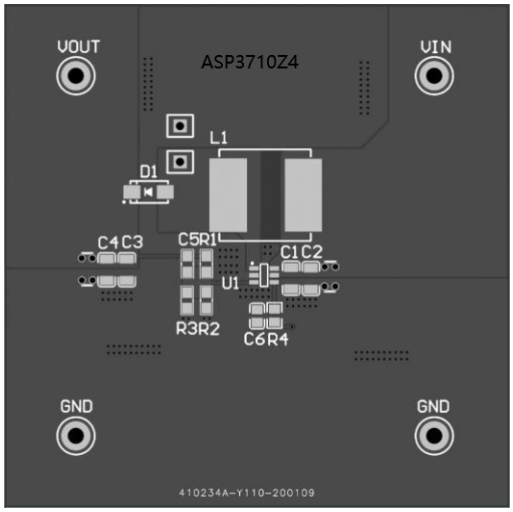
A Schottky diode should be used for the output diode. The forward current rating of the diode should be higher than the load current, and the reverse voltage rating must be higher than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

Layout Guidelines

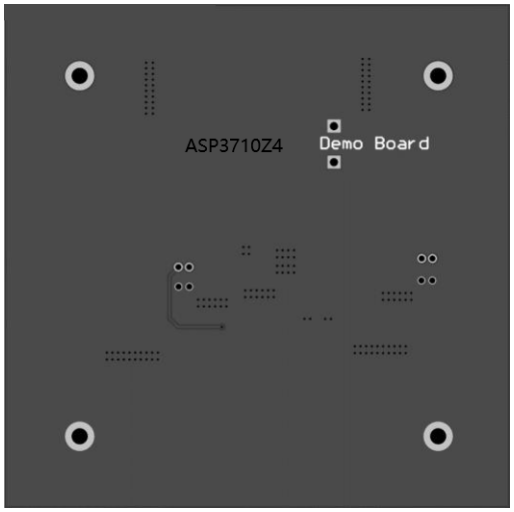
PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the CIN input capacitor, to the regulator VIN terminal, to the regulator SW terminal, to the inductor then out to the output capacitor COUT and load. The second loop starts from the output capacitor ground, to the regulator GND terminals, to the inductor and then out to COUT and the load. To minimize both loop areas the input capacitor should be placed as close as possible to the VIN terminal. Grounding for both the input and output capacitors should consist of a small localized topside plane that connects to GND. The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The SW terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with an enough width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW terminal. The inductors should be placed as close as possible to the SW terminals to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the FB terminal. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

Top Layer



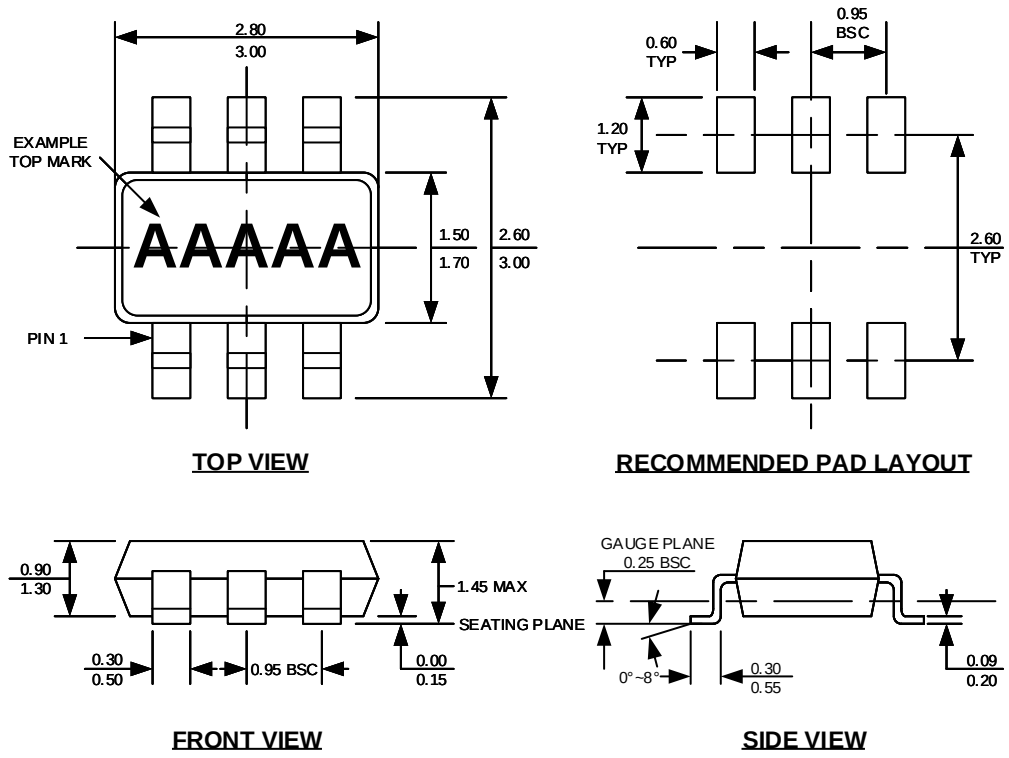
Bottom Layer



Sample Board Layout

Package Description

SOT23-6



NOTE:
1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.

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