UMW IRF7307TR

20V N-Channel MOSFET
-20V P-Channel MOSFET

1.Description

The SOP-8 has been modified through a customized leadtrame for enhanced thermal characteristics and multiple die capability making it ideal in a varietyof power applications. Withtheseimprovements. multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase. infra red. or wave soldering technigues. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.

2.1 Features

N-Ch:

- $V_{DS\ (V)}$=20V
- I_D=5.7A
- $R_{DS(ON)}$<53mΩ(V_{GS}=4.5)
- $R_{DS(ON)}$<70mΩ(V_{GS}=2.7V)

P-Ch:

- $V_{DS\ (V)}$=-20V
- I_D=-4.7A
- $R_{DS(ON)}$<100mΩ(V_{GS}=-4.5)
- $R_{DS(ON)}$<140mΩ(V_{GS}=-2.7V)

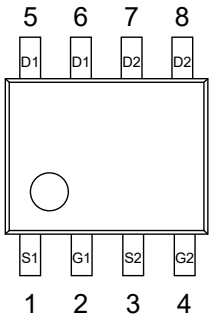
2.2 Features

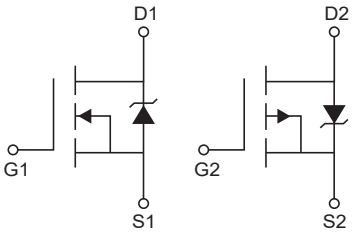
- Generation V Technology Ultra
- Low On-Resistance
- Dual N and P Channel Mosfet
- Surface Mount
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free

3.Pinning Information

Pin	Symbol	Description
2,4	G1,G2	GATE
1,3	S1,S2	SOURCE
5,6,7,8	D1,D2	DRAIN

SOP-8





4.Absolute Maximum Ratings T_A= 25°C

Parameter		Symbol	Max n-channel	Max p-channel	Units
10 Sec. Pulse Drain Current, V_{GS}=4.5V	T_A=25°C	I_D	5.7	-4.7	A
Continuous Drain Current, V_{GS}=4.5V	T_A=25°C		5.2	-4.3	A
Continuous Drain Current, V_{GS}=4.5V	T_A=70°C		4.1	-3.4	A
Pulsed Drain Current ①		I_{DM}	21	-17	A
Power Dissipation	T_A=25°C	P_D	2		W
Linear Derating Factor			0.016		W/°C
Gate-to-Source Voltage		V_{GS}	±12		V
Peak Diode Recovery dv/dt ②		dv/dt	5	-5	V/ns
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

5.Thermal resistance rating

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ④	$R_{\theta JA}$		62.5	°C/W

6.Electrical Characteristics T_J=25°C

Parameter	Symbol		Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	N-Ch	I_D=250μA, V_{GS}=0V	-20			V
		P-Ch	I_D=-250μA, V_{GS}=0V	20			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/T_J$	N-Ch	I_D=1mA,Reference to 25°C		0.044		V/°C
		P-Ch	I_D=-1mA,Reference to 25°C		-0.012		V/°C
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	N-Ch	V_{GS}=4.5V, I_D=2.6A ③			53	mΩ
			V_{GS}=2.7V, I_D=2.2A ③			70	mΩ
		P-Ch	V_{GS}=-4.5V, I_D=-2.2A ③			100	mΩ
			V_{GS}=-2.7V, I_D=-1.8A ③			140	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	N-Ch	V_{DS}=V_{GS}, I_D=250μA	0.7			V
		P-Ch	V_{DS}=V_{GS}, I_D=-250μA	-0.7			V
Forward Transconductance	g_{FS}	N-Ch	V_{DS}=15V, I_D=2.6A ③	8.3			S
		P-Ch	V_{DS}=-15V, I_D=-2.2A ③	4			S
Drain-to-Source Leakage Current	I_{DSS}	N-Ch	V_{DS}=16V, V_{GS}=0V			1	μA
		P-Ch	V_{DS}=-16V, V_{GS}=0V			-1	μA
		N-Ch	V_{DS}=16V, V_{GS}=0V, T_J=125°C			25	μA
		P-Ch	V_{DS}=-16V, V_{GS}=0V, T_J=125°C			-25	μA
Gate-to-Source Forward Leakage	I_{GSS}	N-P	V_{GS}=±12V			±100	nA
Total Gate Charge	Q_g	N-Ch	N-Channel			20	nC
		P-Ch	I_D=2.6A, V_{DS}=16V			22	nC
Gate-to-Source Charge	Q_{gs}	N-Ch	V_{GS}=4.5V			2.2	nC
		P-Ch	P-Channel			3.3	nC
Gate-to-Drain ("Miller") Charge	Q_{gd}	N-Ch	I_D=-2.2A			8	nC
		P-Ch	V_{DS}=-16V, V_{GS}=-4.5V			9	nC
Turn-On Delay Time	$t_{D(on)}$	N-Ch	N-Channel		9		ns
		P-Ch	V_{DD}=10V, I_D=2.6A		8.4		ns
Rise Time	t_r	N-Ch	R_G=6Ω, R_D=3.8Ω		42		ns
		P-Ch			26		ns

Turn-Off Delay Time	$t_{D(off)}$	N-Ch	P-Channel V_{DD}=-10V, I_D=-2.2A R_G=6Ω, R_D=4.5Ω		32		ns
		P-Ch			51		ns
Fall Time	t_f	N-Ch			51		ns
		P-Ch			33		ns
Internal Drain inductance	L_D	N-P	Between lead tipand center of die contact		4		nH
Internal Source inductance	L_S	N-P			6		nH
Input Capacitance	C_{iss}	N-Ch	N-Channel V_{GS}=0V, V_{DS}=15V, f=1.0MHz P-Channel V_{GS}=0V, V_{DS}=-15V, f=1.0MHz		660		pF
		P-Ch			610		pF
Output Capacitance	C_{oss}	N-Ch			280		pF
		P-Ch			310		pF
Reverse Transfer Capacitance	C_{rss}	N-Ch			140		pF
		P-Ch			170		pF
Source-Drain Ratings and Characteristics							
Continuous Source Current (Body Diode)	I_S	N-Ch				2.5	A
		P-Ch				-2.5	
Pulsed Source Current (Body Diode) ①	I_{SM}	N-Ch				21	
		P-Ch				-17	
Diode Forward Voltage	V_{SD}	N-Ch	T_J=25°C, I_S=1.8A, V_{GS}=0V ③			1	V
		P-Ch	T_J=25°C, I_S=-1.8A, V_{GS}=0V ③			-1	V
Reverse Recovery Time	t_{rr}	N-Ch	N-Channel:T_J=25°C I_F=2.6A,dI/dt=100A/μs P-Channel:T_J=25°C I_F=-2.2A, dI/dt=100A/μs ③		29	44	ns
		P-Ch			56	84	ns
Reverse Recovery Charge	Q_{rr}	N-Ch			22	33	nC
		P-Ch			71	110	nC
Forward Turn-On Time	t_{on}	N-Ch	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				
		P-Ch					

① Repetitive rating; pulse width limited bymax. junction temperature. (See fig. 23)

② N-Channel I_{SD}≤2.6A, di/dt ≤100Aμs, V_{DD}≤ $V_{BR(DSS)}$, T_J≤ 150°C.

P-Channel I_{SD}≤ -2.2A, di/dt ≤ 50A/μs, V_{DD}≤$V_{BR(DSS)}$, T_J≤ 150°C.

③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

④ Surface mounted on FR-4 board, t≤ 10sec.

7.1Typical Characterisitics

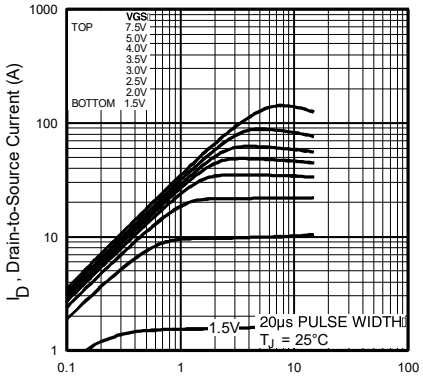


Fig 1. Typical Output Characteristics

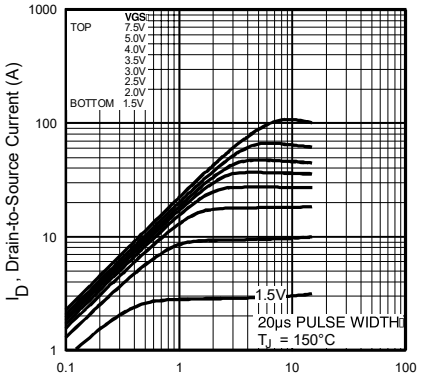


Fig 2. Typical Output Characteristics

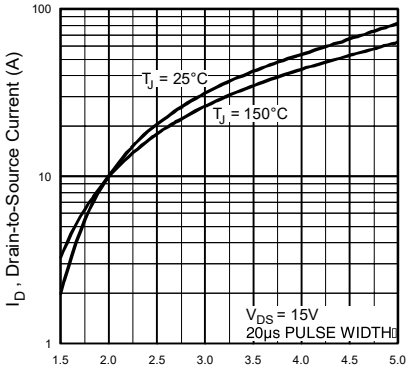


Fig 3. Typical Transfer Characteristics

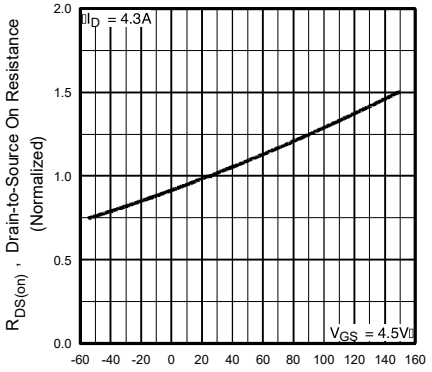


Fig 4. Nomalized On-ResistanceVs. Temperature

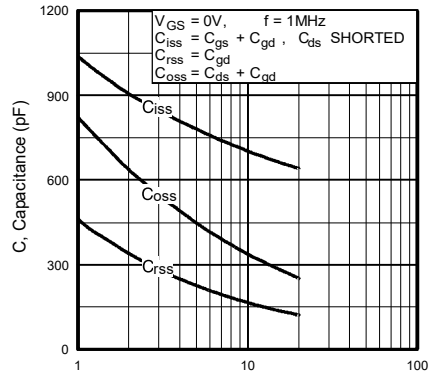


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

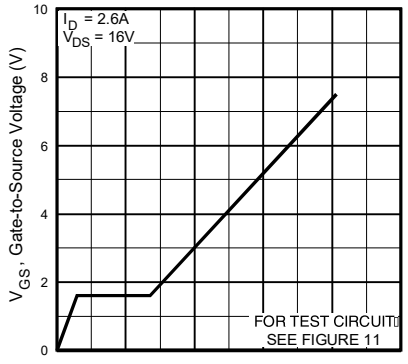


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

7.2Typical Characterisitics

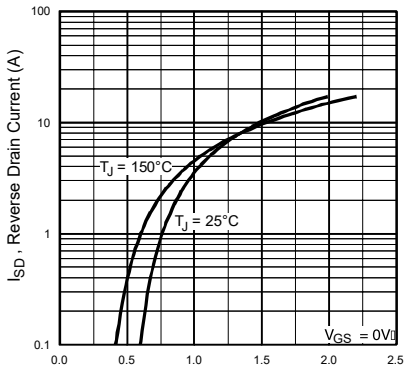


Fig 7. Typical Source-Drain Diode Forward Voltage

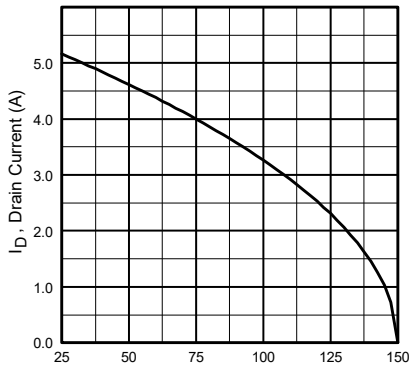


Fig 8. Maximum Drain Current Vs.AmbientTemperature

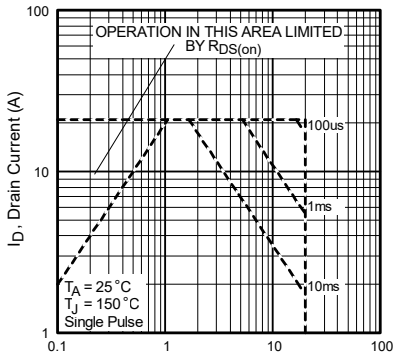


Fig 9. Maximum Safe Operating Area

7.3Typical Characterisitics

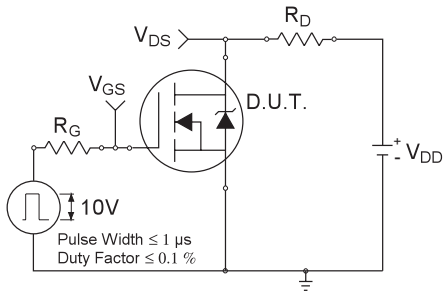


Fig 10a. Switching Time Test Circuit

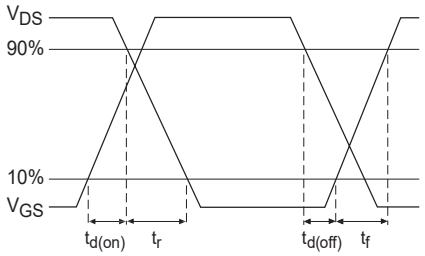


Fig 10b. Switching Time Waveforms

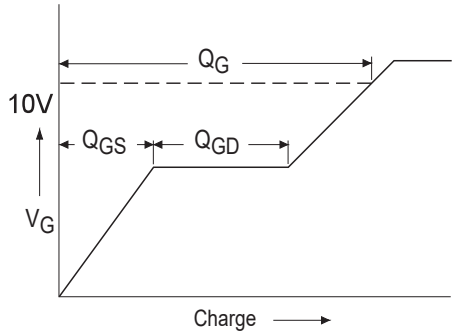


Fig 11a. Basic Gate Charge Wavefomm

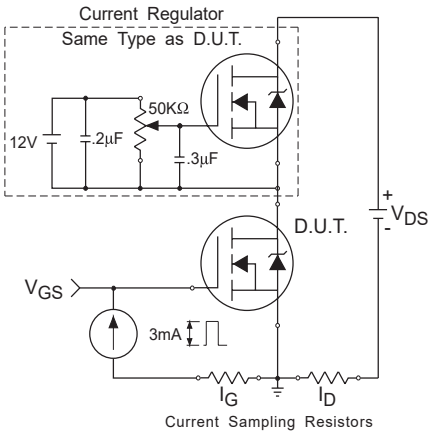


Fig 11b. Gate Charge Test Circuit

7.4Typical Characterisitics

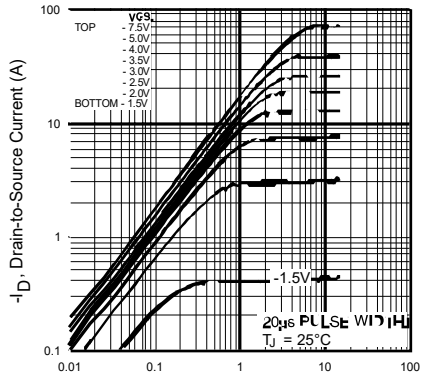


Fig 12. Typical Output Characteristics

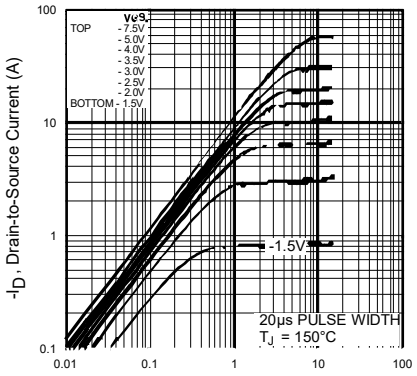


Fig 13. Typical Output Characteristics

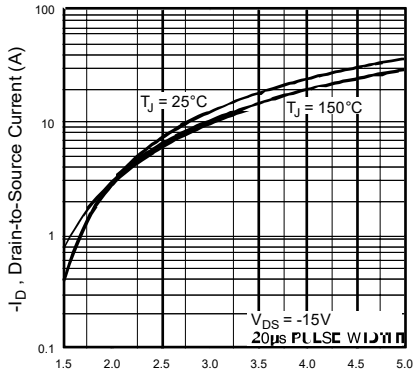


Fig 14. Typical Transfer Characteristics

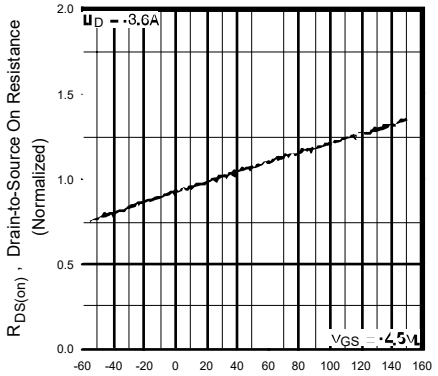


Fig 15. Nomalized On-ResistanceVs. Temperature

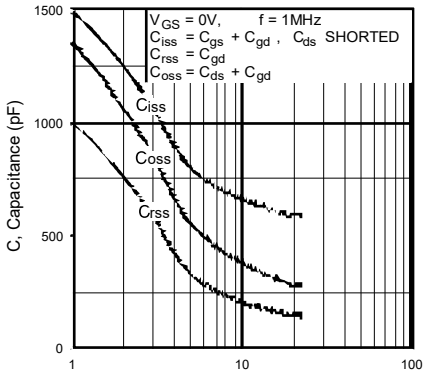


Fig 16. Typical Capacitance Vs. Drain-to-Source Voltage

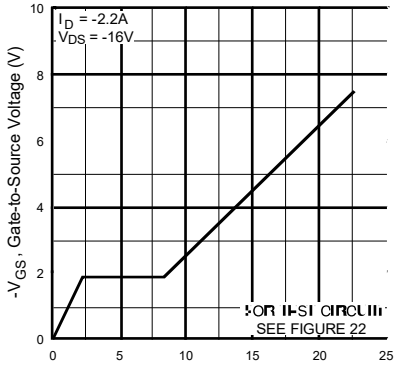


Fig 17. Typical Gate Charge Vs. Gate-to-Source Voltage

7.5Typical Characterisitics

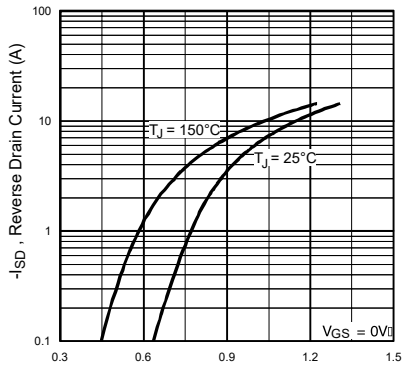


Fig 18. Typical Source-Drain Diode Forward Voltage

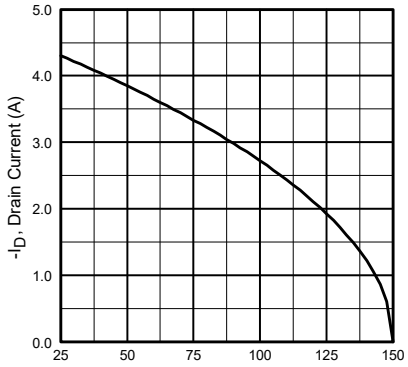


Fig 19. Maximum Drain Current Vs.AmbientTemperature

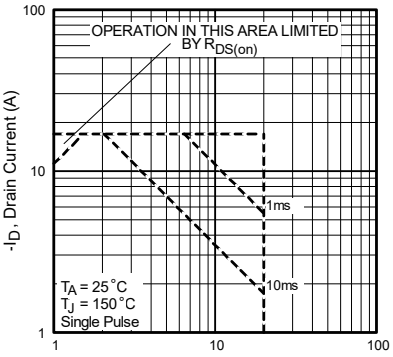


Fig 20. Maximum Safe Operating Area

7.6Typical Characterisitics

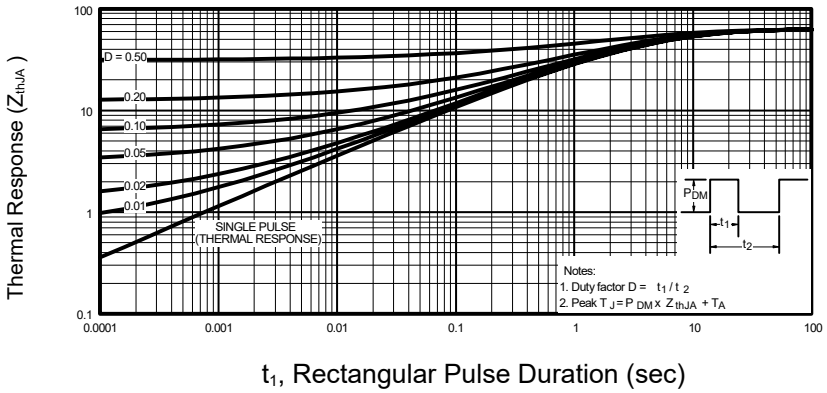


Fig 23. Maximum Effective Transient Themal Impedance, Junction-to-Ambient

7.7Typical Characterisitics

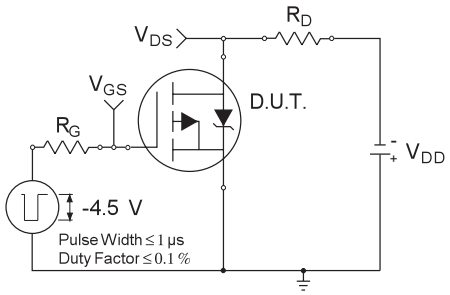


Fig 21a. Switching Time Test Circuit

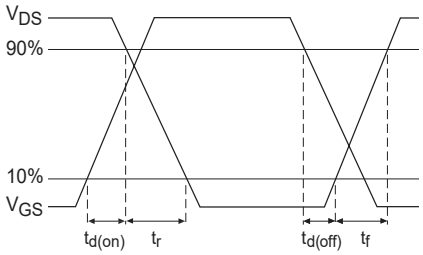


Fig 21b. Switching Time Waveforms

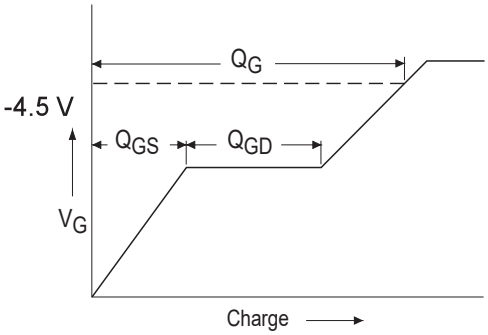


Fig 22a. Basic Gate Charge Wavefomm

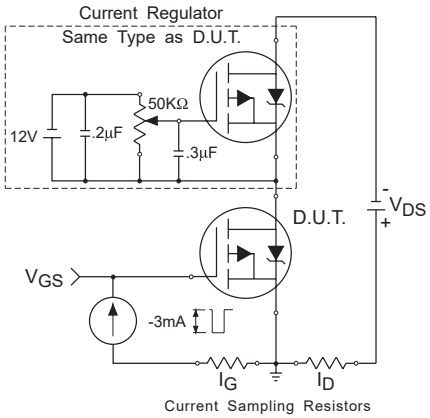
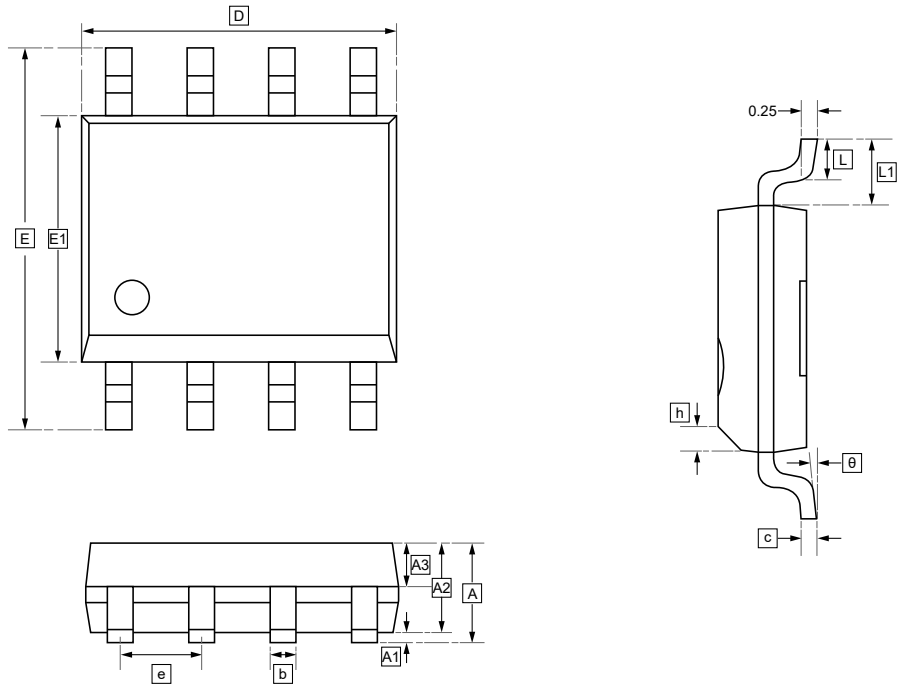


Fig 22b. Gate Charge Test Circuit

8.SOP-8 Package Outline Dimensions

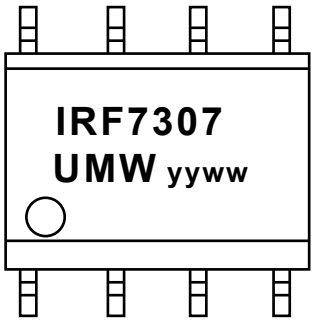


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.70	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.10	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRF7307TR	SOP-8	3000	Tape and reel

10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

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