UMW SN74LVC1G08

1.Description

The UMW SN74LVC1G08 is a 2-input AND gate integrated circuit, which can realize the mathematical logic operation of Y=A·B and Y=$\overline{A+B}$. Advanced CMOS process design is adopted, which has the working characteristics of low power consumption and high output driving capability. The chip can work normally when the power supply voltage V_{CC} is between 1.65V and 5.5V. And UMW SN74LVC1G08 has a variety of small package shapes, It can be widely used in high-end precision instruments, miniaturized low-power handheld devices, artificial intelligence and other fields.

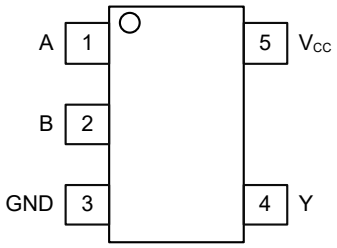
2.Product Usage

- Portable audio interface
- digital television
- Wireless headphones, smart watches, etc.
- Blu-ray player and home theater
- Solid state drive
- Smart wearable devices

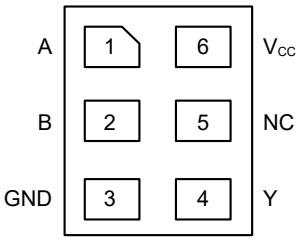
3.Features

- Low input current: 0.1μA typical
- Low static power consumption: 10μA typical
- High output drive: V_{CC}=4.5V, more than 32MA
- Wide working voltage range: 1.65V to 5.5V

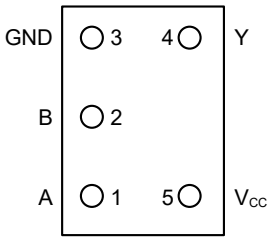
4.Pinning information



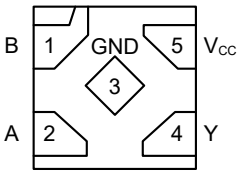
SOT23-5/SC70-5
SOT-553



DFN/SON-6



DSBGA-5



X2SON-5

5.Pin Function

Pin				Description
Name	SOT23-5/SC70-5/SOT-553/DSBGA-5	DFN/SON-6	X2SON-5	
A	1	1	2	Input
B	2	2	1	Input
GND	3	3	3	Ground
Y	4	4	4	Output
V_{CC}	5	6	5	Power pin
NC		5		Not connected

Notes: NC null pin, no connecting wire inside.

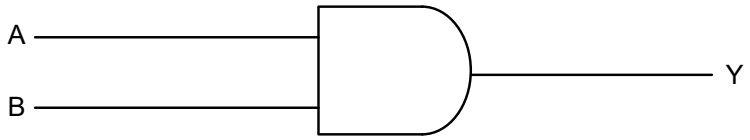
6.Limit parameter

Parameter	Symbol	Limit Value	Unit
Operating voltage	V_{CC}	6.5	V
Input	V_{IN}	-0.5 ~ 6.5	V
Output voltage(1)	V_{OUT}	-0.5 ~ 6.5	V
Continuous output current	I_O	±50	mA
Continuous current through V_{CC} or GND		±100	mA
Storage temperature	T_S	-65 to 150	°C
Pin welding temperature	T_W	260, 10s	°C
Working temperature	T_A	-40 to 105	°C

Note: 1. Under the condition of V_{CC}=0V power-off, the output can withstand the limit voltage,

2. Limit parameter refers to the limit value that cannot be exceeded under any condition. In case of exceeding this limit value, physical properties such as product degradation may be caused Damage; At the same time, the chip can not be guaranteed to work normally under the near limit parameters.

7.Principle Logic Diagram



Function Table

Input	Input	Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

8.Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage	V_{CC}		1.65		5.5	V
Input High Level Voltage	V_{IH}	V_C=1.65V~1.95V	0.65*V_{CC}			V
		V_C=2.3V~2.7V	1.7			V
		V_C=3V~5.5V	0.7*V_{CC}			V
Low-level Input Voltage	V_{IL}	V_C=1.65V~1.95V			0.35*V_{CC}	V
		V_C=2.3V~2.7V			0.7	V
		V_C=3V~5.5V			0.3*V_{CC}	V
Input Voltage	V_I		0		5.5	V
Output Voltage	V_O		0		V_{CC}	V
High Level Output Current	I_{OH}	V_C=1.65V			-4	mA
		V_C=2.3V			-8	mA
		V_C=3V			-16	mA
		V_C=4.5V			-32	mA
Low Level Output Current	I_{OL}	V_C=1.65V			4	mA
		V_C=2.3V			8	mA
		V_C=3V			16	mA
		V_C=4.5V			32	mA
High Level Load Voltage	V_{OH}	I_{OH}=-100μA, V_{CC}=1.65V~5.5V	V_{CC}-0.1			V
		I_{OH}=-4mA, V_{CC}=1.65V	1.2			V
		I_{OH}=-8mA, V_{CC}=2.3V	1.9			V
		I_{OH}=-16mA, V_{CC}=3V	2.4			V
		I_{OH}=-24mA, V_{CC}=3V	2.3			V
		I_{OH}=-32mA, V_{CC}=4.5V	3.8			V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Low Level Load Voltage	V_{OL}	I_{OL}=100μA,V_{CC}=1.65V~5.5V			0.1	V
		I_{OL}=4mA, V_{CC}=1.65V			0.45	V
		I_{OL}=8mA, V_{CC}=2.3V			0.3	V
		I_{OL}=16mA, V_{CC}=3V			0.4	V
		I_{OL}=24mA, V_{CC}=3V			0.55	V
		I_{OL}=32mA, V_{CC}=4.5V			0.55	V
Incoming Current (A or B inputs)	I_I	V_I=5.5V or GND, V_{CC}=0 to 5.5V			±5	μA
Turn-off Current	I_{off}	V_I or V_O=5.5V, V_{CC}=0V			±10	μA
Operational Current	I_{CC}	V_{CC}=5.5V or GND, I_O=0			10	μA
Working Current Variation Value	ΔI_{CC}	One Input at V_{CC}-0.6V Other Inputs at V_{CC} or GND			500	μA

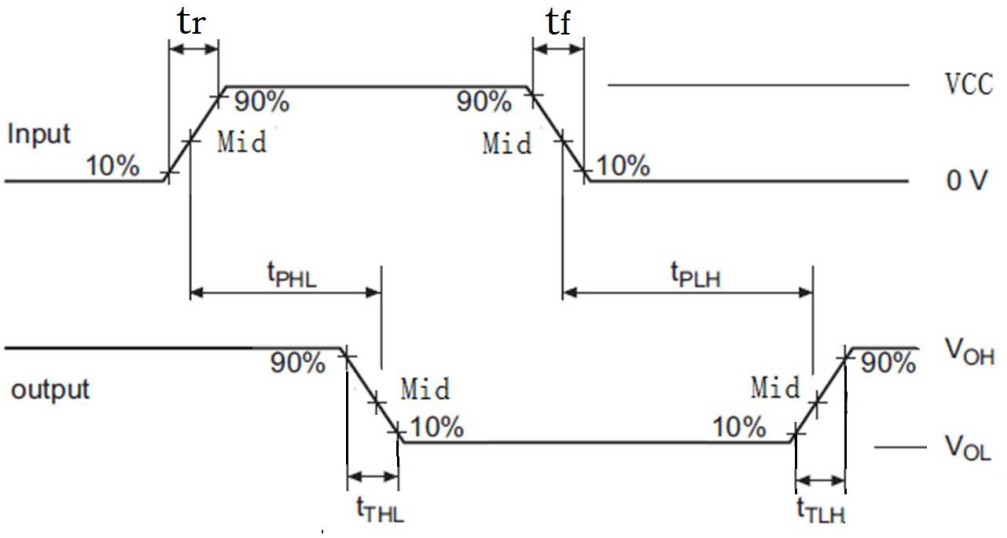
Ta=25°C V(298)=5.0V,tr =≤20ns. See test method.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Maximum transmission	t_{PHL}	C_L=15pF		10		ns
delay time a, B to Y	t_{PLH}			10		ns

9.Principle Logic Diagram

Parameter	Symbol	Conditions	Typ.	Unit
Input Capacitance	C_{IN}	V_{CC}=5.5V, V_I=0V or V_{CC}	>2.5	pF
Power Dissipation Capacitance (5)	C_{PD}	10MHz, V_{CC}=3.3V, V_I=0V or V_{CC}	26	pF
		10MHz, V_{CC}=5.5V, V_I=0V or V_{CC}	30	pF

Note5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)}=C_{PD} \times V_{CC} \times fin + I_{CC} \times C_{PD}$ is used to determine the no-load dynamic power consumption; $P_D=C_{PD} \times V_{CC}^2 \times fin+I_{CC} \times V_{CC} \times$ Fig.

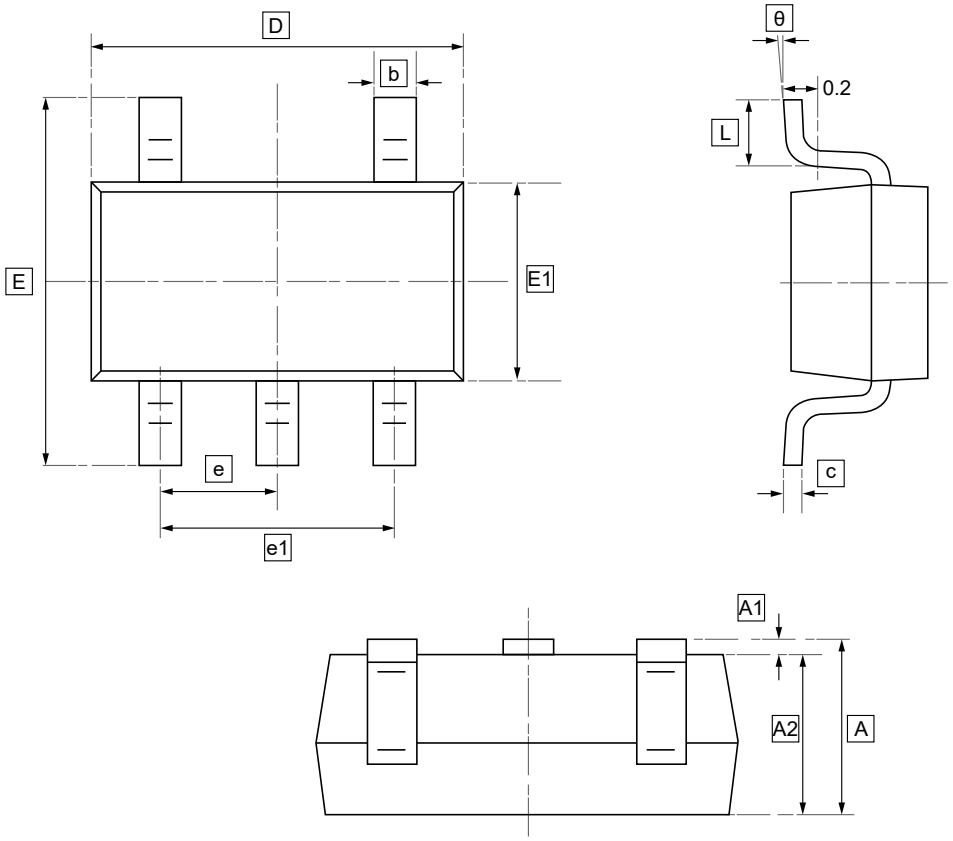


Note: 1. CL capacitor is external chip capacitor (0603), which is connected close to the output pin, and the capacitor ground is close to the chip GND;

2. Input: port input level, f=500kHz,D=50%; tr=tf≤20ns;

3. Output: Y-terminal output test.

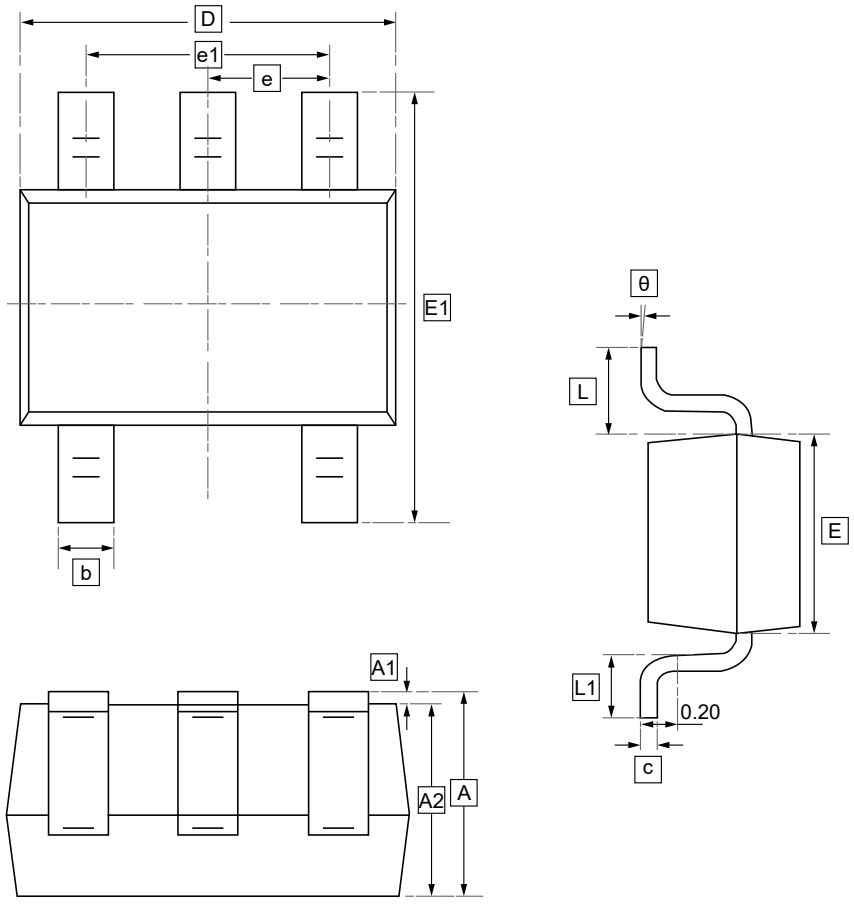
10.1 SOT23-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E1	E	e	e1	L	θ
Min	1.050	0.000	1.050	0.300	0.100	2.820	1.500	2.650	0.950	1.800	0.300	0°
Max	1.250	0.100	1.150	0.500	0.200	3.020	1.700	2.950	BSC	2.000	0.600	8°

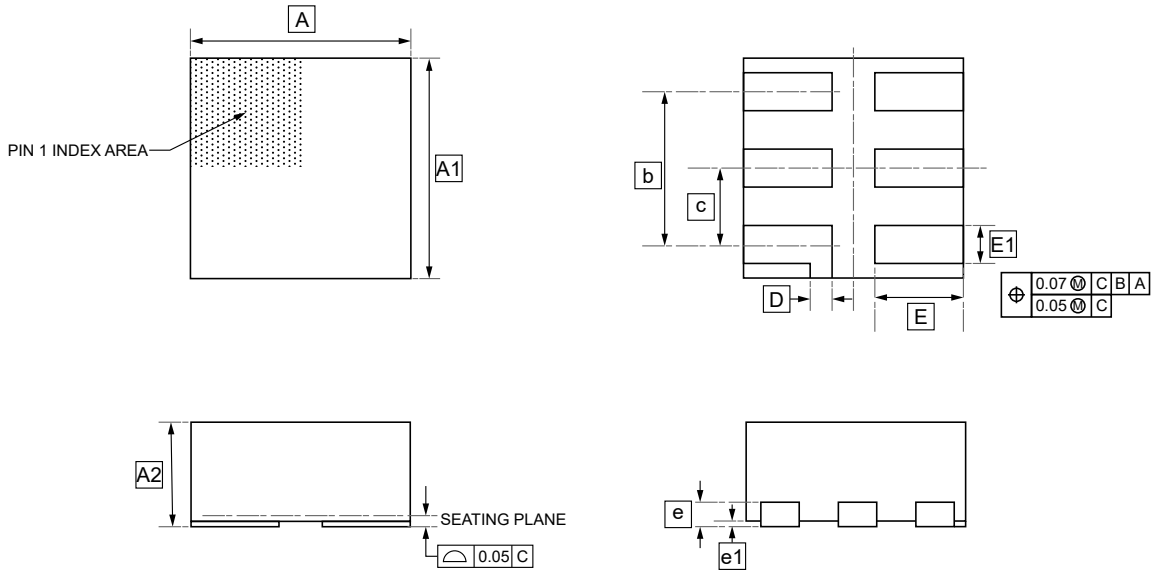
10.2 SC70-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1	L	θ
Min	0.90	0.00	0.90	0.15	0.08	1.80	1.15	2.15	0.65	1.20	0.26	7°
Max	1.10	0.10	1.00	0.35	0.15	2.25	1.35	2.45	TYP	1.40	0.46	REF.

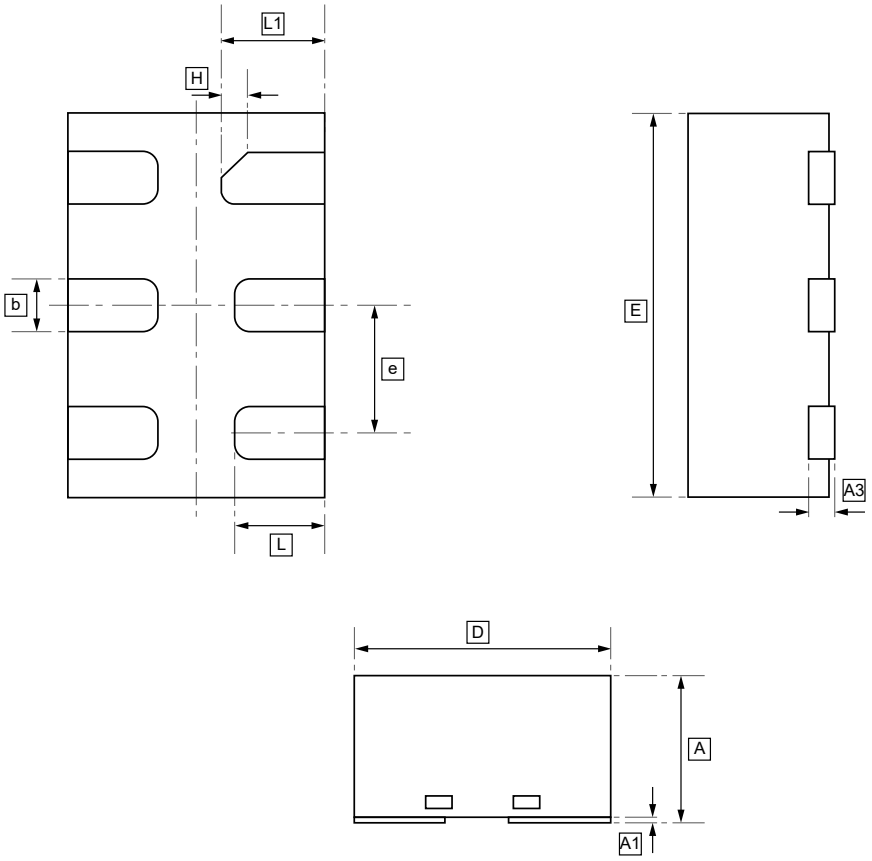
10.3 DFN-6(1*1) Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1
Min	0.95	0.95	-	0.7	0.35	0.1	0.35	0.12	0.11	0.00
Max	1.05	1.05	0.4				0.45	0.22	TYP	0.05

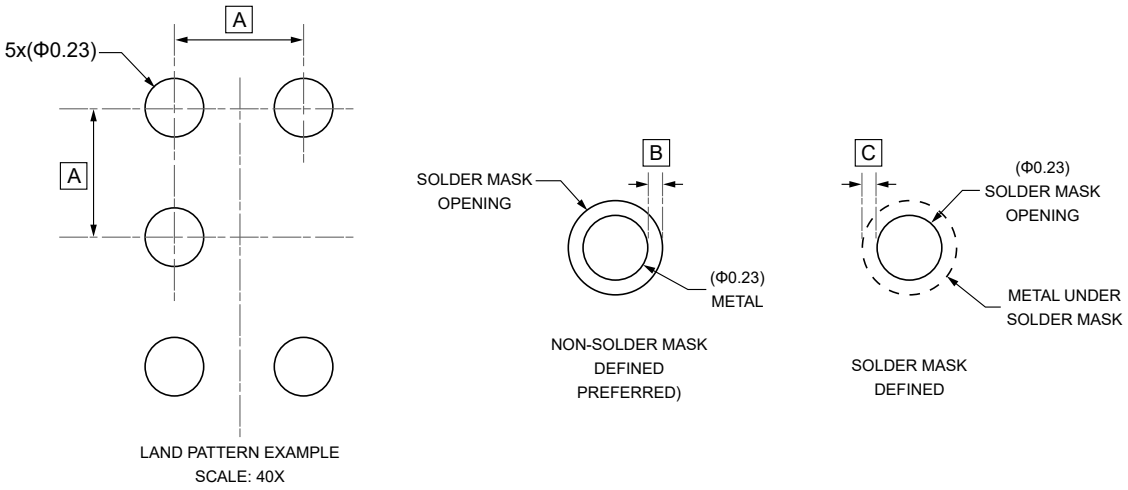
10.4 DFN6(1x1.5) Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A3	b	D	E	e	H	L	L1
Min	0.50	0	0.10	0.15	0.90	1.40	0.40	0.10	0.30	0.35
Max	0.60	0.05	REF	0.25	1.10	1.60	0.60	REF	0.40	0.45

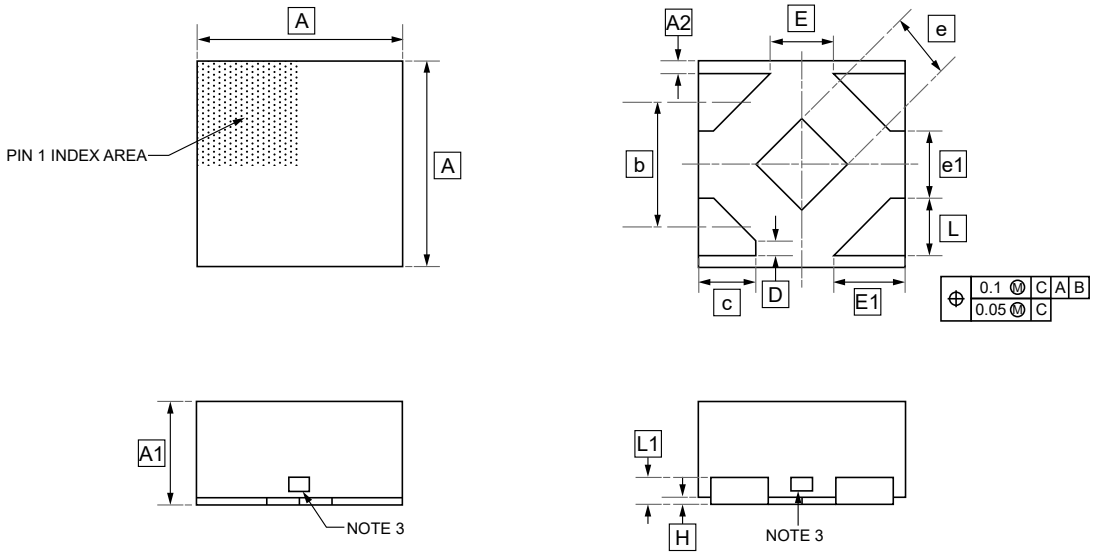
10.5 DSBGA-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	B	C
Min	0.5	-	0.05
Max	TYP	0.05	-

10.6 X2SON-5 Package Outline Dimensions

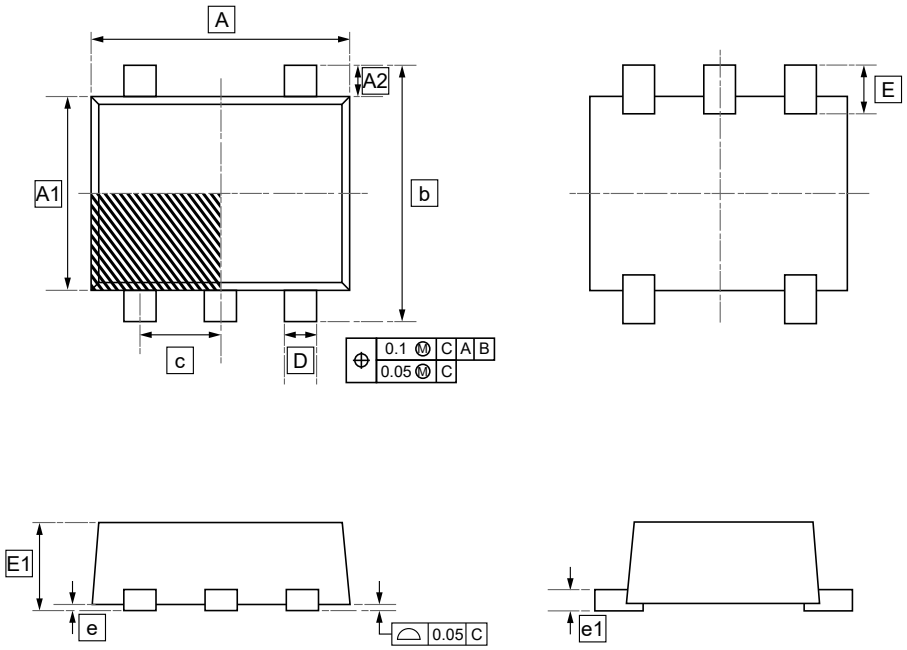


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1	L	L1
Min	0.75	-	0.05	0.48	0.17	0.06	0.25	0.23	0.15	0.26	0.17	0.1
Max	0.85	0.4			0.27			0.32	0.35		0.27	

Symbol	H
Min	0.00
Max	0.05

10.7 SOT-553 Package Outline Dimensions

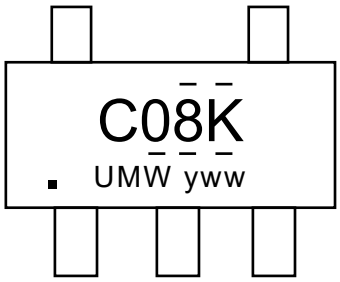


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1
Min	1.50	1.10	0.13	1.50	0.50	0.15	0.20	0.50	0.00	0.08
Max	1.70	1.30	0.27	1.70		0.25	0.40	0.60	0.05	0.18

11.Ordering Information

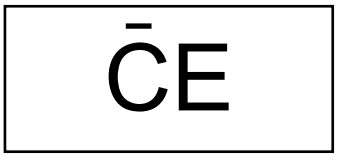
SOT23-5



DFN(1*1.5)



DFN(1*1)



yww: Batch Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW SN74LVC1G08DBVR	C08K	SOT23-5	3000	Tape and reel
UMW SN74LVC1G08DCKR	CE5	SC70-5	3000	Tape and reel
UMW SN74LVC1G08YZPR	CE	DSBGA-5	3000	Tape and reel
UMW SN74LVC1G08DPWR	M7	X2SON-5	3000	Tape and reel
UMW SN74LVC1G08DRLR	CE7	SOT-553	4000	Tape and reel
UMW SN74LVC1G08DSFR	CE	DFN(1*1)	5000	Tape and reel
UMW SN74LVC1G08DRYR	CE	DFN(1*1.5)	5000	Tape and reel

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