UMW NTMD3P03R2G

Dual -30V P-Channel MOSFET

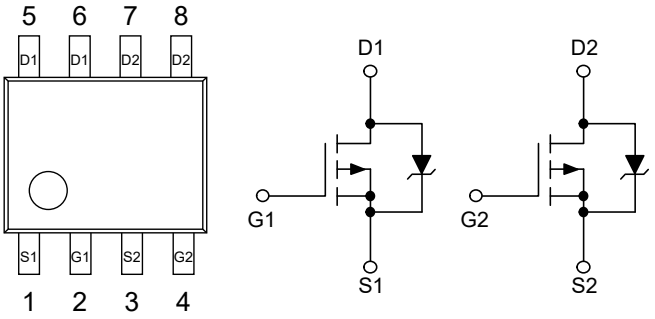
1.Features

- $V_{DS\ (V)}$=-30V
- $R_{DS(ON)}$<85mΩ(V_{GS}=-10V)
- $R_{DS(ON)}$<125mΩ(V_{GS}=-4.5V)
- High Density Power MOSFET with Low $R_{DS(ON)}$
- High Efficiency Components in a Dual SOP−8 Package
- Miniature SOP-8 Surface Mount Package Saves Board Space
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Diode Exhibits High Speed with Soft Recovery

3.Pinning information

Pin	Symbol	Description
2,4	G1,G2	GATE
1,3	S1,S2	SOURCE
5,6,7,8	D1,D2	DRAIN

SOP-8



3.Absolute Maximum Ratings T_J=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DSS}	-30	V
Gate-Source Voltage		V_{GSS}	±20	V
Junction−to−Ambient (Note 1)	Thermal Resistance	$R_{\theta JA}$	171	°C/W
Total Power Dissipation @ T_A=25°C		P_D	0.73	W
Continuous Drain Current @ 25°C		I_D	-2.34	A
Continuous Drain Current @ 70°C		I_D	-1.87	A
Pulsed Drain Current (Note 4)		I_{DM}	-8	A
Junction−to−Ambient (Note 2)	Thermal Resistance	$R_{\theta JA}$	100	°C/W
Total Power Dissipation @ T_A=25°C		P_D	1.25	W
Continuous Drain Current @ 25°C		I_D	-3.05	A
Continuous Drain Current @ 70°C		I_D	-2.44	A
Pulsed Drain Current (Note 4)		I_{DM}	-12	A

Junction−to−Ambient (Note 3)	Thermal Resistance	$R_{\theta JA}$	62.5	°C/W
Total Power Dissipation @ T_A=25°C		P_D	2	W
Continuous Drain Current @ 25°C		I_D	-3.86	A
Continuous Drain Current @ 70°C		I_D	-3.1	A
Pulsed Drain Current (Note 4)		I_{DM}	-15	A
Operating and StorageTemperature Range		T_J, T_{stg}	-55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J=25°C (V_{DD}=-30V_{dc}, V_{GS}=−4.5Vdc, Peak I_L=−7.5 Apk, L=5 mH, R_G=25Ω)		E_{AS}	140	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8” from case for 10 seconds		T_L	260	°C

4.Electrical Characteristics T_J=25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	-30			V
Temperature Coefficient (Positive)				-30		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V,V_{GS}=0V,T_J=25°C			-1	μA
		V_{DS}=-24V,V_{GS}=0V,T_J=125°C			-20	
		V_{DS}=-30V,V_{GS}=0V,T_J=25°C			-2	
Gate−Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1	-1.7	-2.5	V
Static Drain−to−Source	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-3.05A		63	85	mΩ
On−State Resistance		V_{GS}=-4.5V, I_D=-1.5A		90	125	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-15V, I_D=-3.05A		5		S
Input Capacitance	C_{iss}	V_{DS}=-24V, V_{GS}=0V f = 1.0 MHz		520	750	pF
Output Capacitance	C_{oss}			170	325	pF
Reverse Transfer Capacitance	C_{rss}			70	135	pF
Turn-On DelayTime	$t_{D(on)}$	V_{DD}=-24V, I_D=-3.05A V_{GS}=-10V, R_G=6Ω		12	22	ns
Rise Time	t_r			16	30	ns
Turn-Off DelayTime	$t_{D(off)}$			45	80	ns
Fall Time	t_f			45	80	ns
Turn-On DelayTime	$t_{D(on)}$	V_{DD}=-24V, I_D=-1.5A V_{GS}=-4.5V, R_G=6Ω		16		ns
Rise Time	t_r			42		ns
Turn-Off DelayTime	$t_{D(off)}$			32		ns
Fall Time	t_f			35		ns
Total Gate Charge	Q_{tot}	V_{DS}=-24V V_{GS}=-10V I_D=-3.05A		16	25	nC
Gate−Source Charge	Q_{gs}			2		nC
Gate−Drain Charge	Q_{gd}			4.5		nC

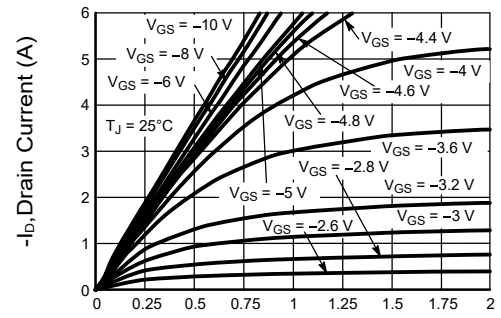
Diode Forward On−Voltage	V_{SD}	I_S=-3.05A, V_{GS}=0V		-0.96	-1.25	V
		I_S=-3.05A, V_{GS}=0V, T_J=125°C		-0.78		V
Reverse Recovery Time	t_{rr}	I_S=-3.05A, V_{GS}=0V dis/dt=100A/μs		34		ns
	t_a			18		ns
	t_b			16		ns
Reverse Recovery Stored Charge	Q_{rr}			0.03		μC

5. Handling precautions to protect against electrostatic discharge is mandatory.

6. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.

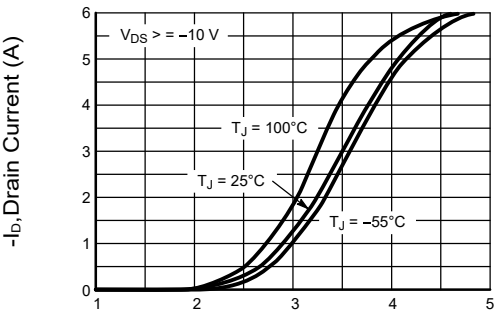
7. Switching characteristics are independent of operating junction temperature.

5.1Typical Characterisitics



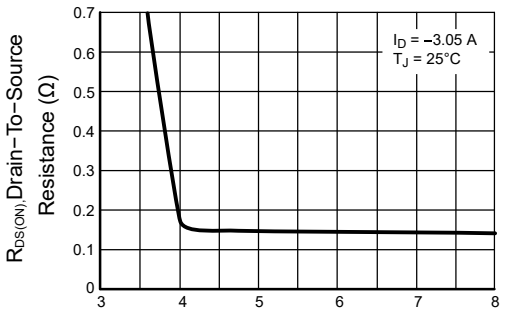
-V_{DS},Drain-to-Source Voltage (V)

Figure 1: On−Region Characteristics



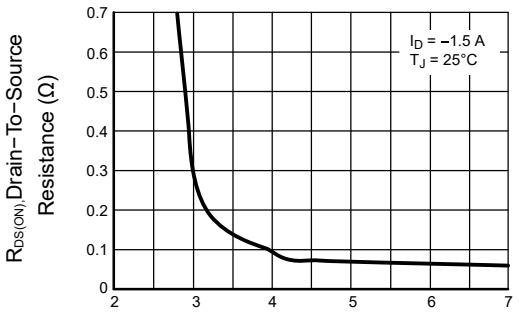
-V_{GS},Gate-to-Source Voltage (V)

Figure 2: Transfer Characteristics



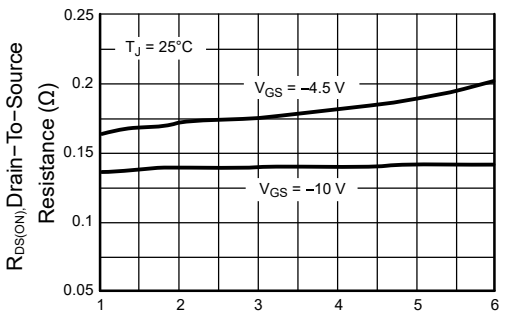
-V_{GS}, Gate−To−Source Voltage (V)

Figure 3: On-Resistance vs. Gate−to−Source Voltage



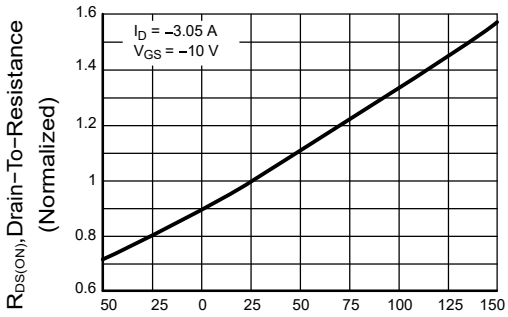
-V_{GS}, Gate−To−Source Voltage (V)

Figure 4: On−Resistance vs. Drain Current and Gate Voltage



$-I_D$, Drain Current (A)

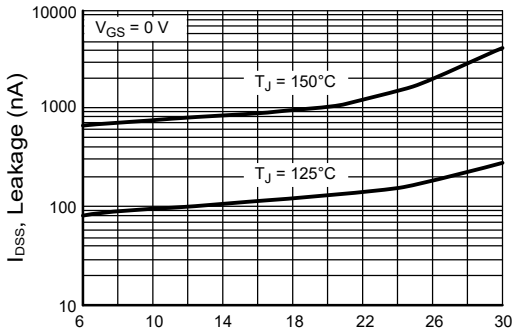
Figure 5: On-Resistance vs. Drain Current and Gate Voltage



T_J, Junction Temperature (°C)

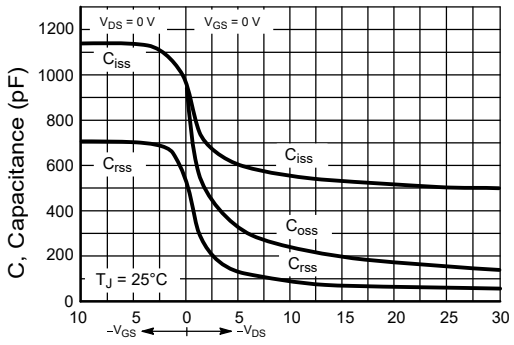
Figure 6: On Resistance Variation with Temperature

5.2Typical Characterisitics



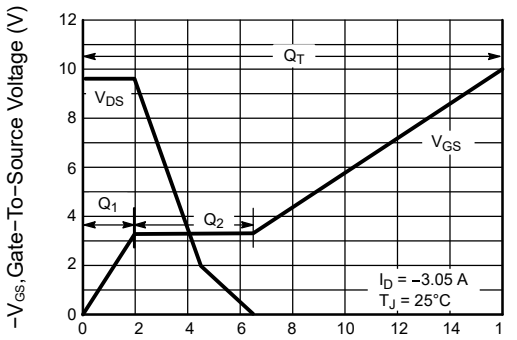
$-V_{DS}$, Drain−To−Source Voltage (V)

Figure 7: Drain-to-Source Leakage Current vs. Voltage



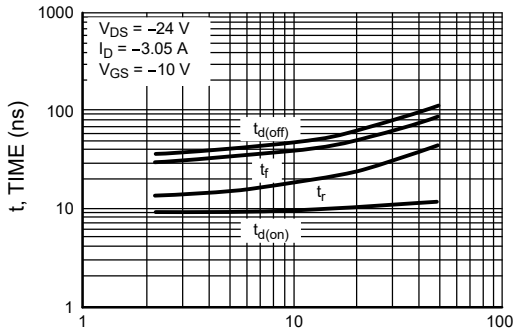
Gate−To−Source Or Drain−To−Sourcevoltage (V)

Figure 8: Capacitance Variation



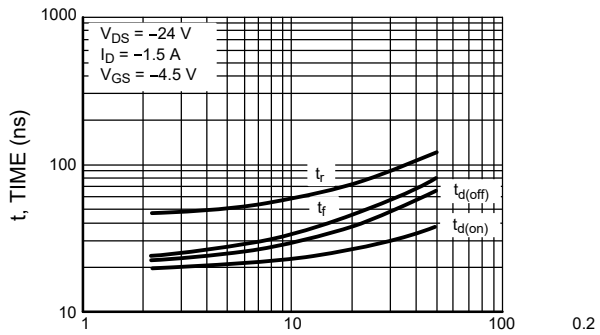
Q_g, Total Gate Charge (nC)

Figure 9: Gate-to-Source and Drain-to-Source Voltage vs. Total Charge



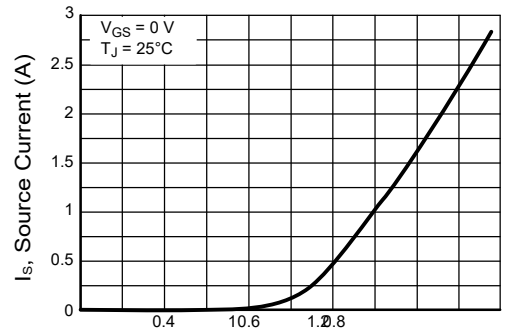
R_G, Gate Resistance (Ω)

Figure 10: Resistive Switching Time Variation vs. Gate Resistance



R_G, Gate Resistance (Ω)

Figure 11: Resistive Switching Time Variation vs. Gate Resistance



$-V_{SD}$, Drain−To−Source Voltage (V)

Figure 12: Diode Forward Voltage vs. Current

5.3Typical Characterisitics

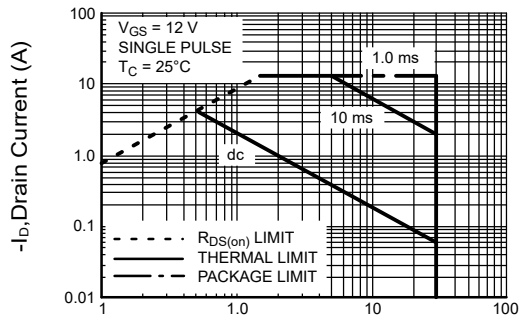


Figure 13: Maximum Rated Forward Biased Safe Operating Area

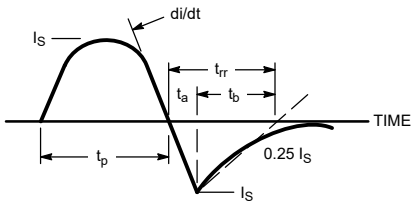


Figure 14: Diode Reverse Recovery Waveform

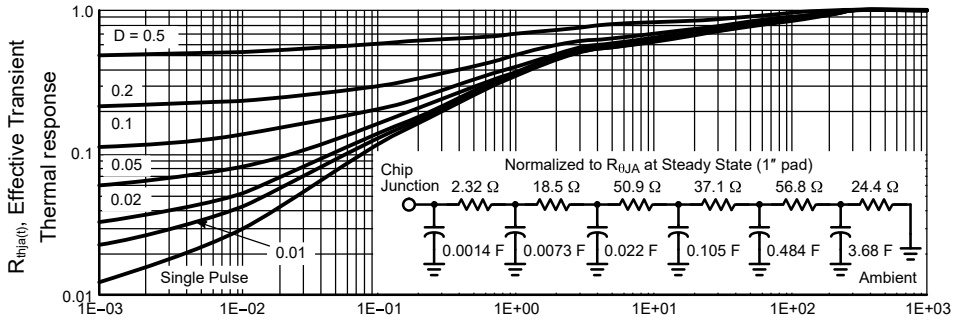
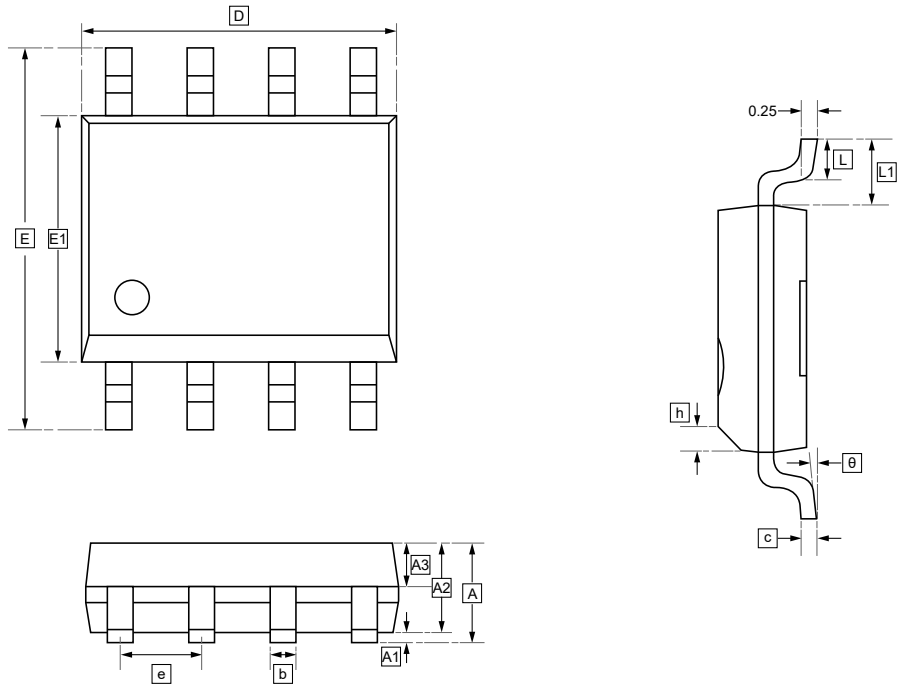


Figure 15: FET Thermal Response

6.SOP-8 Package Outline Dimensions

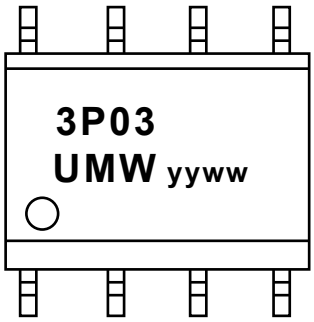


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.70	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.10	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

7.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW NTMD3P03R2G	SOP-8	3000	Tape and reel

8.Disclaimer

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