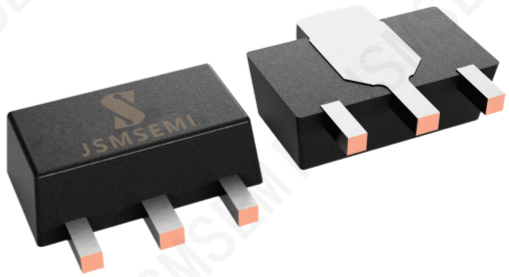
General Description

The TLV709AxxPKR-JSM are a group of low-dropout (LDO) voltage regulators offering the benefits of wide input voltage range, lowdropout voltage, low power consumption, and miniaturized packaging. Quiescent current of only 1.5μA makes these devices ideal for powering the battery-powered, always-on systems that require very little idle-state power dissipation to a longer service life. The TLV709AxxPKR-JSM of linear regulators are stable with the ceramic output capacitor over its wide input range from 2V to 23Vand the entire range of output load current (0mA to 500mA).



SOT-89-3L

Features

- 1.5μA Ground Current at no Load
- ±1% Output Accuracy
- 500mA Output Peak Current
- Wide Operating Input Voltage Range: 2V to 23V
- Dropout Voltage: 0.35V at 100mA / V_{OUT} 5V
- Support Fixed Output Voltage 1.8V, 2.5V, 2.8V, 3.0V, 3.3V, 3.6V, 5V
- Stable with Ceramic or Tantalum Capacitor
- Current Limit Protection
- Over-Temperature Protection
- SOT-89-3L Packages Available

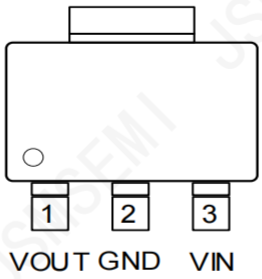
Applications

- Portable, Battery Powered Equipment
- Low Power Microcontrollers
- Laptop, Palmtops and PDAs
- Wireless Communication Equipment
- Audio/Video Equipment
- Car Navigation Systems
- Industrial Controls
- Weighting Scales
- Meters
- Home Automation

Ordering Information

Order number	Package	Marking	Operation Temperature Range	MSL Grade	Ship, Quantity	Green
TLV709A33PKR-JSM	SOT-89-3L	AAFL	-40to 150°C	3	TUBE,1000	Rohs
TLV709A50PKR-JSM	SOT-89-3L	AAFP	-40 to 150°C	3	TUBE,1000	Rohs

Pin Configurations



Description of Functional Pins

Pin No SOT-89-3L	Pin Name	Pin Function
2	GND	Ground
1	VOUT	Output of the Regulator
3	VIN	Input of Supply Voltage.

Typical Application Circuits

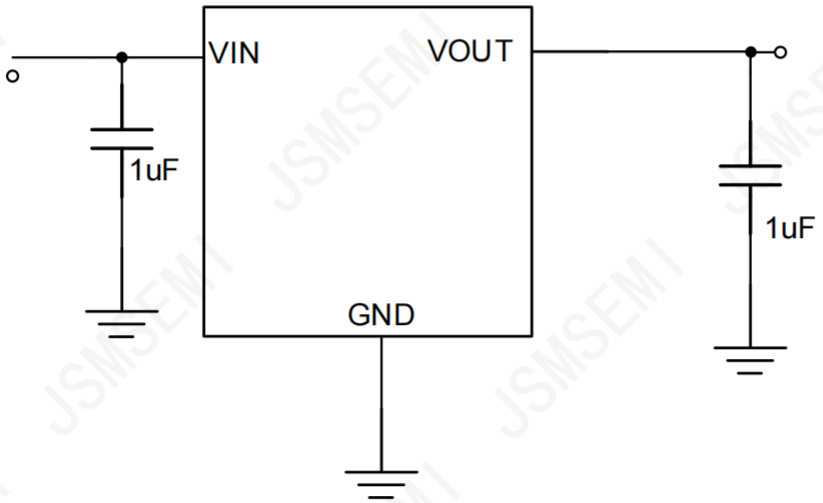


Figure 1: Application circuit of Fixed VOUT LDO

Absolute Maximum Ratings (Note 1)

VIN to GND ---------- -0.3V to 28V

VOUT to GND ---------- -0.3V to 6.0V

VOUT to VIN ---------- -27V to 0.3V

Package Thermal Resistance (Note 2)

SOT-89-3L, θ_{JA} ---------- 130 °C /W

Lead Temperature (Soldering, 10 sec.) ---------- 260 °C

Junction Temperature ---------- 150 °C

Storage Temperature Range ---------- -40 °C to 150 °C

ESD Susceptibility

HBM ---------- 2KV

MM ---------- 200V

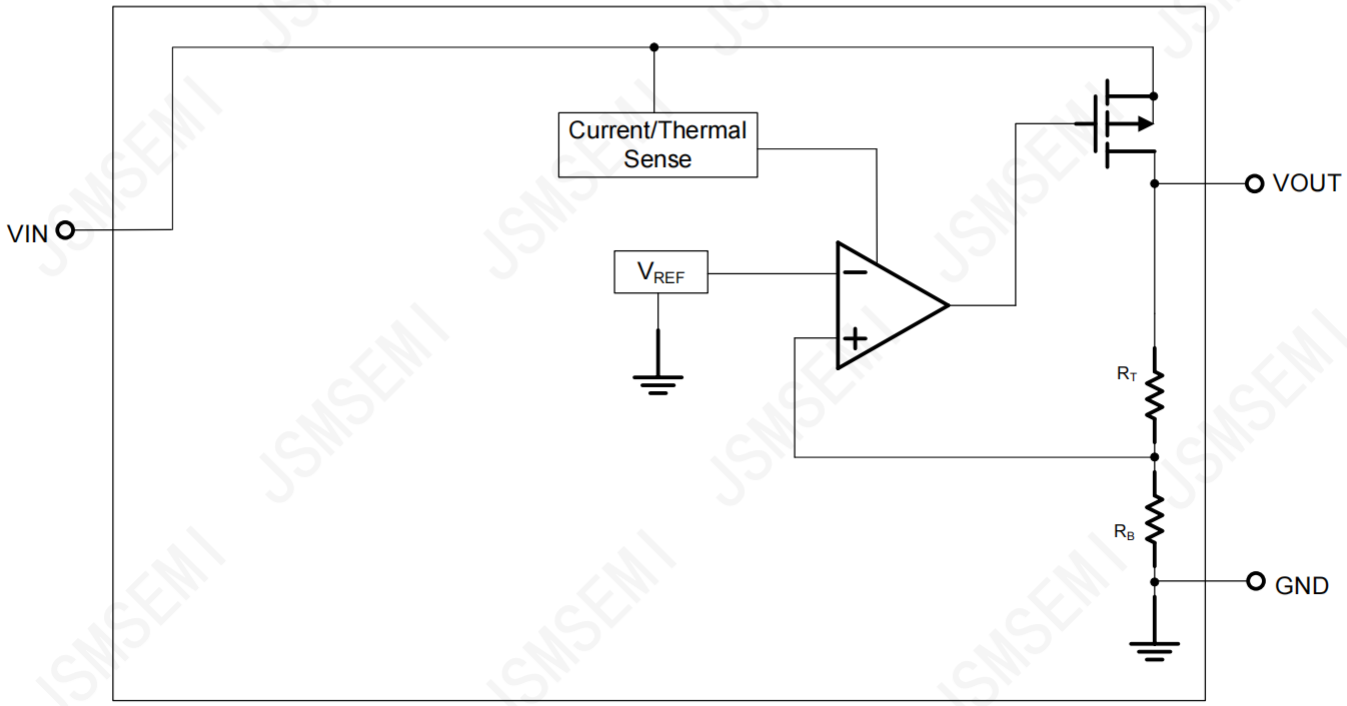
Recommended Operating Conditions

Input Voltage VIN ---------- 2.0V to 23V

Junction Temperature Range ---------- -40 °C to 125 °C

Ambient Temperature Range ---------- -40 °C to 85 °C

Function Block Diagram



Electrical Characteristics

(V_{IN} =12V, V_{EN} =5V, T_A=25°C unless otherwise specified)

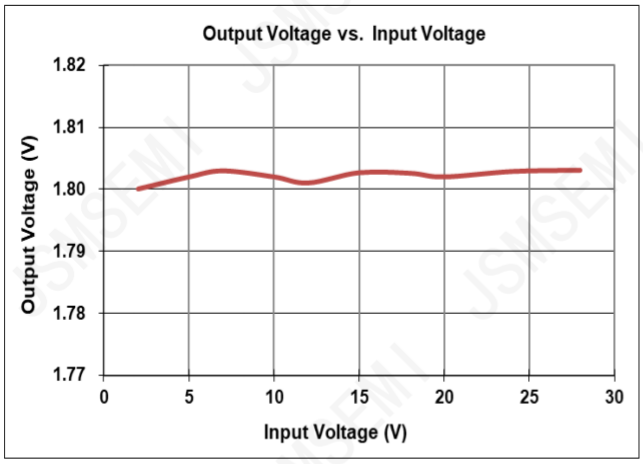
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{IN}		2	--	23	V
DC Output Voltage Accuracy		I_{LOAD} = 0.1mA	-1		1	%
Dropout Voltage (I_{LOAD} =100mA)	V_{DROP}	V_{OUT} ≥ 5V	--	0.35		V
	$V_{DROP_3.3V}$	V_{OUT} = 3.3V		0.42		
	$V_{DROP_1.8V}$	V_{OUT} = 1.8V		0.5		
Ground Current (I_{LOAD} = 0mA) (Note 3)	I_Q	V_{IN} > V_{OUT}		1.5		μA
Line Regulation	ΔLINE	I_{LOAD} =1mA, 10V ≤ V_{IN} ≤ 20V	--	0.5		%
Load Regulation	ΔLOAD	10mA≤ I_{LOAD} ≤ 0.2A		0.3		%
Output Peak Loading Current	I_{OUT}	V_{IN} = V_{OUT} + 1.8V		500		mA
Output Current Limit	I_{LIM}	V_{OUT} = 0V	501	700		mA
Power Supply Rejection Ratio	PSRR	V_{OUT} = 5V, I_{LOAD} = 30mA, V_{IN} = 12V, f = 1KHz		70		dB
Thermal Shutdown Temperature	T_{SD}	I_{LOAD} = 10mA	--	160	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}			15		°C

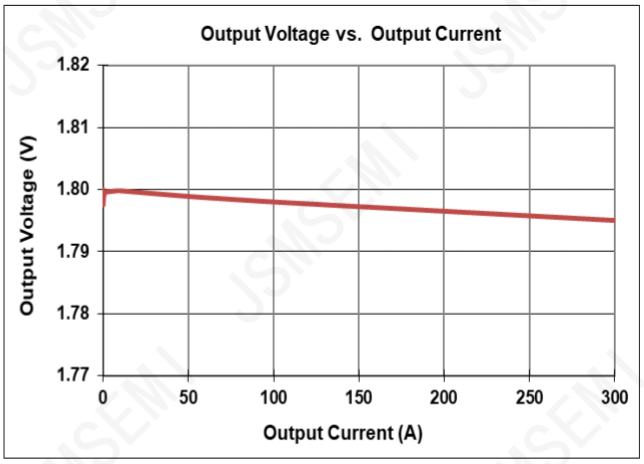
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

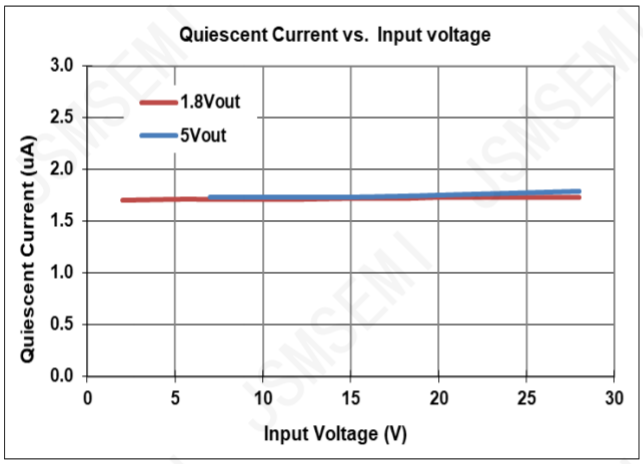
Note 2. θ_{JA} is measured at T_A = 25°C on a JSMSEMI EVB board.

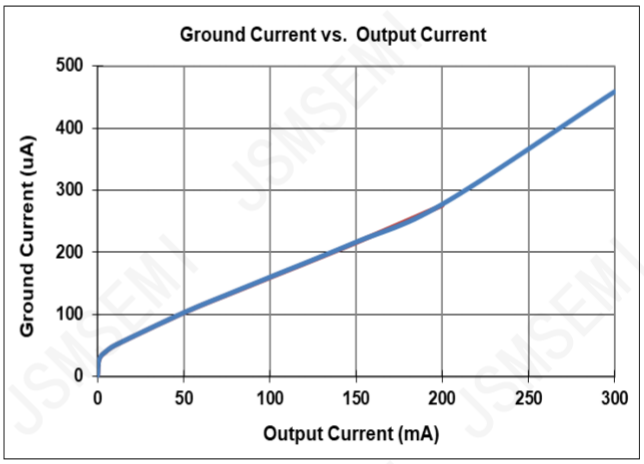
Note 3. When V_{IN} > V_{OUT}, the quiescent current is the normal specification value, but when V_{IN} ≤ V_{OUT}, the quiescent current will be greater than the specification value.

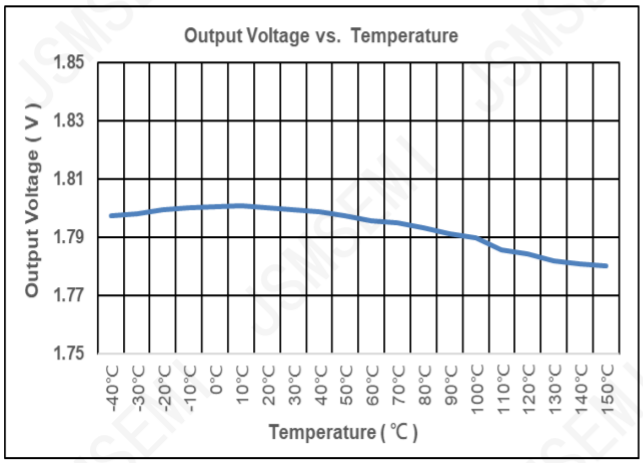
Typical Characteristics

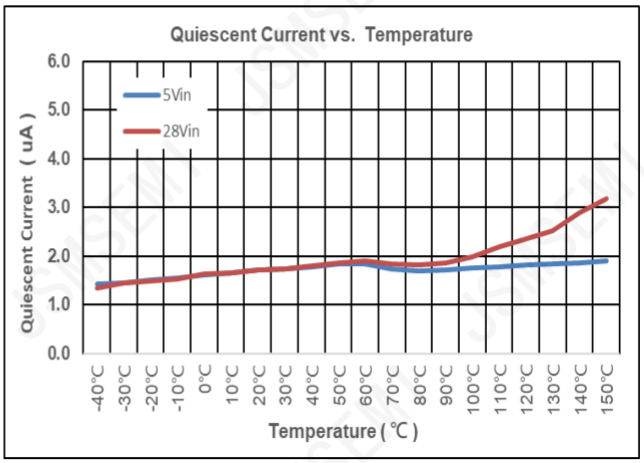




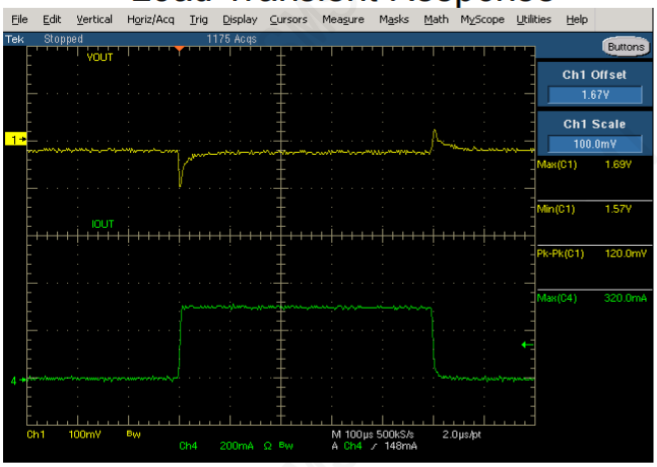




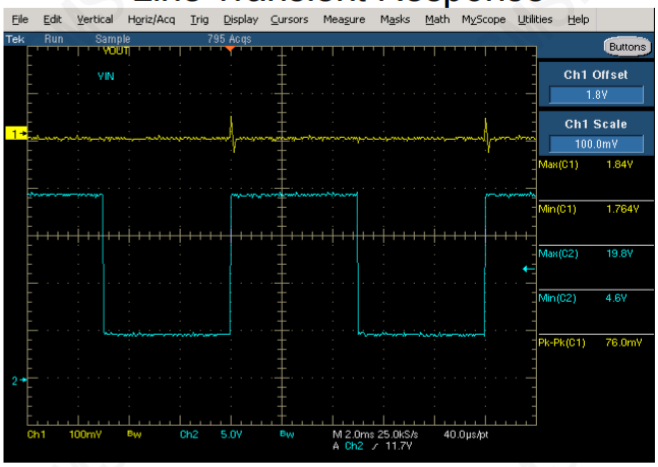




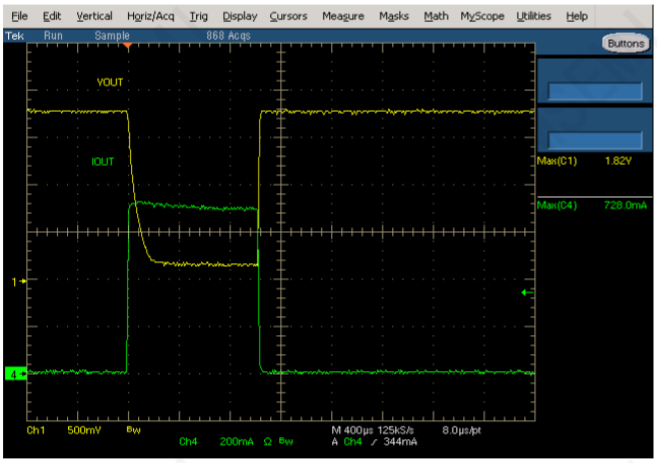
Load Transient Response

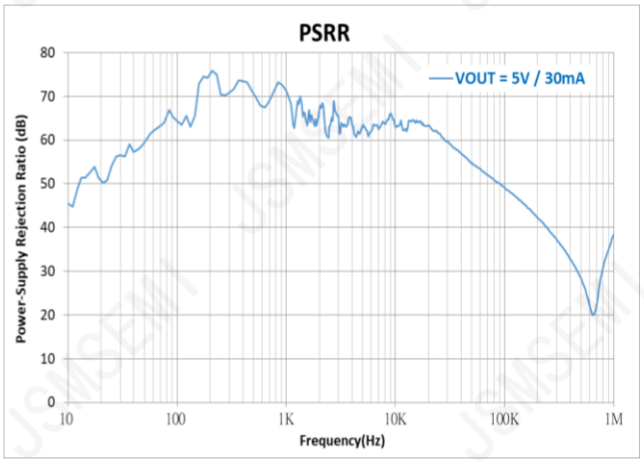


Line Transient Response



Current Limit





Application Guideline

Input and Output Capacitor Requirements

The external input and output capacitors of TLV709Axx PKR-JSM must be properly selected for stability and performance. Use a 1μF or larger input capacitor and place it close to the IC's VIN and GND pins. Any output capacitor meeting the minimum 1mΩ ESR (Equivalent Series Resistance) and effective capacitance between 1μF and 22μF requirement may be used. Place the output capacitor close to the IC's VOUT and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

Current Limit

The TLV709AxxPKR-JSM contain the current limiter of output power transistor, which monitors and controls the transistor, limiting the output current to 700mA (typical). The output can be shorted to ground indefinitely without damaging the part.

Dropout Voltage

The TLV709AxxPKR-JSM use a PMOS pass transistor to achieve low dropout. When (VIN –VOUT) is less than the dropout voltage (VDROP), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the RDS(ON)of the PMOS pass element. VDROPscales approximately with the output current because the PMOS device behaves as a resistor in dropout condition.

As any linear regulator, PSRR and transient response are degraded as (VIN –VOUT) approaches dropout condition.

OTP (Over Temperature Protection)

The over temperature protection function of TLV709AxxPKR-JSM will turn off the P-MOSFET when the junction temperature exceeds 160°C (typ.). Once the junction temperature cools down by approximately 15°C, the regulator will automatically resume operation.

Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below:

T_A=25°C, JSMSEMI PCB,

The max PD (Max)= (125°C − 25°C) / (130°C/W) = 0.77W for SOT-89-3L package

Power dissipation (PD) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

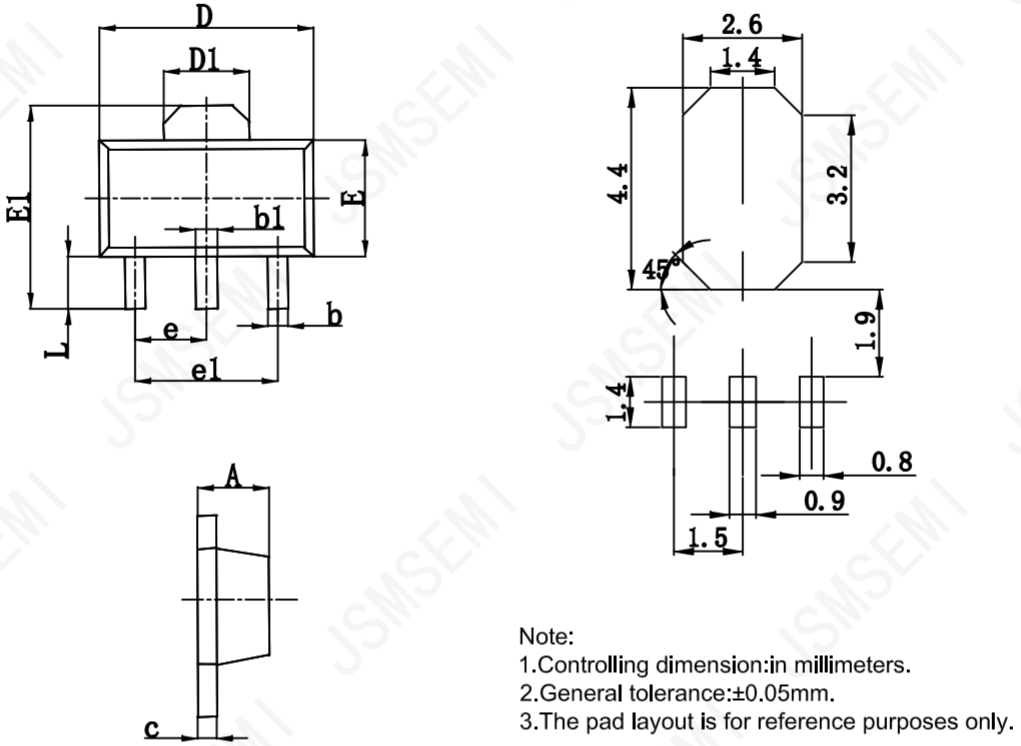
PD = (VIN – VOUT) × IOUT

Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the TLV709AxxPKR-JSM ground pin using as wide and as short of a copper trace as is practical. Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

Package Information

SOT-89-3L



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.197
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF		0.061 REF	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP		0.060 TYP	
e1	3.000 TYP		0.118 TYP	
L	0.900	1.200	0.035	0.047

Revision History

Rev.	Change	Date
V1.0	Initial version	6/27/2021

Important Notice

JSMSEMI Semiconductor (JSMSEMI) PRODUCTS ARE NEITHER DESIGNED NOR INTENDED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS UNLESS THE SPECIFIC JSMSEMI PRODUCTS ARE SPECIFICALLY DESIGNATED BY JSMSEMI FOR SUCH USE. BUYERS ACKNOWLEDGE AND AGREE THAT ANY SUCH USE OF JSMSEMI PRODUCTS WHICH JSMSEMI HAS NOT DESIGNATED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS IS SOLELY AT THE BUYER' S RISK.

JSMSEMI assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using JSMSEMI products.

Resale of JSMSEMI products or services with statements diferent from or beyond the parameters stated by JSMSEMI for that product or service voids all express and any implied warranties for the associated JSMSEMI product or s ervice. JSMSEMI is not responsible or liable for any such statements.

JSMSEMI All Rights Reserved. Information and data in this document are owned by JSMSEMI wholly and may not be edited, reproduced, or redistributed in any way without the express written consent from JSMSEMI.

Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc.When designing equipment, refer to the "Delivery Specification" for the JSMSEMI product that you intend to use.

For additional information please contact Kevin@jsmsemi.com or visit www.jsmsemi.com