UMW IRF7424TR

P-Channel 30 V (D-S) MOSFET

1.Description

The SOP-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infrared, or wave soldering techniques.

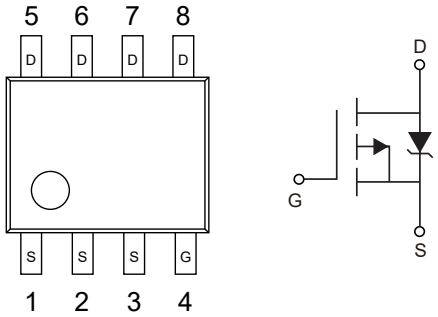
2.Features

- V_{DSS}=-30V
- $R_{DS(ON)}$<13.5mΩ(V_{GS}=-10), I_D=-11A
- $R_{DS(ON)}$<22mΩ(V_{GS}=-4.5V), I_D=-8.8A

3.Pinning information

Pin	Symbol	Description
1,2,3	S	SOURCE
4	G	GATE
5,6,7,8	D	DRAIN

SOP-8



4.Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Rating	Units
Drain- Source Voltage		V_{DS}	-30	V
Continuous Drain Current, V_{GS}=-10V	T_A=25°C	I_D	-11	A
Continuous Drain Current, V_{GS}=-10V	T_A=70°C		-9.3	A
Pulsed Drain Current ①		I_{DM}	-47	A
Power Dissipation ③	T_A=25°C	P_D	2.5	W
Power Dissipation ③	T_A=70°C		1.6	W
Linear Derating Factor			20	mW/°C
Gate-to-Source Voltage		V_{GS}	±20	V
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

5.Thermal Resistance Rating

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ③	$R_{\theta JA}$		50	°C/W

6.Electrical Characteristics T_J=25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=-250μA, V_{GS}=0V	-30			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/T_J$	I_D=-1mA,Reference to 25°C		-0.019		V/°C
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-11A ②			13.5	mΩ
		V_{GS}=-4.5V, I_D=-8.8A ②			22	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1		-2.5	V
Forward Transconductance	g_{FS}	V_{DS}=-10V, I_D=-11A	17			S
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=-24V, V_{GS}=0V			-15	μA
		V_{DS}=-24V,V_{GS}=0V,T_J=70°C			-25	
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS}=-20V			-100	nA
Gate-to-Source Reverse Leakage		V_{GS}=20V			100	
Total Gate Charge	Q_g	I_D=-11A		75	110	nC
Gate-to-Source Charge	Q_{gs}	V_{DS}=-15V		14	21	
Gate-to-Drain ("Miller") Charge	Q_{gd}	V_{GS}=-10V		12	18	
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=-15V ②		15		ns
Rise Time	t_r	I_D=-1A		23		ns
Turn-Off Delay Time	$t_{D(off)}$	R_G=6Ω		150		ns
Fall Time	t_f	V_{GS}=-10V		76		ns
Input Capacitance	C_{iss}	V_{GS}=0V		4030		pF
Output Capacitance	C_{oss}	V_{DS}=-25V		580		pF
Reverse Transfer Capacitance	C_{rss}	f=1.0kHz		410		pF

7.Source-Drain Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			-2.5	A
Pulsed Source Current (Body Diode) ①	I_{SM}				-47	
Diode Forward Voltage	V_{SD}	T_J=25°C,I_S=-2.5A,V_{GS}=0V ②			-1.2	V
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=-2.5A dI/dt=-100A/μs ②		40	60	ns
Reverse Recovery Charge	Q_{rr}			47	71	nC

Notes:

① Repetitive rating; pulse width limited bymax.junction temperature.

② Pulse width ≤ 400μs; duty cycle ≤ 2%.

③ Surface mounted on 1 in square Cu board.

8.1Typical Characterisitics

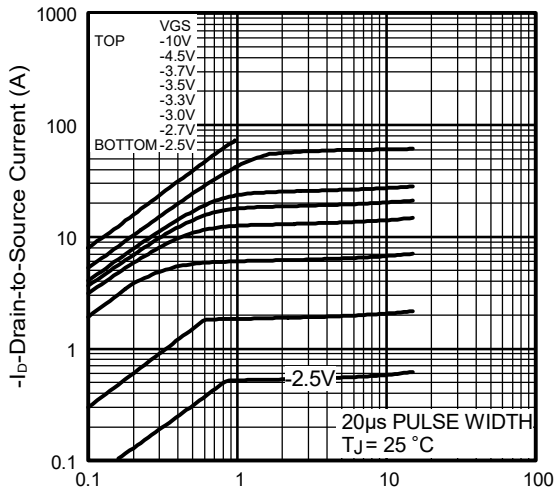


Fig 1. Typical Output Characteristics

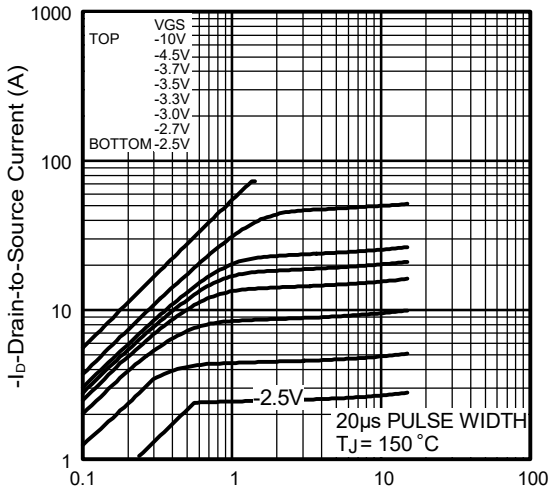


Fig 2. Typical Output Characteristics

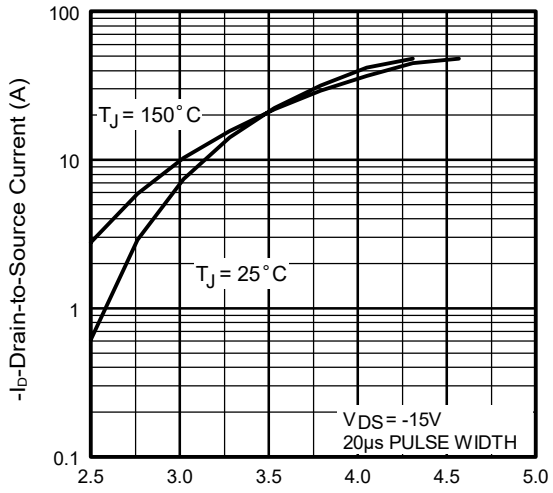


Fig 3. Typical Transfer Characteristics

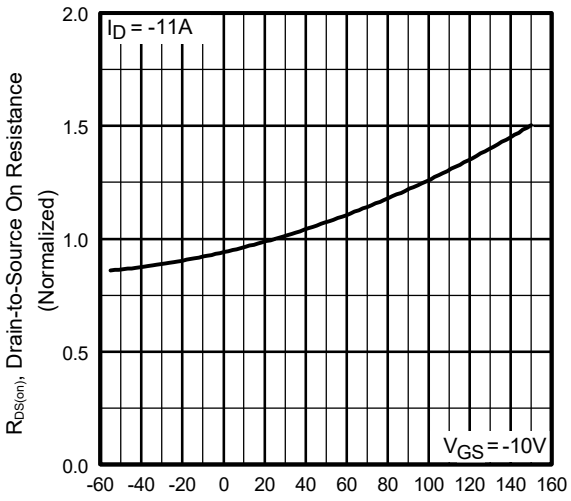
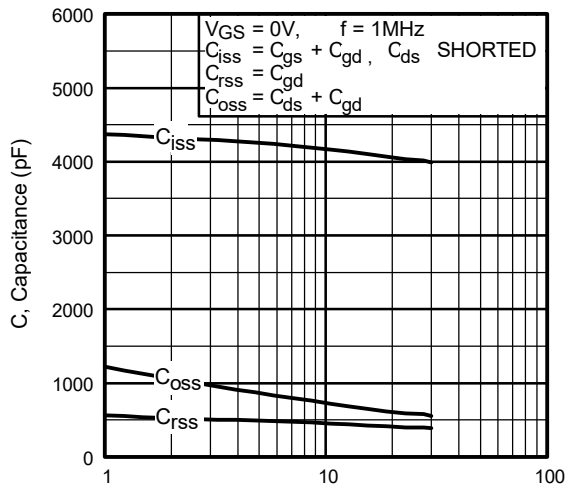


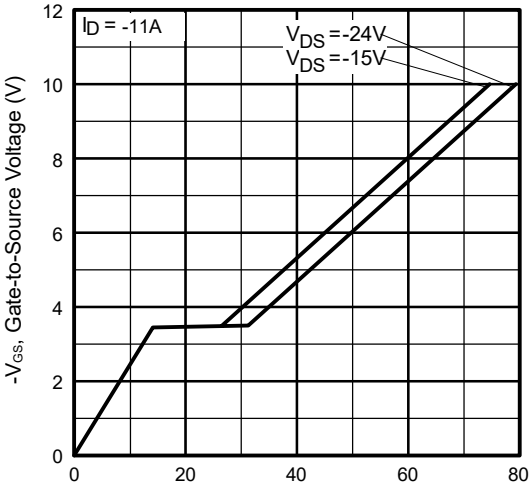
Fig 4. Nomalized On-ResistanceVs. Temperature

8.2Typical Characterisitics



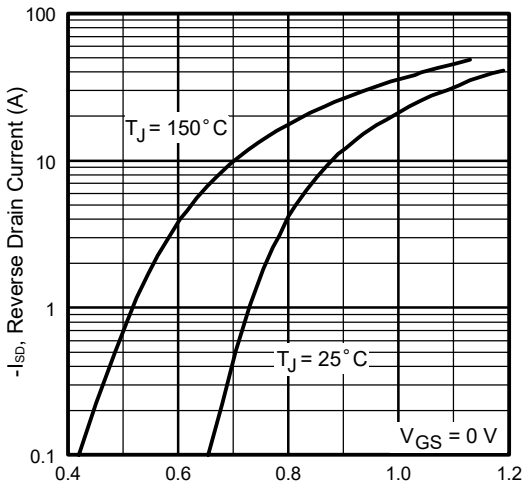
-V_{DS} ,Drain-to-Source Voltage (V)

Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage



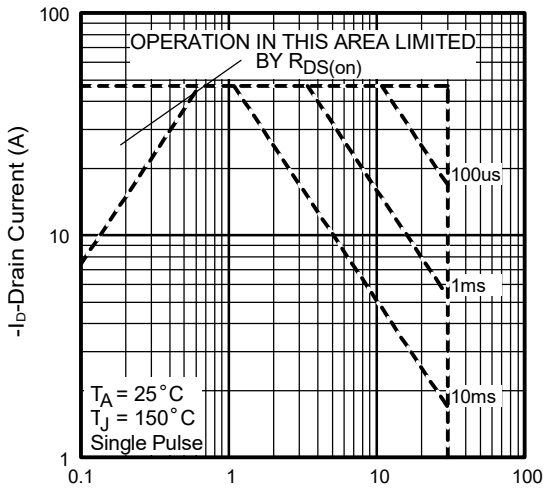
Q_G, Total Gate Charge (nC)

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage



-V_{SD}, Source-to-Drain Voltage (V)

Fig 7. Typical Source-Drain Diode Forward Voltage



-V_{DS}, Drain-to-Source Voltage (V)

Fig 8. Maximum Safe Operating Area

8.3Typical Characterisitics

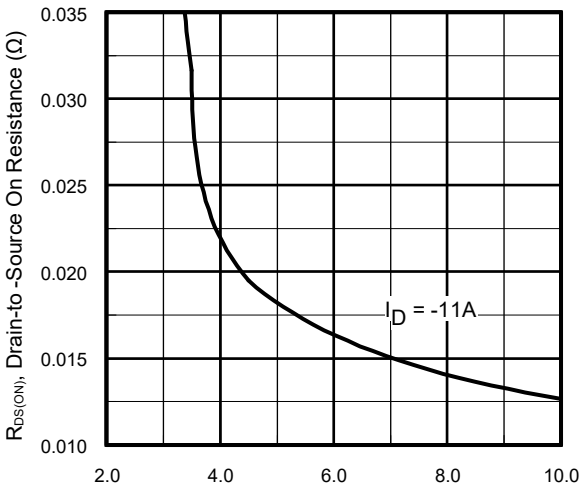


Fig 9. Typical Capacitance Vs. Gate Voltage

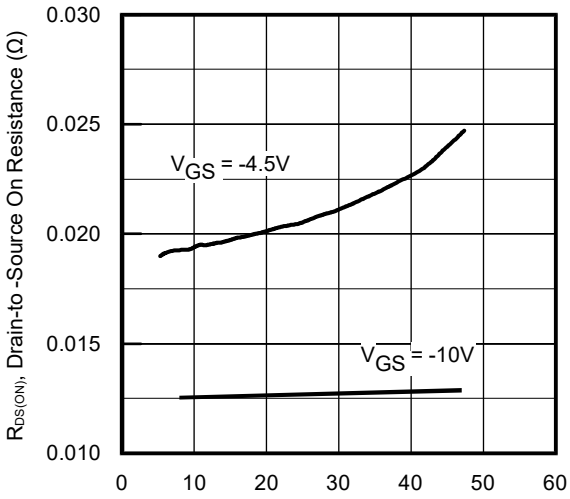


Fig 10. Typical On-Resistance Vs. Drain Current

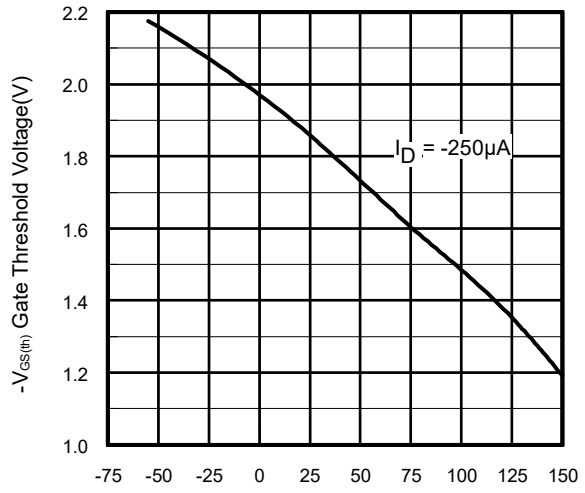


Fig 11. Typical Vgs(th) Vs. Junction Temperature

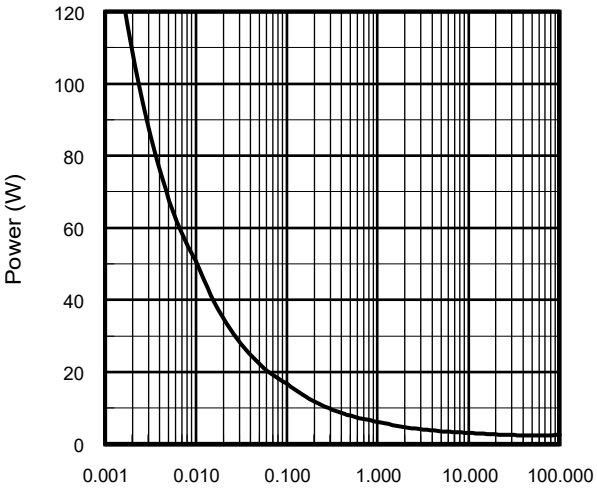


Fig 12. Typical Power Vs. Time

8.4Typical Characterisitics

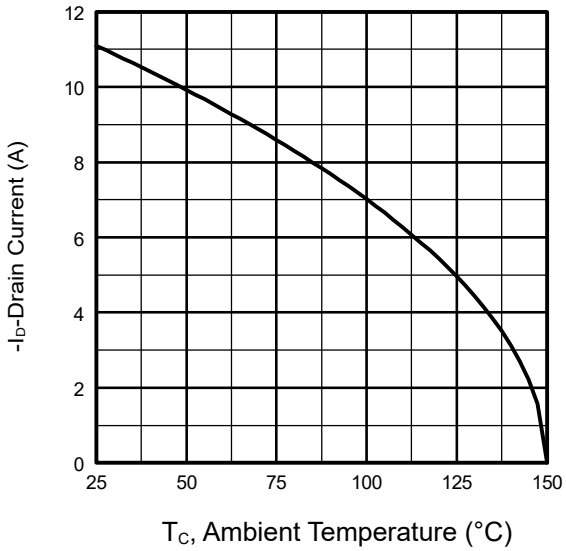


Fig 13. Maximum Drain Current Vs.AmbientTemperature

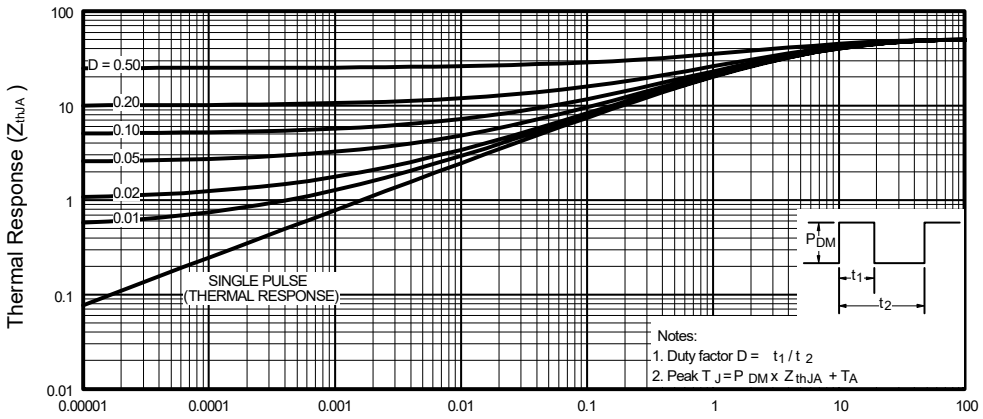


Fig 14. Maximum Effective Transient Themal Impedance, Junction-to-Ambient

8.5Typical Characterisitics

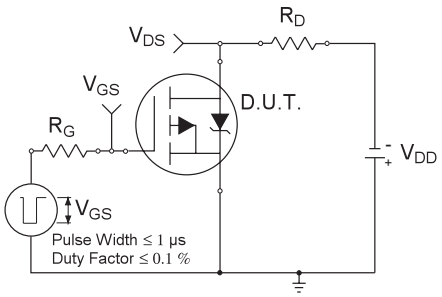


Fig 15a. Switching Time Test Circuit

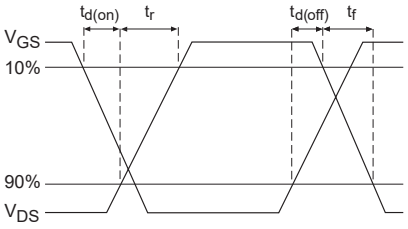


Fig 15b. Switching Time Waveforms

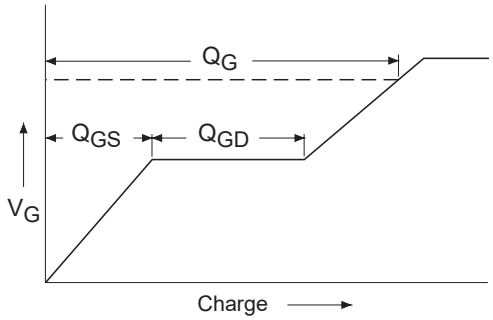


Fig 16a. Basic Gate Charge Wavefomm

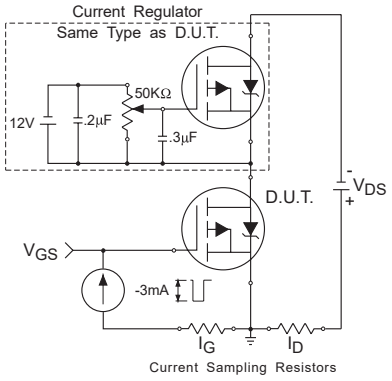
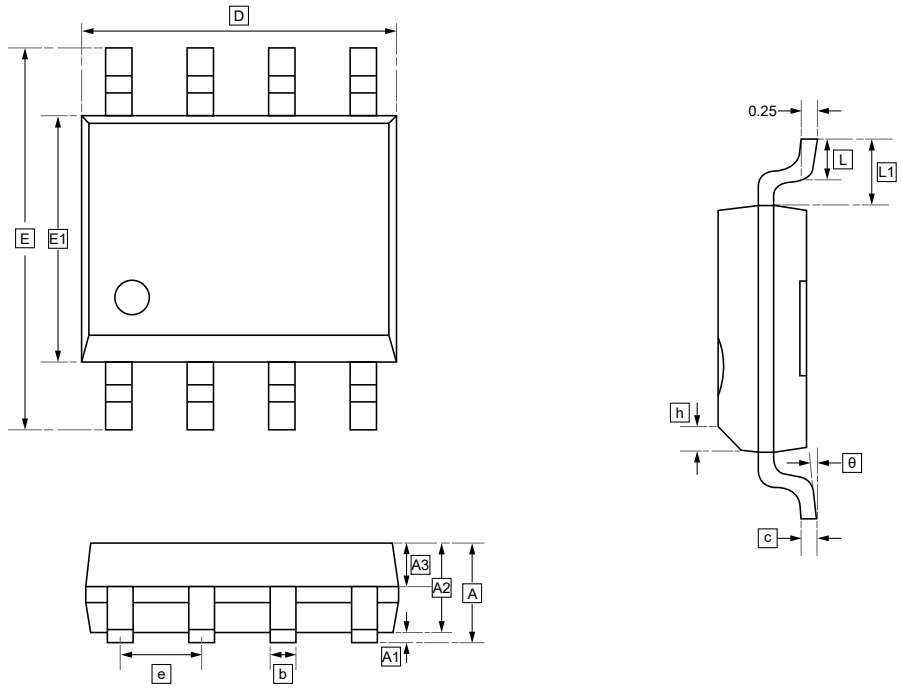


Fig 16b. Gate Charge Test Circuit

9.SOP-8 Package Outline Dimensions

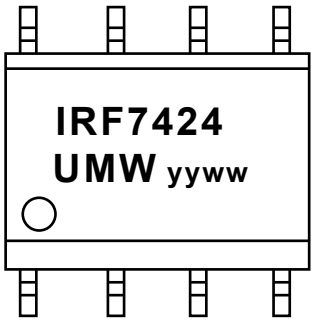


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.70	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.10	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

10.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRF7424TR	SOP-8	3000	Tape and reel

11.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.