N-Channel Enhancement Mode Field Effect Transistor

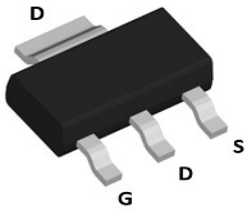
WG09V10

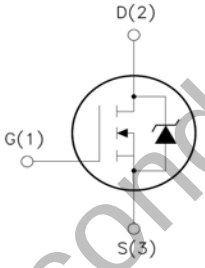
Features:

- ☐ Low Intrinsic Capacitances.
- ☐ Excellent Switching Characteristics.
- ☐ Extended Safe Operating Area.
- ☐ Unrivalled Gate Charge :Qg= 26nC (Typ.).
- ☐ BVDSS=100V,I_D=4 A
- ☐ R_{DS}(on) : 0.095Ω (Typ) @V_G=10V
- ☐ 100% Avalanche Tested

SOT-223

RoHS COMPLIANT





1. Gate (G)
2. Drain (D)
3. Source (S)

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Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	100	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_A=25℃	I_D	4	A
	T_A=70℃		3.2	
Pulsed Drain Current [A]		I_{DM}	16	A
Total Power Dissipation @ T_A=25℃		P_D	2.5	W
Thermal Resistance Junction-to-Ambient [B]		$R_{\theta JA}$	50	℃/ W
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	16	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.1	1.8	3.0	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=4A		95	110	mΩ
		V_{GS}= 4.5V, I_D=3.2A		100	120	
Diode Forward Voltage	V_{SD}	I_S=4A,V_{GS}=0V		0.8	1.2	V
Maximum Body-Diode Continuous Current	I_S				4	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=50V,V_{GS}=0V,f=1MHZ		1070		pF
Output Capacitance	C_{oss}			33		
Reverse Transfer Capacitance	C_{rss}			30		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=50V,I_D=10A		26		nC
Gate-Source Charge	Q_{gs}			5.4		
Gate-Drain Charge	Q_{gd}			5.8		
Reverse Recovery Charge	Q_{rr}	I_F=10A, di/dt=100A/us		30.1		
Reverse Recovery Time	t_{rr}			40		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=50V,R_L=6.4Ω R_{GEN}=3Ω		7		
Turn-on Rise Time	t_r			24		
Turn-off Delay Time	$t_{D(off)}$			24		
Turn-off fall Time	t_f			31		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JL}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

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Typical Performance Characteristics

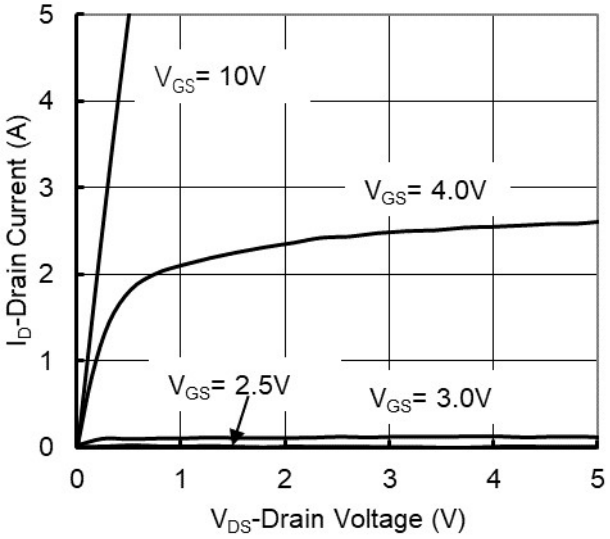

Figure 1. Output Characteristics

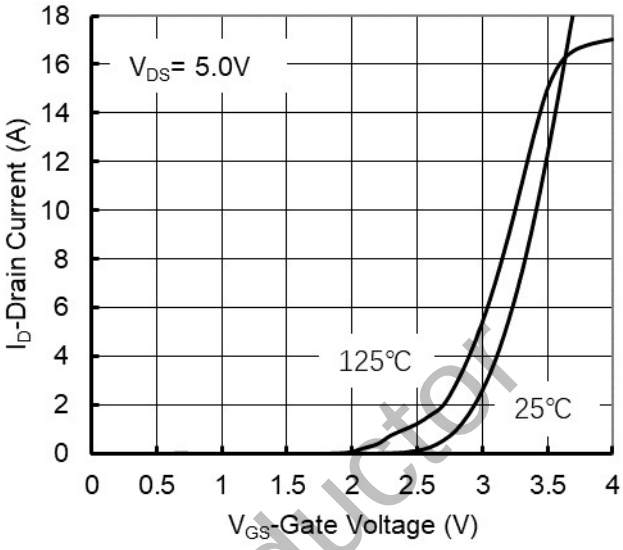

Figure 2. Transfer Characteristics

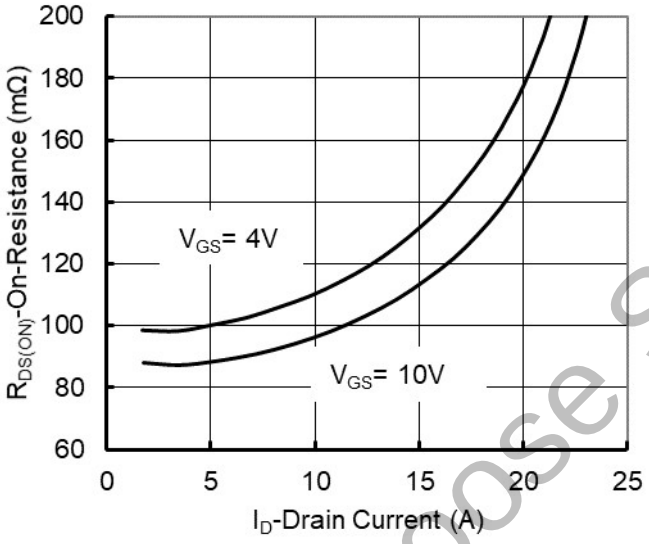

Figure 3. On-Resistance vs. Drain Current and Gate Voltage

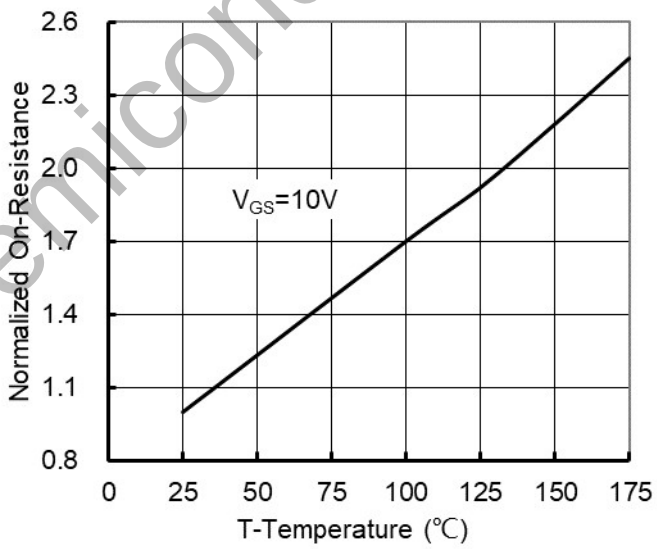

Figure 4. On-Resistance vs. Junction Temperature

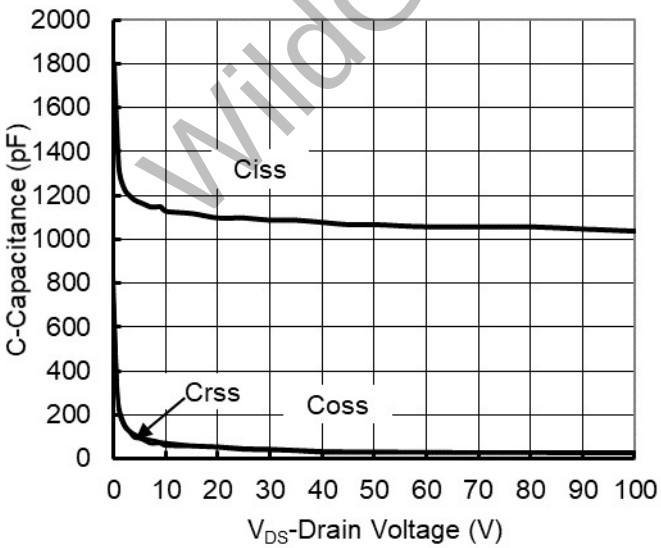

Figure 5. Capacitance Characteristics

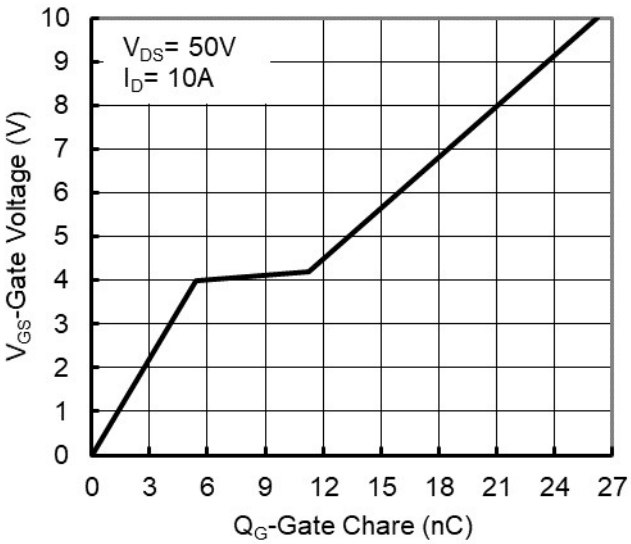

Figure 6. Gate Charge

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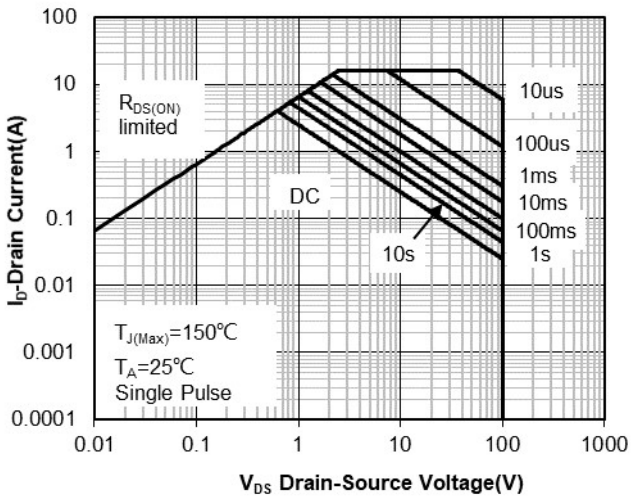

Figure 7. Safe Operation Area

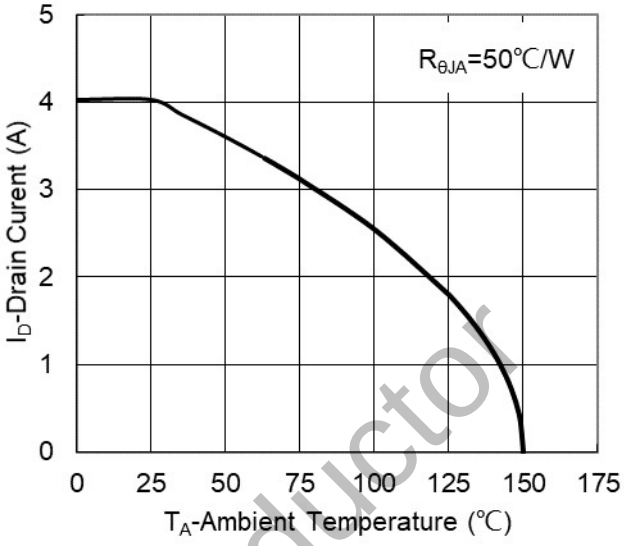

Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

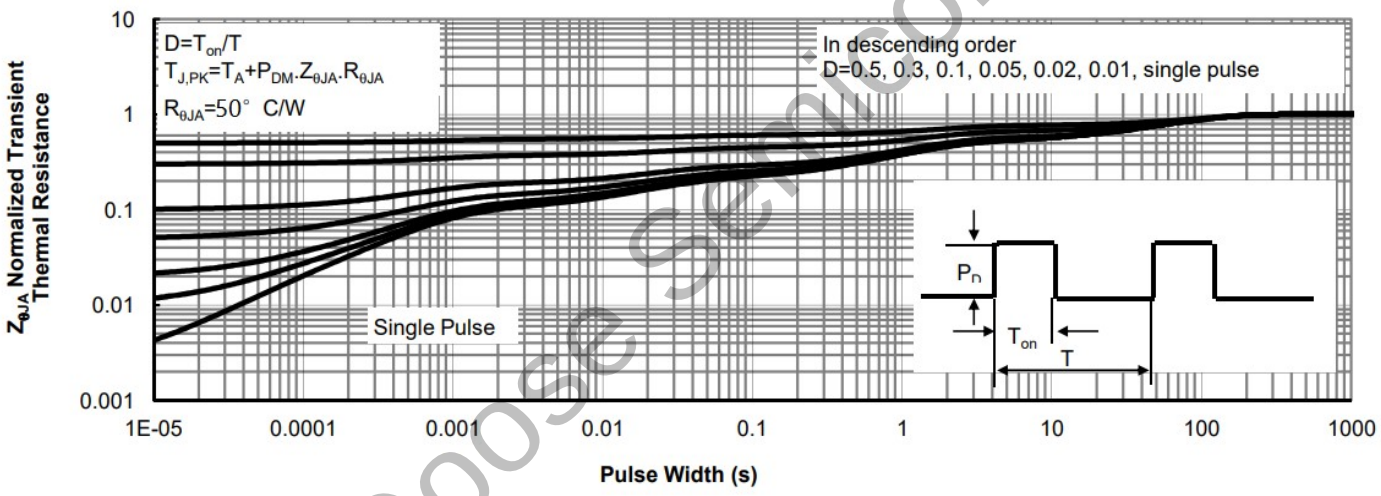

Figure 9. Normalized Maximum Transient Thermal Impedance

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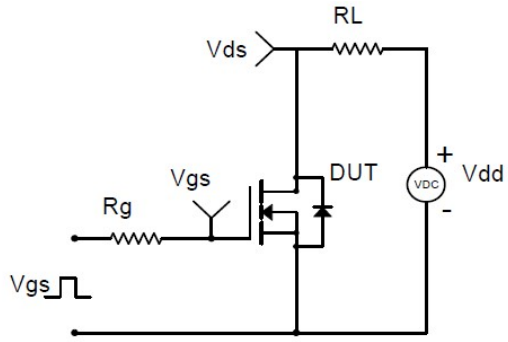
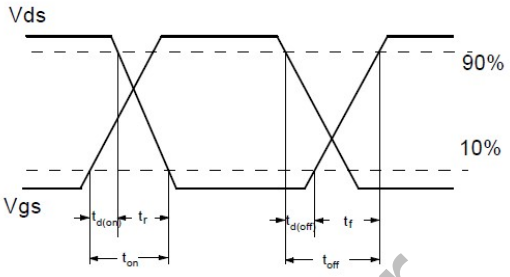
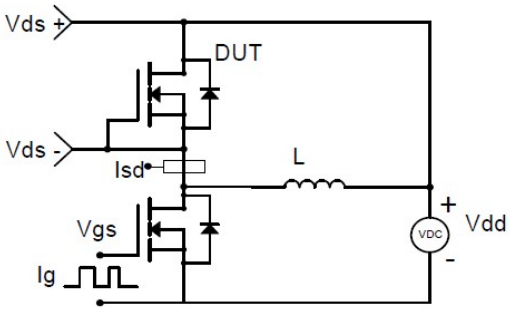
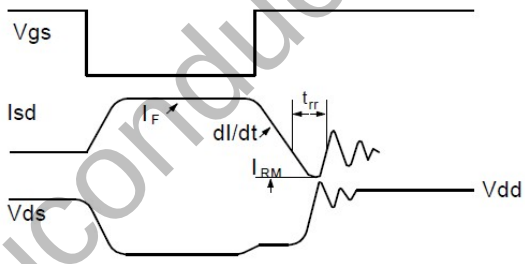


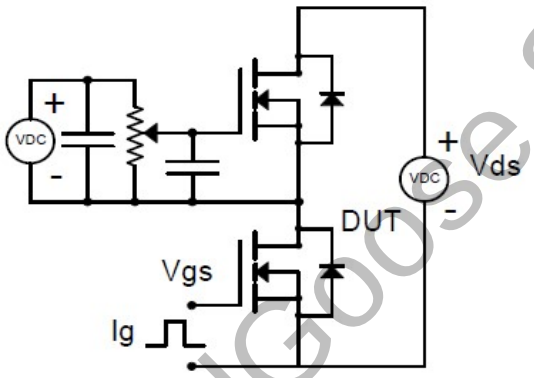


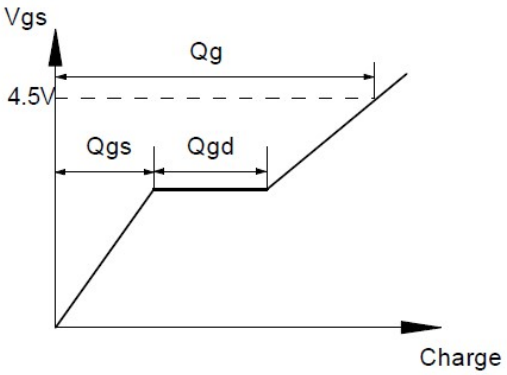
Resistive Switching Test Circuit & Waveforms



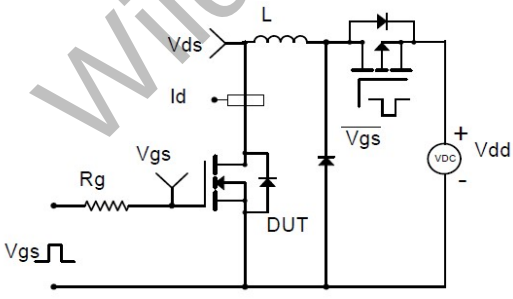


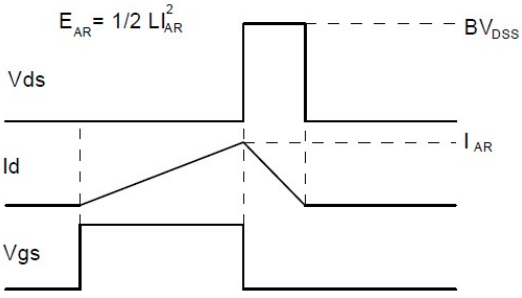
Diode Recovery Test Circuit & Waveforms





Gate Charge Test Circuit & Waveform





Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

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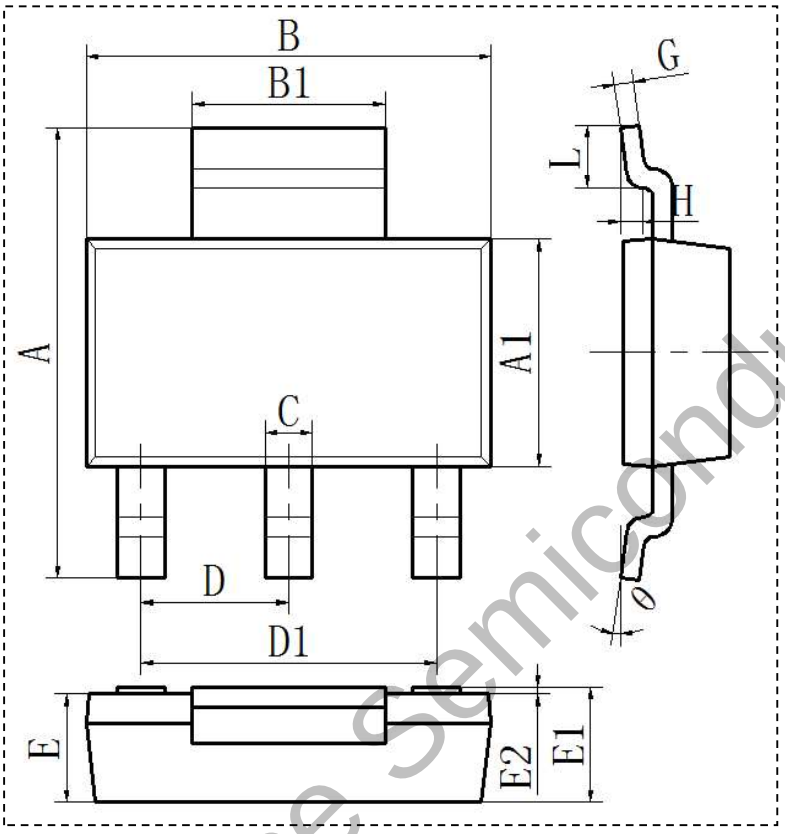
Package Dimension

SOT-223 （单位：mm）



符号	标准	下公差	上公差	下限值	上限值
A	6.95	-0.24	0.24	6.71	7.19
A1	3.5	-0.1	0.1	3.4	3.6
B	6.4	-0.1	0.1	6.2	6.4
B1	3.00	-0.1	0.1	2.9	3.1
C	0.74	-0.08	0.08	0.66	0.82
D	2.3	-0.05	0.05	2.25	2.35
D1	4.6	-0.1	0.1	4.5	4.7
E	1.6	-0.1	0.1	1.5	1.7
E1	1.66	-0.14	0.14	1.52	1.8
E2(测试后)	/	/	/	0	0.1
E2（成型后）	/	/	/	0.02	0.08
G	0.3	-0.05	0.05	0.25	0.35
H	0.25	-0.05	0.05	0.20	0.30
L	0.95	-0.15	0.15	0.8	1.1
θ	8	/	/	8	8

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