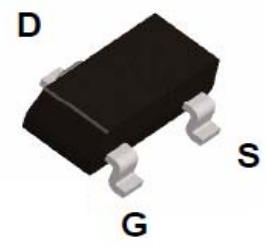
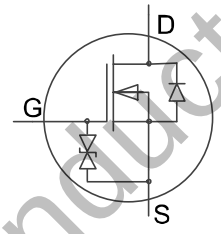
WGF601D-G

SOT-23

RoHS COMPLIANT





Schematic diagram

Features:

- ☐ **N-Channel**
- ☐ **ESD improved Capability**
- ☐ **Depletion Mode**
- ☐ **dv/dt rated**
- ☐ **Pb-free lead plating; ROHS compliant**
- ☐ **Halo en Free**

Absolute（Tc= 25℃ unless otherwise specified）：

Symbol	Parameter	Rating	Units
V_{DSX}	Drain-to-Source Voltage	600	V
I_D	Continuous Drain Current	0.030	A
	Continuous Drain Current T_C =70 C	0.024	A
I_{DM} [a1]	Pulsed Drain Current	0.120	A
V_{GS}	Gate-to-Source Voltage	±20	V
dv/dt [a2]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	0.5	W
$V_{ESD(G-S)}$	Gate source ESD (HBM-C= 100pF, R=1.5kΩ)	1200	V
T_J， T_{stg}	Operating Junction and Storage Temperature Range	150，–55 to 150	℃

Electrical Characteristics（Tc= 25℃ unless otherwise specified）：

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSX}	Drain to Source Breakdown Voltage	V_{GS}=-5V, I_D=250μA	600	--	--	V
$I_{D(off)}$	Off-state Drain to Source Current	V_{DS} =600V, V_{GS}= -5V	--	--	0.1	μA
		V_{DS} =480V, V_{GS}= -5V Ta=125 C			10	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS} =+20V	--	--	10	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-20V	--	--	-10	μA

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ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
Idss	On-state drain current	V_{GS}=0V, V_{DS} =25V	12			mA
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=0V,I_D=3mA	--	100	300	Ω
		V_{GS}=10V,I_D=16mA		85	300	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = 3V, I_D =8.0μA	-2.7		-1.0	V

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Trans conductance	V_{DS}=50V, I_D =0.01A		0.005	--	S
C_{iss}	Input Capacitance	V_{GS} =-5V V_{DS} = 25V f = 1.0MHz	--	15.5		pF
C_{oss}	Output Capacitance		--	4.7		
C_{rss}	Reverse Transfer Capacitance		--	1.6		

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D =0.01A V_{DD} =300V V_{GS} = -5…7V R_G =6.0Ω	--	6.6	--	ns
tr	Rise Time		--	21.6	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	6.2	--	
t_f	Fall Time		--	96.4	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)	Ta=25° C	--	--	0.025	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	0.100	A
V_{SD}	Diode Forward Voltage	I_F=16mA,V_{GS}= -5V	--	--	1.2	V

Symbol	Parameter	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient	250	℃/W

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Gate-source Zener diode						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{GSO}	Gate-source breakdown voltage	I_{GS}= ±1mA(Open Drain)	20			V
The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.						

[a1]: Repetitive rating; pulse width limited by maximum junction temperature

[a2]: I_F =0.01A,di/dt ≤100A/us,V_{DD}≤$BV_{DS,}$ Start T_J=25℃

[a3]: Recommend soldering temperature defined by IPC/JEDEC J-STD 020

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Characteristics Curve:

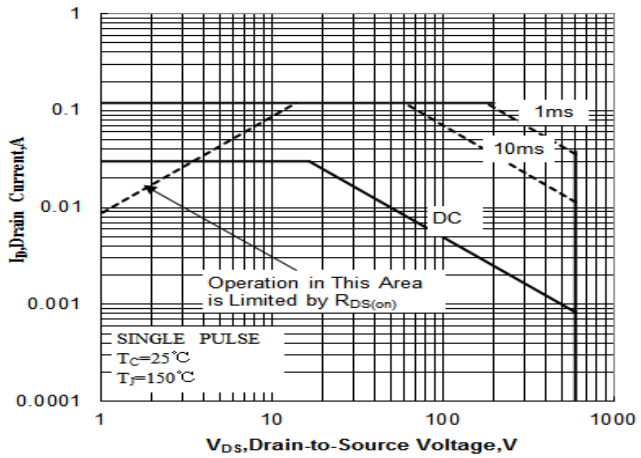


Figure 1 Maximum Forward Bias Safe Operating Area

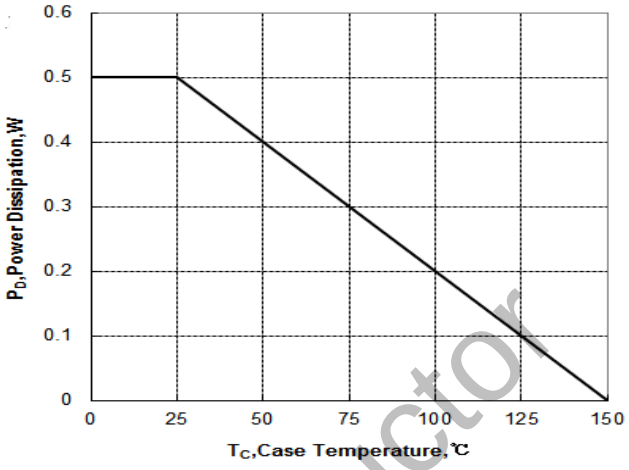


Figure 2 Maximum Power dissipation vs Case Temperature

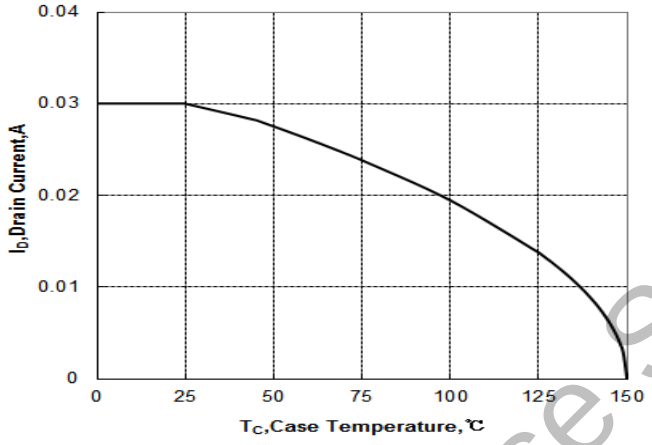


Figure 3 Maximum Continuous Drain Current vs Case Temperature

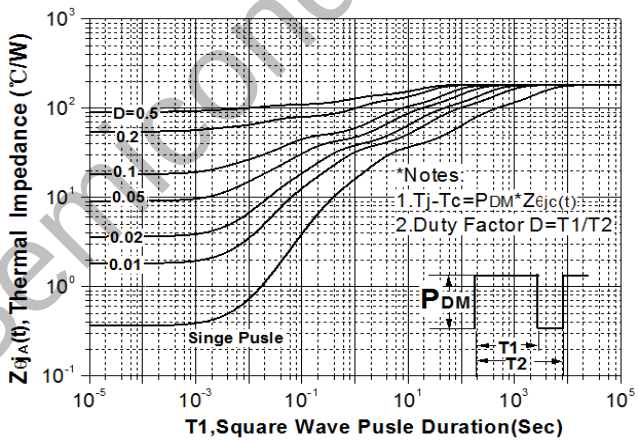


Figure 4 Max. transient Thermal Impedance RthJA

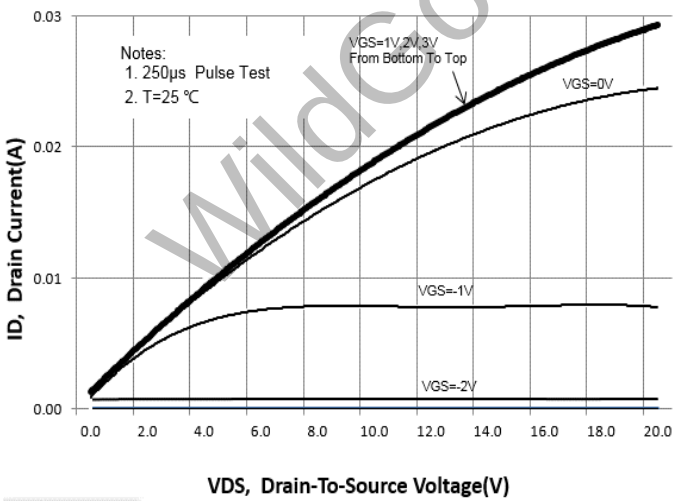


Figure 5 Typical Output Characteristics

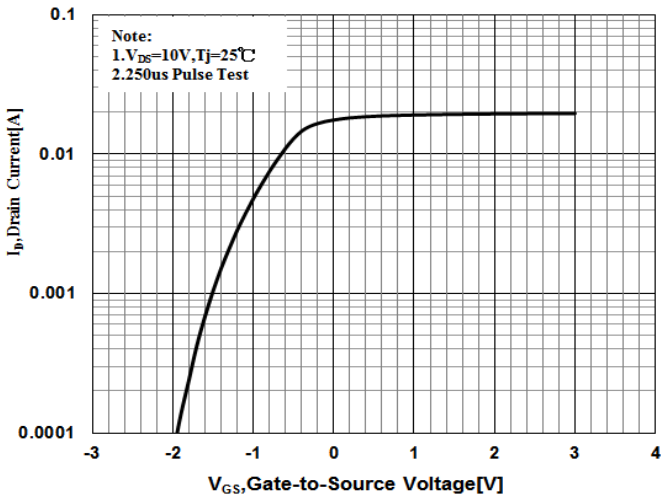


Figure 6 Typical Transfer Characteristics

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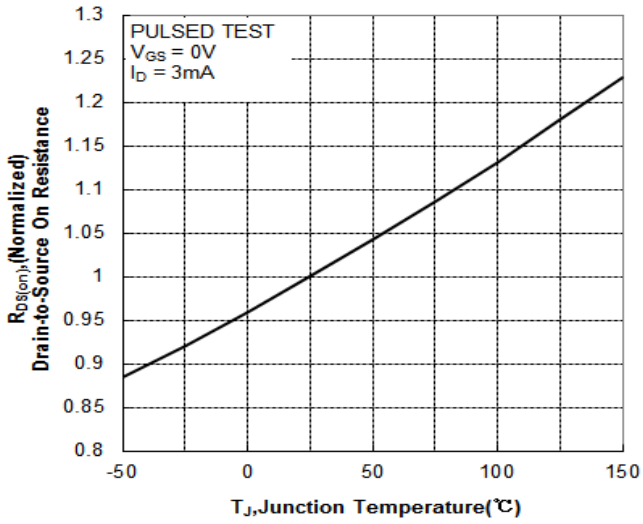


Figure 7 Typical Drian to Source on Resistance vs Junction Temperature

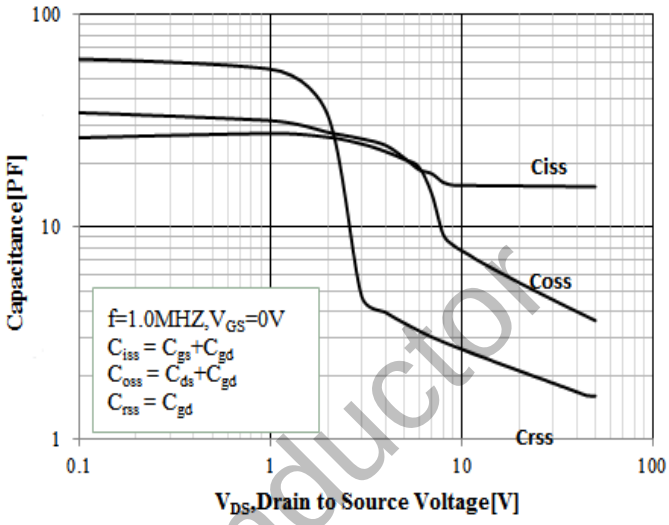


Figure 8 Typical Capacitance vs Drain to Source Voltage

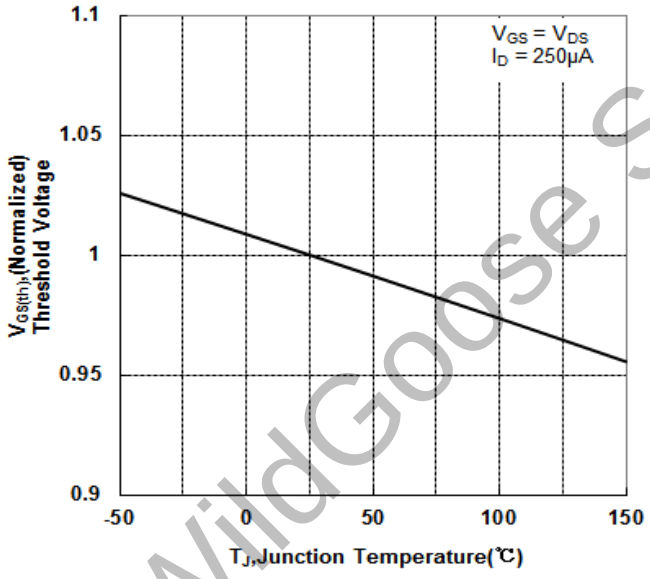


Figure 9 Typical Theshold Voltage vs Junction Temperature

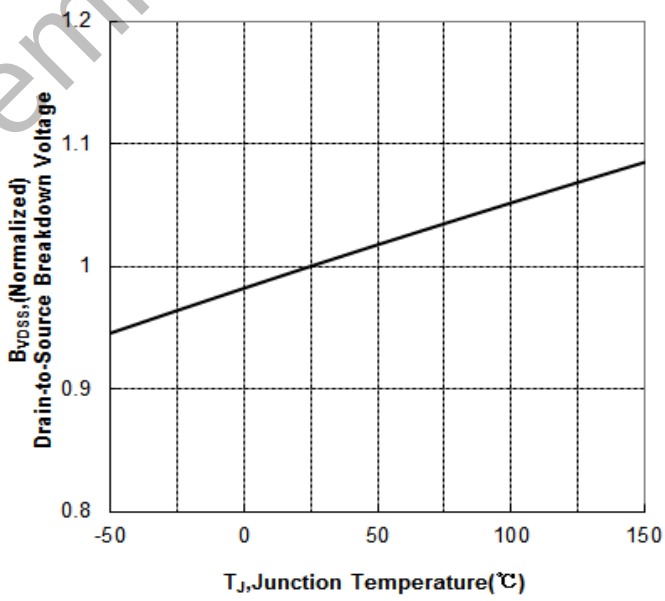


Figure 10 Typical Breakdown Voltage vs Junction Temperature

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Test Circuit and Waveform

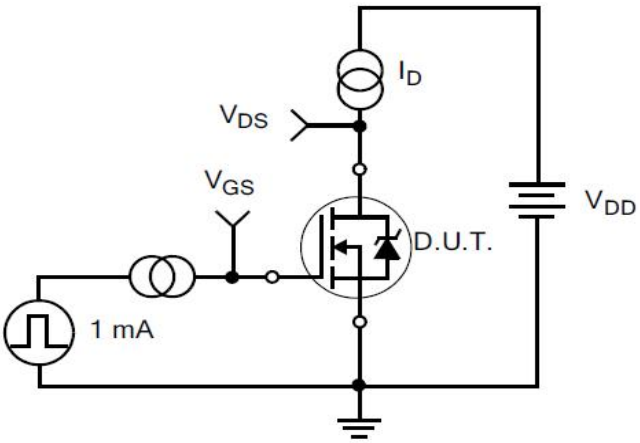


Figure 11. Gate Charge Test Circuit

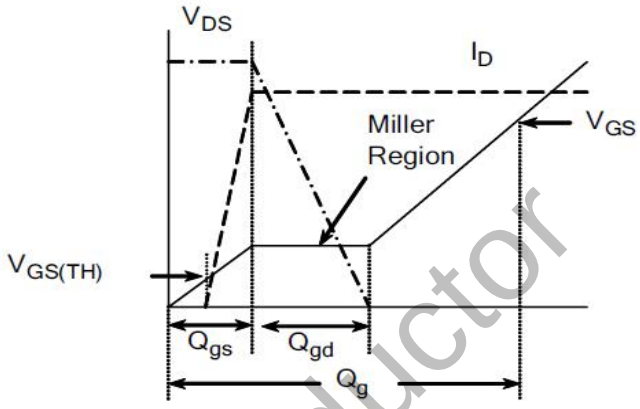


Figure 12. Gate Charge Waveforms

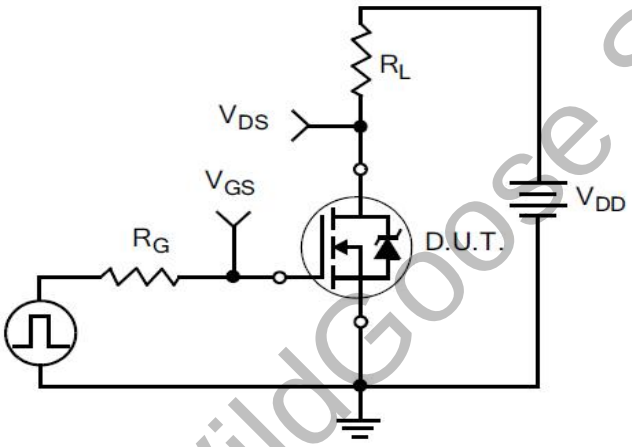


Figure 13. Resistive Switching Test Circuit

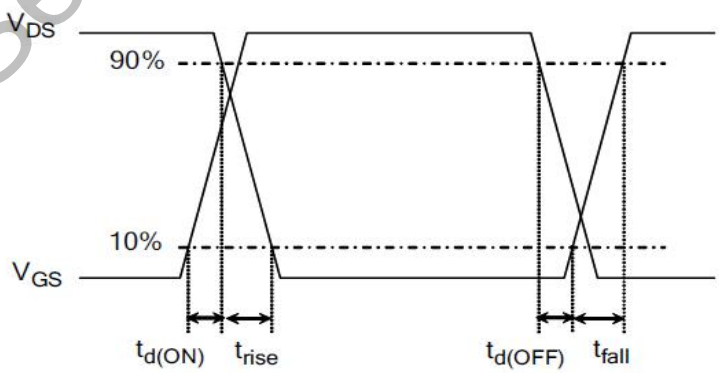


Figure 14. Resistive Switching Waveforms

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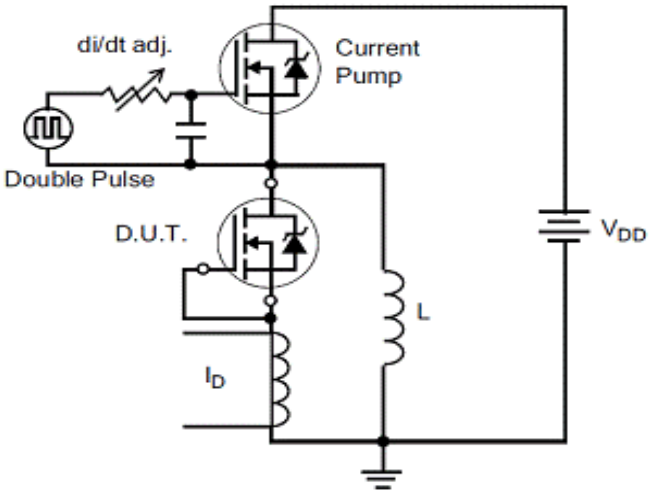


Figure 15. Diode Reverse Recovery Test Circuit

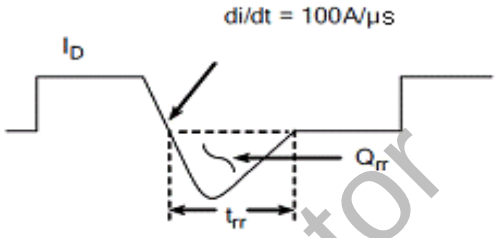


Figure 16. Diode Reverse Recovery Waveform

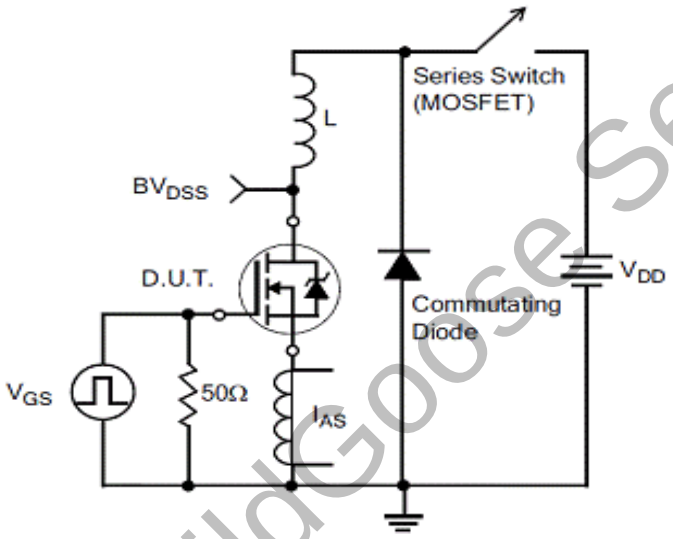


Figure 17.Unclamped Inductive Switching Test Circuit

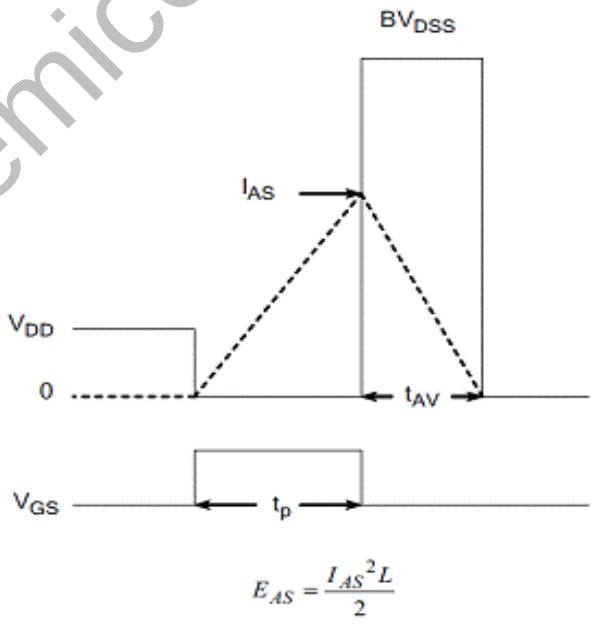


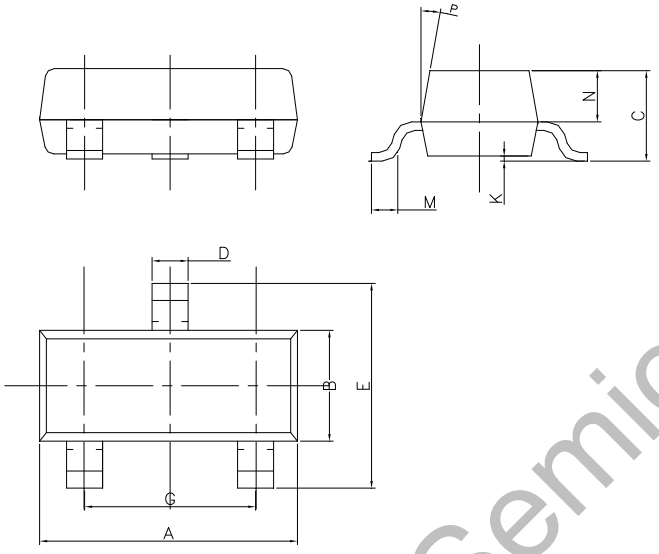
Figure 18.Unclamped Inductive Switching Waveform

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Package Dimension

SOT-23

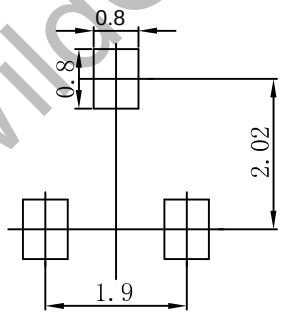
Unit: mm



DIM	MILLIMETERS
A	2.85~3.04
B	1.30±0.10
C	1.00±0.10
D	0.45±0.05
E	2.25~2.55
G	1.90±0.1
K	0.00−0.10
M	0.20 MIN
N	0.60±0.10
P	7±2°

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SOT-23 Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.