1. DESCRIPTION

The XLISO7420DR, XLISO7420MDR and XLISO7421DR provide galvanic isolation up to 2500 V_{RMS} for 1 minute per UL. These digital isolators have two isolated channels. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuit from entering the local ground and interfering with or damaging sensitive circuitry. The suffix M indicates wide temperature range (–40°C to 105°C).

These devices have TTL input thresholds and require two supply voltages, 3.3 or 5 V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply.

Note: The XLISO7420DR and XLISO7421DR are specified for signaling rates up to 1 Mbps. Due to their fast response time, under most cases, these devices will also transmit data with much shorter pulse widths. Designers should add external filtering to remove spurious signals with input pulse duration <20 ns if desired.

2. FEATURES

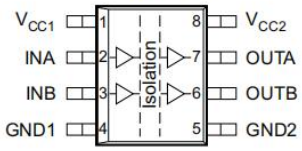
- Highest Signaling Rate: 1 Mbps
- Low Power Consumption, Typical I_{cc} per Channel (3.3-V operation):
- XLISO7420DR: 1.1 mA, XLISO7421DR: 1.5 mA
- Low Propagation Delay – 9 ns Typical
- Low Skew – 300 ps Typical
- Wide T_A Range: –40°C to 105°C
- 50-kV/μs Transient Immunity, Typical
- Over 25-Year Isolation Integrity at Rated Voltage
- Operates From 3.3-V and 5-V Supply and Logic Levels
- 3.3-V and 5-V Level Translation
- Narrow Body SOIC-8 Package

3. Applications

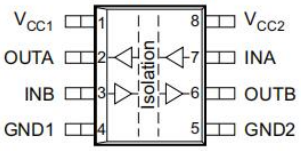
- Optocoupler Replacement in:
  - Industrial Fieldbus
    - Profibus
    - Modbus
    - DeviceNet™ Data Buses
  - Servo Control Interface
  - Motor Control
  - Power Supplies
  - Battery Packs

4. Pin Configuration and Functions

XLISO7420: D Package
8-Pin SOIC
(Top View)



XLISO7421: D Package
8-Pin SOIC
(Top View)



Pin Functions

PIN			I/O	DESCRIPTION
NAME	XLISO7420DR	XLISO7421DR		
GND1	4	4	—	Ground connection for V_{CC1}
GND2	5	5	—	Ground connection for V_{CC2}
INA	2	7	I	Input, channel A
INB	3	3	I	Input, channel B
OUTA	7	2	O	Output, channel A
OUTB	6	6	O	Output, channel B
V_{CC1}	1	1	—	Power supply, V_{CC1}
V_{CC2}	8	8	—	Power supply, V_{CC2}

5. Specifications

5.1. Absolute Maximum Ratings

See(1)		MIN	MAX	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}	-0.5	6	V
V_I	Voltage at IN, OUT	-0.5	V_{CC}+ 0.5(3)	V
I_O	Output current	-15	15	mA
$T_{J(max)}$	Maximum junction temperature		150	℃
T_{stg}	Storage temperature	-40	150	℃

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

5.2. ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Field-induced charged-device model, JEDEC Standard 22, Test Method C101	±1500	
		Machine model, ANSI/ESDS5.2-1996	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3. Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage - 3.3-V operation		3.15	3.3	3.45	V
	Supply voltage - 5-V operation		4.75	5	5.25	
I_{OH}	High-level output current		-4			mA
I_{OL}	Low-level output current				4	mA
V_{IH}	High-level input voltage		2		5.25	V
V_{IL}	Low-level input voltage		0		0.8	V
$1/t_{ui}$	Signaling rate		0		1	Mbps
t_{ui}	Input pulse duration		1			us
T_J(1)	Junction temperature		-40		136	℃
T_A	Ambient temperature	7420, 7421	-40	25	105	℃
		7420M	-40	25	105	℃

(1) To maintain the recommended operating conditions for TJ, see the *Thermal Information*

5.4 Thermal Information

THERMAL METRIC(1)			742x D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K Board	212	°C/W
		High-K Board	116.6	
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance		71.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		57.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter		28.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter		56.8	°C/W

（1） For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5. Electrical Characteristics: V_{CC1} and V_{CC2} at 5 V ±5%

T_A = –40°C to 105°C for XLISO742x

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 6		V_{CCO}(1) – 0.8	4.6		V
		I_{OH} = –20 µA; see Figure 6		V_{CCO} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 6			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 6			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INX at 0 Vor V_{CCI}(1)				10	µA
I_{IL}	Low-level input current			-10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see Figure 6		25	50		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
XLISO7421							
I_{CC1}	Supply current for I_{CC1}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15pF load		0.4	1	mA
I_{CC2}	Supply current for I_{CC2}				3	6	
XLISO7421							
I_{CC1}	Supply current for I_{CC1}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15pF load		2	4	mA
I_{CC2}	Supply current for I_{CC2}				2	4	

(1) V_{CCI} = Input-side power supply, V_{CCO} = Output-side power supply

5.6 . Electrical Characteristics: V_{CC1} at 5 V ±5%, V_{CC2} at 3.3 V ±5%

T_A = –40°C to 105°C for XLISO742x

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 6	XLISO7421(5-Vside)	V_{CCO}(1)– 0.8	4.6		V
			XLISO7420/7421(3.3-Vside)	V_{CCO}– 0.4	3		
		I_{OH} = –20 µA; see Figure 6		V_{CCO}– 0.1	V_{CC}		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 6			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 6			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INX at 0 Vor V_{CCI}(1)				10	µA
I_{IL}	Low-level input current			-10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see Figure 8		25	40		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic ICC measurement)							
XLISO7420							
I_{CC1}	Supply current for I_{CC1}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15pF load		0.4	1	mA
I_{CC2}	Supply current for I_{CC2}				2	4.5	
XLISO7421							
I_{CC1}	Supply current for I_{CC1}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15pF load		2	4	mA
I_{CC2}	Supply current for I_{CC2}				1.5	3.5	

（1）V_{CCI} = Input-side power supply, V_{CCO} = Output-side power supply

5.7 . Electrical Characteristics: V_{CC1} at 3.3 V ±5%, V_{CC2} at 5 V ±5%

T_A = –40°C to 105°C for XLISO742x

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 6	XLISO7420/7421(5-Vside)	V_{CCO}(1) – 0.8	4.6		V
			XLISO7421(3.3-Vside)	V_{CCO} – 0.4	3		
		I_{OH} = –20 µA; see Figure 6		V_{CCO} – 0.1	V_{CC}		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 6			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 6			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INX at 0 Vor V_{CCI}(1)				10	µA
I_{IL}	Low-level input current			-10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see Figure 8		25	40		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
XLISO7420							
I_{CC1}	Supply current for V_{CCI}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15pF load		0.2	0.7	mA
I_{CC2}	Supply current for V_{CC2}				3	6	
XLISO7421							
I_{CC1}	Supply current for V_{CCI}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15pF load		1.5	3.5	mA
I_{CC2}	Supply current for V_{CC2}				2	4	

(1) V_{CCI} = Input-side power supply, V_{CCO} = Output-side power supply

5.8 . Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V ±5%

T_A = –40°C to 105°C for XLISO742x

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 6		V_{CCO}(1)– 0.4	3		V
		I_{OH} = –20 µA; see Figure 6		V_{CCO}– 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 6			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 6			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INX at 0 Vor V_{CCI}(1)				10	µA
I_{IL}	Low-level input current			-10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see Figure 6		25	40		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
XLISO7420							
I_{CC1}	Supply current for V_{CCI}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15pF load		0.2	0.7	mA
I_{CC2}	Supply current for V_{CC2}				2	4.5	
XLISO7421							
I_{CC1}	Supply current for V_{CCI}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15pF load		1.5	3.5	mA
I_{CC2}	Supply current for V_{CC2}				1.5	3.5	

(1) V_{CCI} = Input-side power supply, V_{CCO} = Output-side power supply

5.9. Power Dissipation Characteristics

THERMAL METRIC		ISO742x D (SOIC) 8 PINS	UNIT
P_D Device power dissipation	V_{CC1} = V_{CC2} = 5.25 V, T_J = 150°C, C_L = 15 pF Input a 1-Mbps 50% duty-cycle square wave	55	mW

5.10. Switching Characteristics: V_{CC1} and V_{CC2} at 5 V ±5%

T_A= –40°C to 105°C for XLISO742x

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	see Figure 6		9	14	ns
$P_{WD(1)}$	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.3	3.7	ns
$t_{sk(pp)}$	Part-to-part skew time				4.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time				3.6	
t_r	Output signal rise time	see Figure 6		1		ns
t_f	Output signal fall time			1		ns
t_{fs}	Fail-safe output delay time from input power loss	see Figure 7		6		µs

(1) Also known as pulse skew

5.11. Switching Characteristics: V_{CC1} at 5 V ±5%, V_{CC2} at 3.3 V ±5%

T_A = –40°C to 105°C for XLISO742x

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	see Figure 6		10	17	ns
$P_{WD(1)}$	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			0.5	5.6	ns
$t_{sk(pp)}$	Part-to-part skew time				6.3	ns
$t_{sk(o)}$	Channel-to-channel output skew time				4	
t_r	Output signal rise time	see Figure 6		2		ns

(1) Also known as pulse skew

5.12. Switching Characteristics: V_{CC1} at 5 V ±5%, V_{CC2} at 3.3 V ±5% (continued)

T_A = –40°C to 105°C for XLISO742x

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	see Figure 7		6		ns

5.13. Switching Characteristics: V_{CC1} at 3.3 V ±5%, V_{CC2} at 5 V ±5%

T_A = –40°C to 105°C for XLISO742x

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	see Figure 6		10	17	ns
$P_{WD(1)}$	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			0.5	4	ns
$t_{sk(pp)}$	Part-to-part skew time				8.5	ns
$t_{sk(o)}$	Channel-to-channel output skew time				4	
t_r	Output signal rise time	see Figure 6		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	see Figure 7		6		μs

(1) Also known as pulse skew.

5.14. Switching Characteristics: V_{CC1} and V_{CC2} at 3.3 V ±5%

T_A = –40°C to 105°C for XLISO742x

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	see Figure 6		12	20	ns
$P_{WD(1)}$	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			1	5	ns
$t_{sk(pp)}$	Part-to-part skew time				6.8	ns
$t_{sk(o)}$	Channel-to-channel output skew time				5.5	
t_r	Output signal rise time	see Figure 6		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	see Figure 7		6		μs

(1) Also known as pulse skew.

5.15. Typical Characteristics

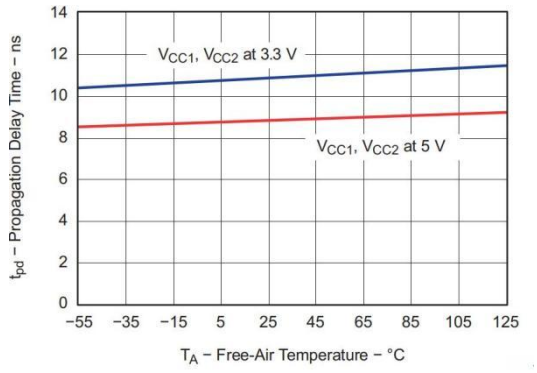


Figure 1. Propagation Delay Time vs Free-Air Temperature

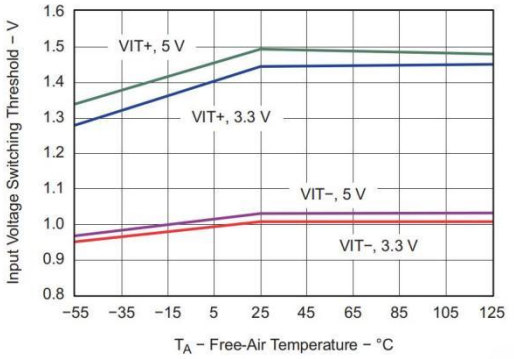


Figure 2. Input Voltage Switching Thresh old vs Free-AirTemperature

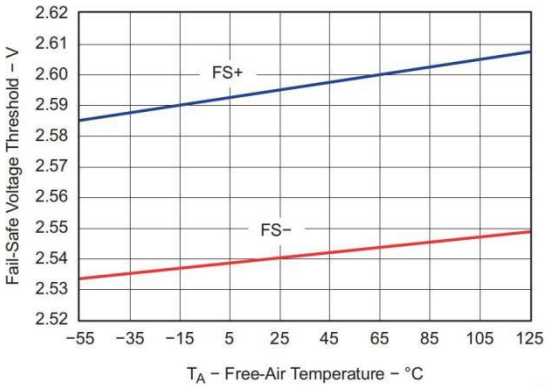


Figure 3. Fail-Safe Voltage Threshold vs Free-Air Temperature

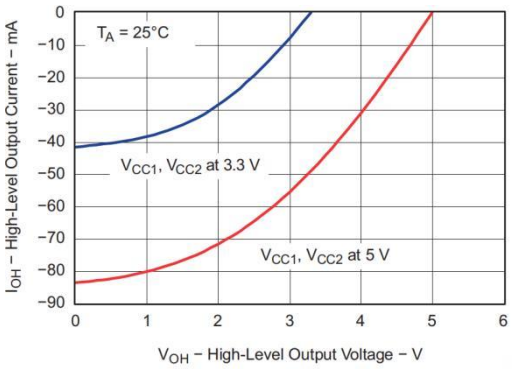


Figure 4. High-Level Output Current vs High-Level Output Voltage

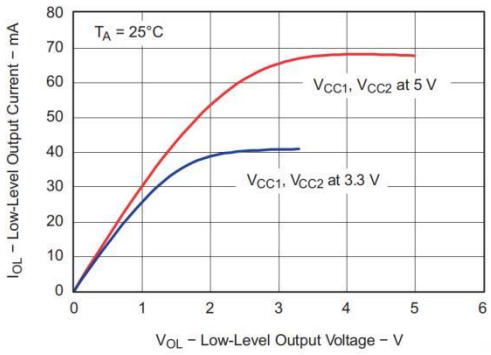
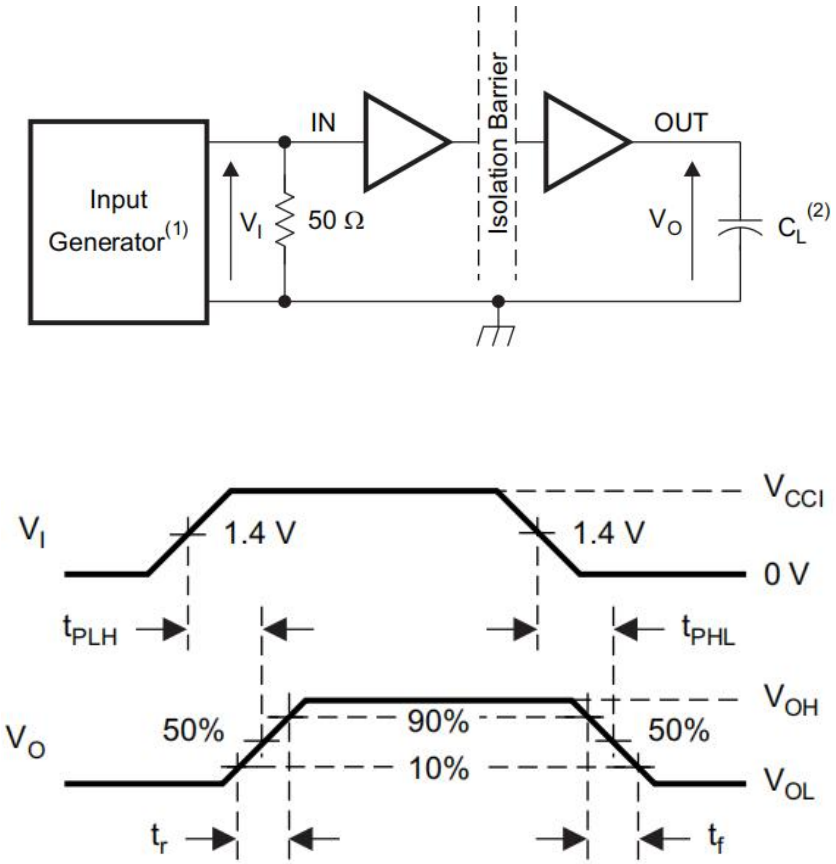


Figure 5. Low-Level Output Current vs Low-Level Output Voltage

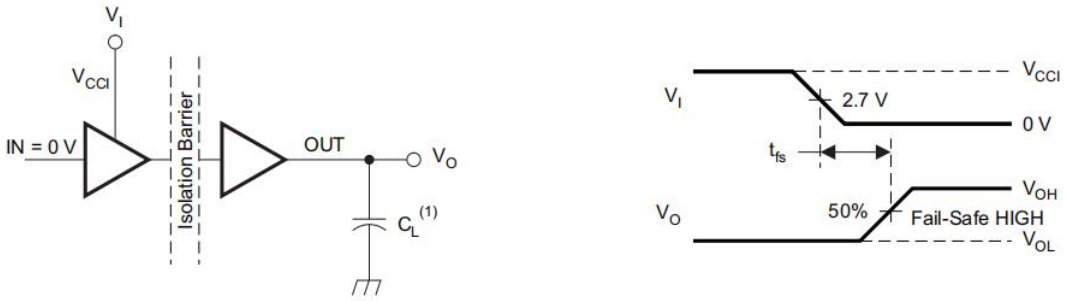
6. Parameter Measurement Information



(1) The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, ZO = 50 Ω. At the input, a 50-Ω resistor is required to terminate the Input Generator signal. It is not needed in actual application.

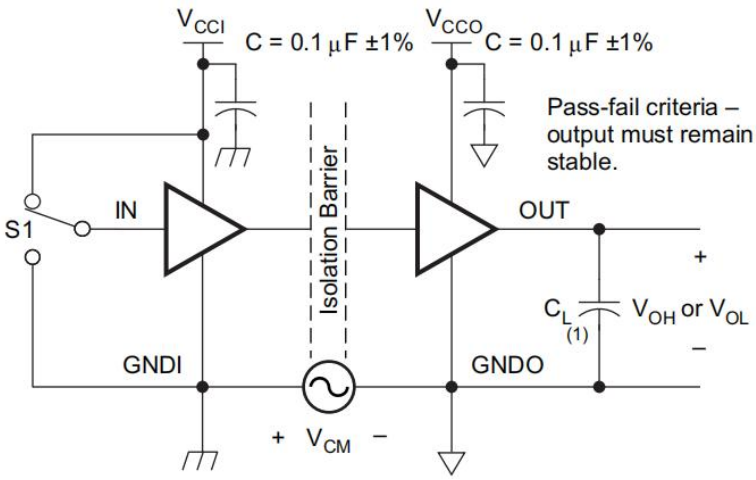
(2) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6. Switching Characteristic Test Circuit and Voltage Waveforms



(1) C_L = 15 pF ± 20% includes instrumentation and fixture capacitance.

Figure 7. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 8. Common-Mode Transient Immunity Test Circuit

7. Detailed Description

7.1 Overview

The isolator in Figure 9 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 1 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single- ended input signal entering the HF-channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

7.2 Functional Block Diagram

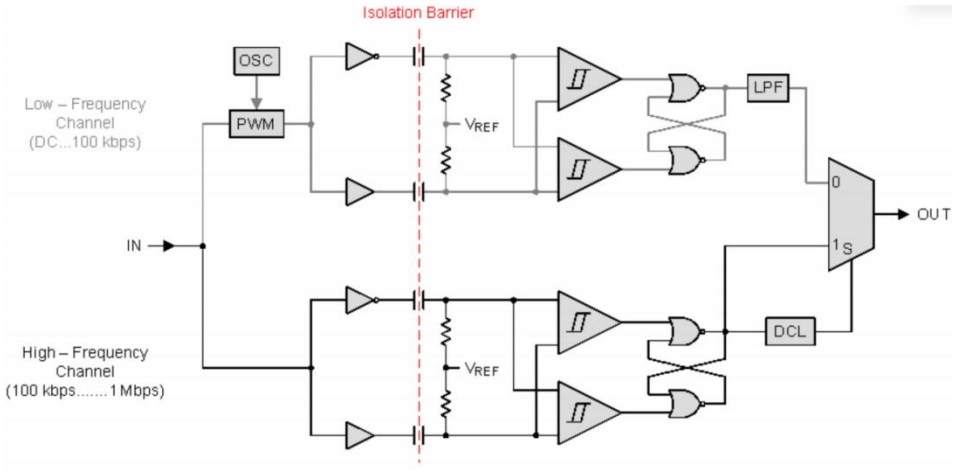


Figure 9. Conceptual Block Diagram of a Digital Capacitive Isolator

7.3 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 212°C/W, V_I = 5.25 V, T_J = 150°C, T_A = 25°C			112	mA
		θ_{JA} = 212°C/W, V_I = 3.45 V, T_J = 150°C, T_A = 25°C			171	
T_S	Maximum safety temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed in the JESD51-3, Low-Effective-Thermal-Conductivity Test Board for Leaded Surface-Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

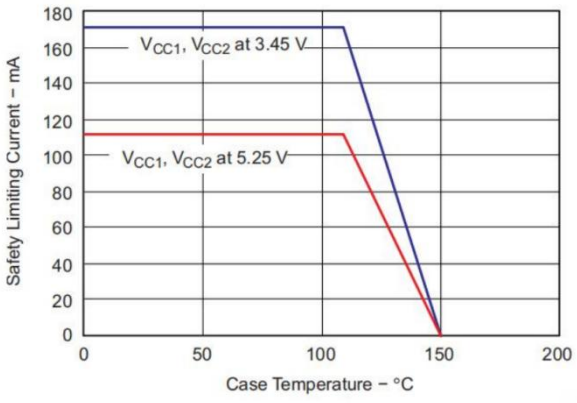


Figure 10. θ_{JC} Thermal Derating Curve per VDE

7.4 Device Functional Modes

Table 2. Function Table(1)

VCCI	VCCO	INPUT INA, INB	OUTPUT OUTA, OUTB
PU	PU	H	H
		L	L
		Open	H(2)
PD	PU	X	H(2)
X	PD	X	Undetermined

(1) V_{CCI} = Input-side power supply; V_{CCO} = Output-side power supply;PU = Powered up (V_{CC} ≥ 3.15 V);PD = Powered down (V_{CC} ≤ 2.1V); X = Irrelevant; H = High level; L = Low level
(2) In fail-safe condition, output defaults to high level.

7.4.1 Device I/O Schematics

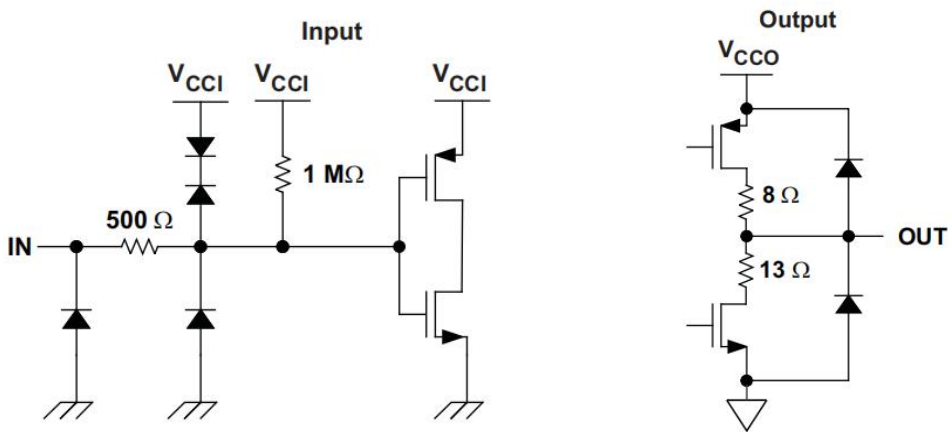


Figure 11. Device I/O Schematics

8 Application Information

XLISO742x utilize single-ended TTL-logic switching technology. Its supply voltage range is from 3.15 V to 5.25 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (i.e. µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

8.1. Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the XLISO742x only require two external bypass capacitors to operate.

8.2. Typical Application (continued)

8.2. 1 Detailed Design Procedure

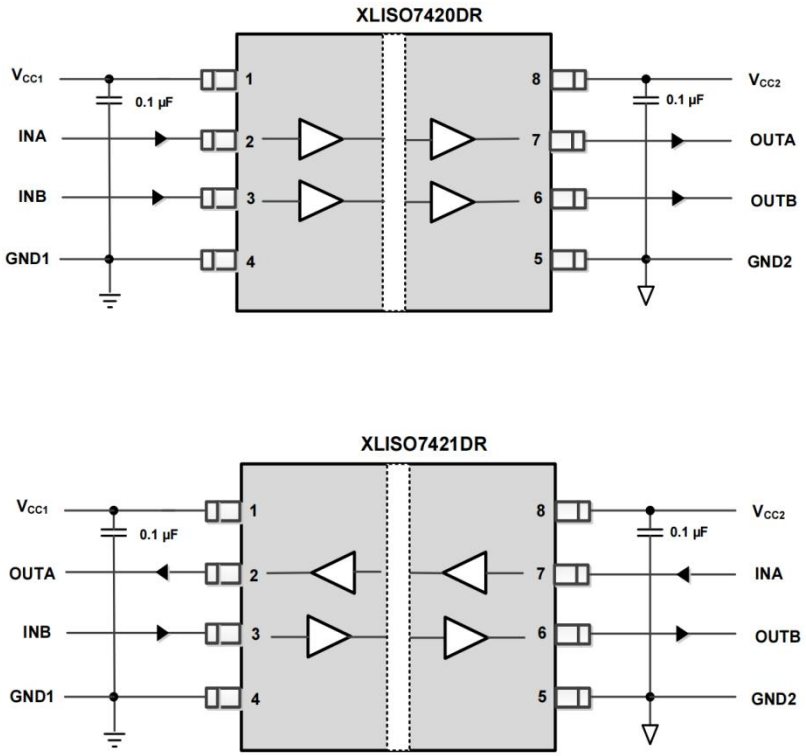


Figure 13. Typical XLISO7420DR and XLISO7421DR Circuit Hookup

8.2. 2 Application Curve

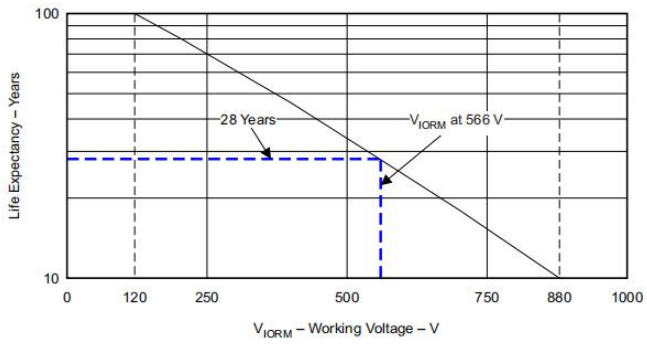


Figure 14. Life Expectancy vs Working Voltage

9 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1 µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible.

10 Layout

10.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design . Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.

- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.

- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in^2.

- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

10.2 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

10.3 Layout Example

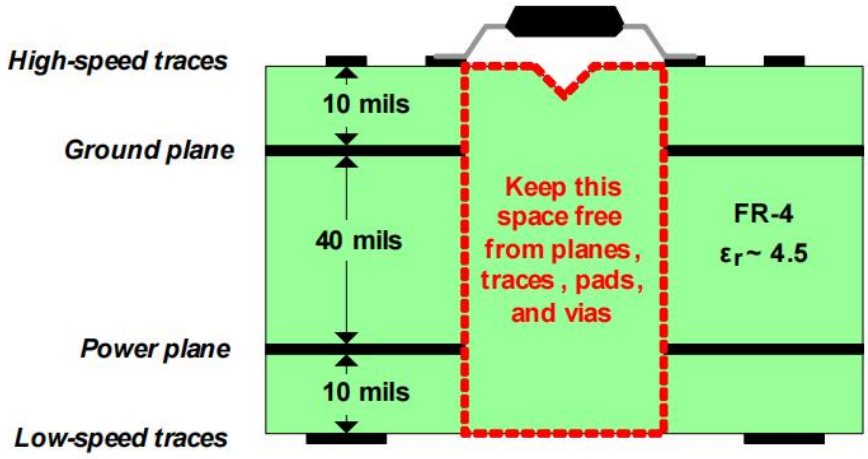


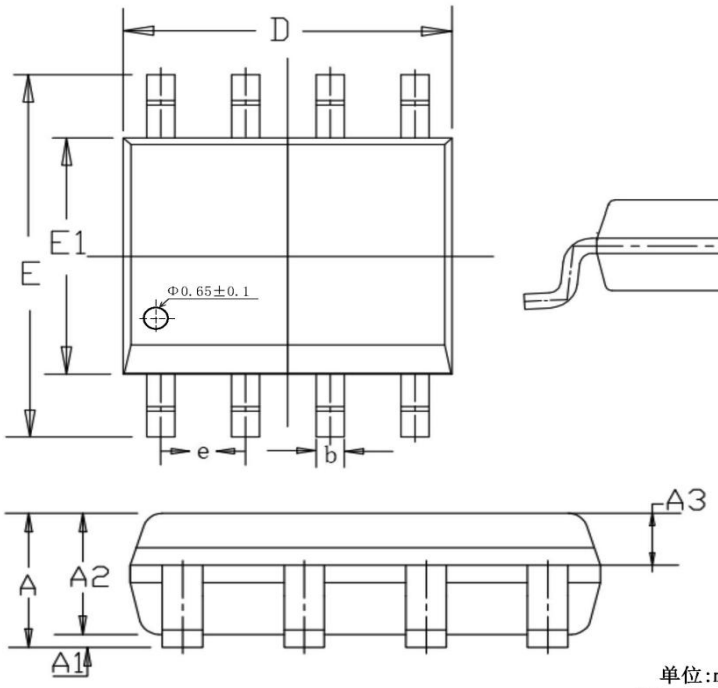
Figure 15. Recommended Layer Stack

11 ORDERING INFORMATION

Ordering Information

Part Number	Device Making	Package type	Body size (mm)	Temperate (°C)	MSL	Transpo Media	Package Quantit
XLISO7420DR	XL7420D	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLISO7420MDR	XL7420M	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLISO7421DR	XL7421D	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500

12 DIMENSIONAL DRAWINGS



单位:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1(站高)	0.100	0.150	0.200
A2(厚度)	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e(脚间距)	1.240	1.270	1.300
D(长度)	4.800	4.900	5.000
E(跨度)	5.800	6.000	6.200
E1(宽度)	3.800	3.900	4.000
L(脚长)	0.450	0.600	0.750
L1	—	0.25BSC	—

[if you need help contact us. Xinluda reserves the right to change the above information without prior notice]