1. DESCRIPTION

Family of ultra-low-power digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages when compared to legacy isolation technologies. The operating parameters of these products remain stable across wide temperature ranges and throughout device service life for ease of design and highly uniform performance. All device versions have Schmitt trigger inputs for high noise immunity and only require V_{DD} bypass capacitors.

All devices achieve worst-case propagation delays of less than 10 ns. A choice of isolation ratings (up to 2.5 kV) and a selectable fail-safe operating mode to control the default output state during power loss.

2. Applications

- Industrial automation systems
- Medical electronics
- Hybrid electric vehicles
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communication systems

3. KEY FEATURES

- No start-up initialization required
- Wide Operating Supply Voltage: 2.6 – 5.5 V
- Up to 2500 VRMS isolation
- High electromagnetic immunity
- Ultra low power (typical)

  -5 V Operation:

  < 2.6 mA/channel at 1 Mbps

  -2.70 V Operation:

  < 2.3 mA/channel at 1 Mbps
- Schmitt trigger inputs
- Selectable fail-safe mode -Default high or low output
- Precise timing (typical)

  11 ns propagation delay max

  1.5 ns pulse width distortion

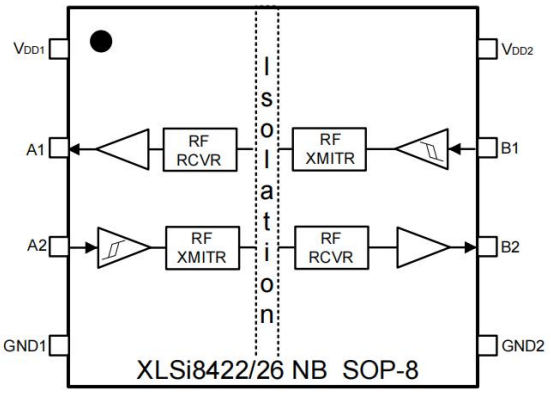
  0.5 ns channel-channel skew

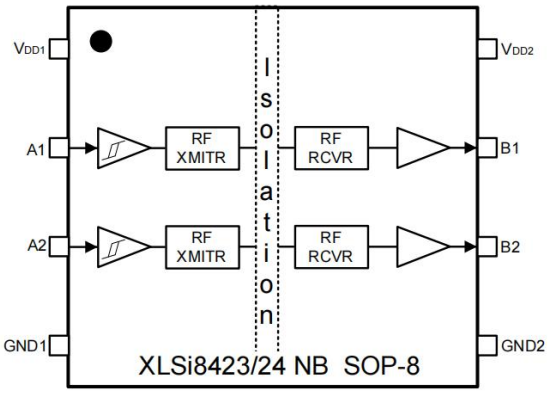
  2 ns propagation delay skew

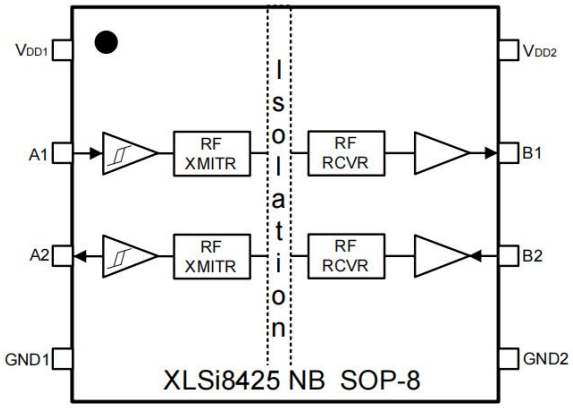
  5 ns minimum pulse width
- Transient immunity 45 kV/μs
- Wide temperature range

  –40 to 105 °C
- RoHS compliant packages

4. PIN DESCRIPTIONS







Pin Descriptions

Name	SOP-8 Pin# XLSi842x	Type	Description
V_{DD1}	1	Supply	Side 1 power supply.
GND1	4	Ground	Side 1 ground.
A1	2	Digital I/O	Side 1 digital input or output.
A2	3	Digital I/O	Side 1 digital input or output.
B1	7	Digital I/O	Side 2 digital input or output.
B2	6	Digital I/O	Side 2 digital input or output.
V_{DD2}	8	Supply	Side 2 power supply.
GND2	5	Ground	Side 2 ground.

5. FUNCTIONAL DESCRIPTION

5.1. Theory of Operation

The operation of an XLSi84xx channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single XLSi84xx channel is shown in the figure below.

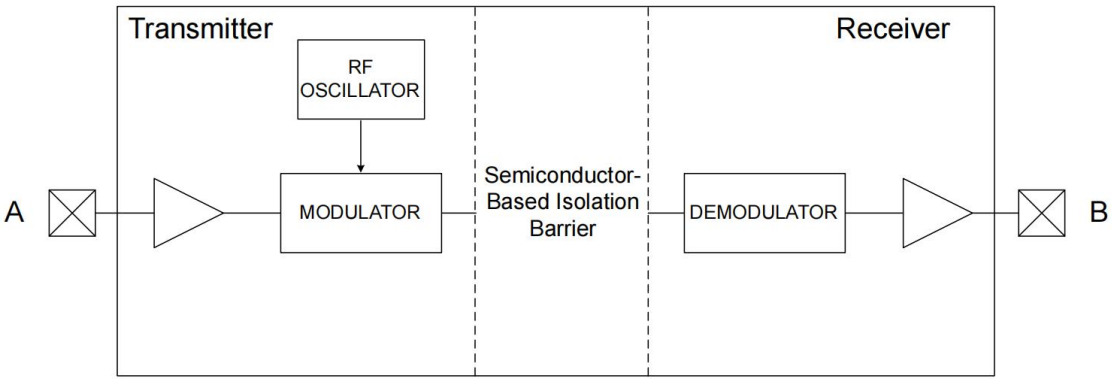


Figure 5.1. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See the figure below for more details.

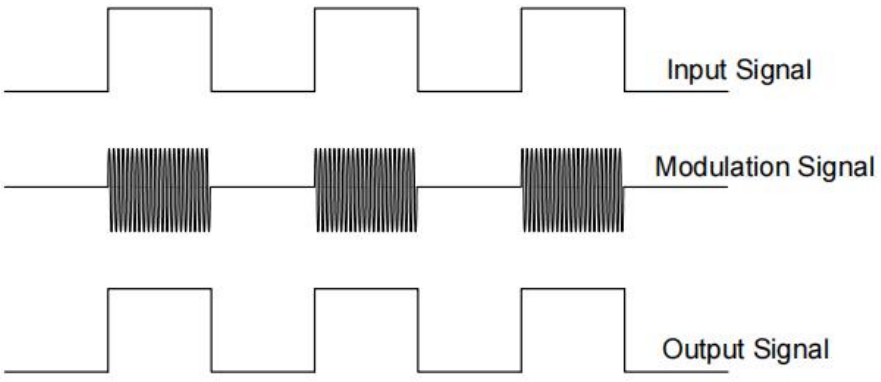


Figure 5.2. Modulation Scheme

5.2. Eye Diagram

The figure below illustrates an eye-diagram taken on an XLSi8422. For the data source, the test used an Pulse Pattern Generator set to 1000 ns/div. The output of the generator's clock and data from an XLSi8422 were captured on an oscilloscope. The results show that 2 ns pulse width distortion and 350 ps peak jitter were exhibited.

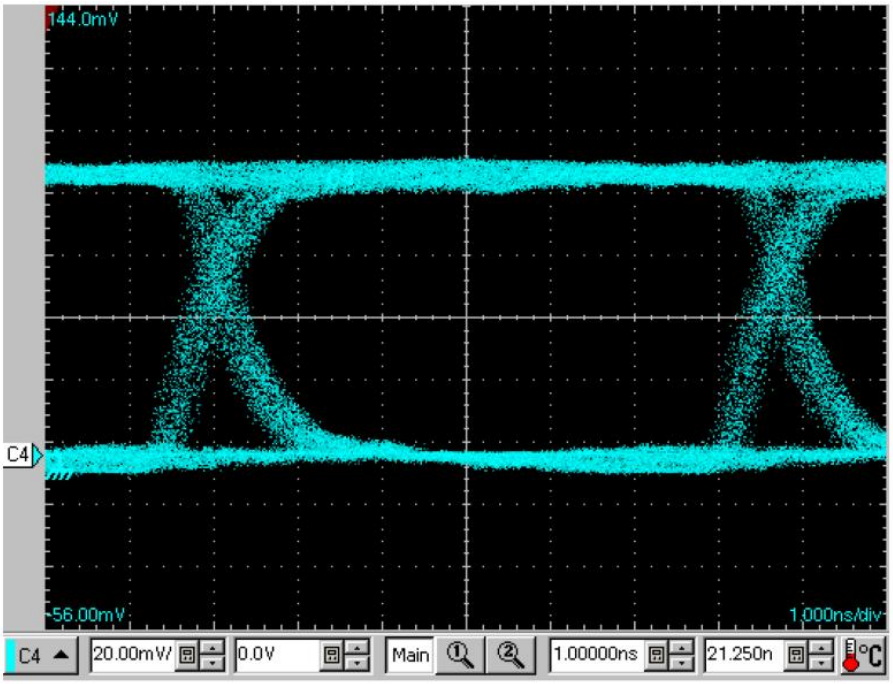


Figure 5.3. Eye Diagram

6. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Figure 6.1 Device Behavior during Normal Operation on page 7, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Refer to the table below to determine outputs when power supply (V_{DD}) is not present.

Table 6.1. XLSi84xx Logic Operation Table

V_I Input[1,4]	VDDI State[1,2,3]	VDDO State[1,2,3]	V_O Output[1,4]	Comments
H	P	P	H	Normal operation.
L	P	P	L	
X[5]	UP	P	H[6]	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X[5]	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 µs.

Notes:
1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals.
2. Powered (P) state is defined as 2.72.60 V < VDD < 5.5 V.
3. Unpowered (UP) state is defined as VDD = 0 V.
4. X = not applicable; H = Logic High; L = Logic Low.
5. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
6. This devices have default output state = H.

6.1. Device Startup

Outputs are held low during powerup until V_{DD} is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs.

6.2. Under Voltage Lockout

Under Voltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when V_{DD} is below its specified operating circuits range. Both Side A and Side B each have their own undervoltage lockout monitors. Each side can enter or exit UVLO independently. For example, Side A unconditionally enters UVLO when V_{DD1} falls below $V_{DD1(UVLO-)}$ and exits UVLO when V_{DD1} rises above $V_{DD1(UVLO+)}$. Side B operates the same as Side A with respect to its V_{DD2} supply.

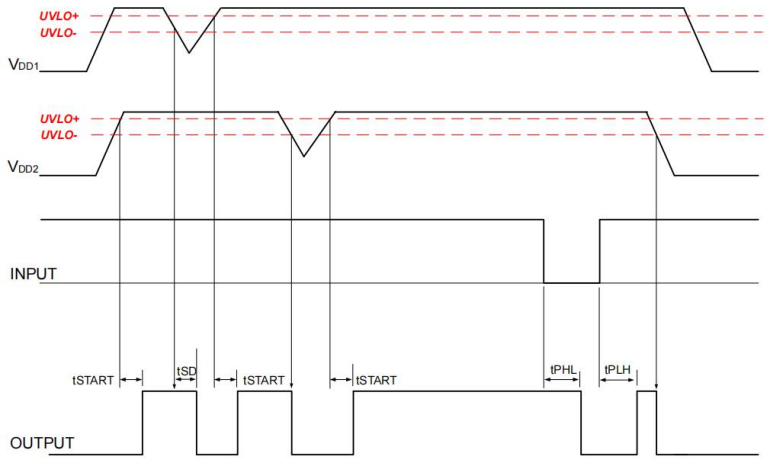


Figure 6.1. Device Behavior during Normal Operation

6.3. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 VAC) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 VAC) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection).

6.3.1. Supply Bypass

The XLSi842x family requires a 0.1 µF bypass capacitor between V_{DD1} and GND1 and V_{DD2} and GND2. The capacitor should be placed as close as possible to the package. To enhance the robustness of a design, it is further recommended that the user also add 1 µF bypass capacitors and include 100 Ω resistors in series with the inputs and outputs if the system is excessively noisy.

6.3.2. Pin Connections

No connect pins are not internally connected. They can be left floating, tied to V_{DD}, or tied to GND.

6.3.3. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

6.4. Fail-Safe Operating Mode

XLSi84xx devices feature a selectable (by ordering option) mode whereby the default output state (when the input supply is unpowered) can either be a logic high or logic low when the output supply is powered. See Table 6.1 XLSi84xx Logic Operation Table on page 6 and Section 2.

6.5. Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Table 7.2 Electrical Characteristics on page 10 through Table 7.4 Electrical Characteristics1 on page 16 for actual specification limits.

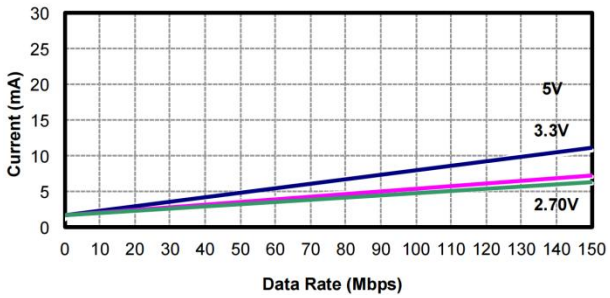


Figure 6.2. XLSi8422 Typical VDD1 or VDD2 Supply Current vs.Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

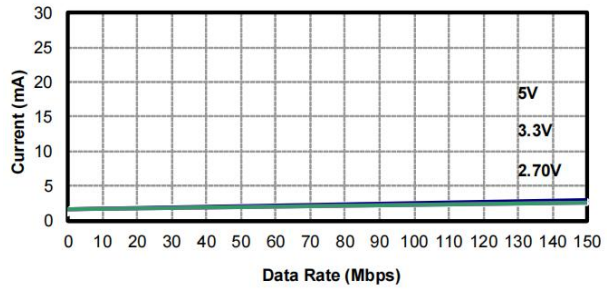


Figure 6.3. XLSi8423 Typical VDD1 Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation

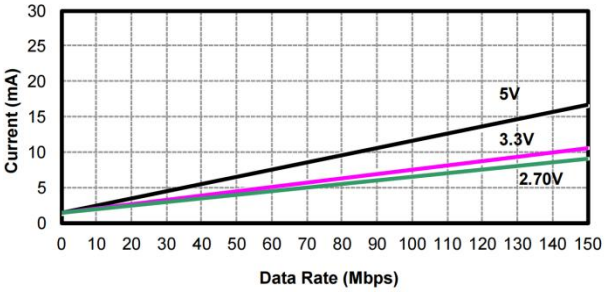


Figure 6.4. XLSi8423 Typical VDD2 Supply Current vs. Data Rate5, 3.3, and 2.70 V Operation(15 pF Load)

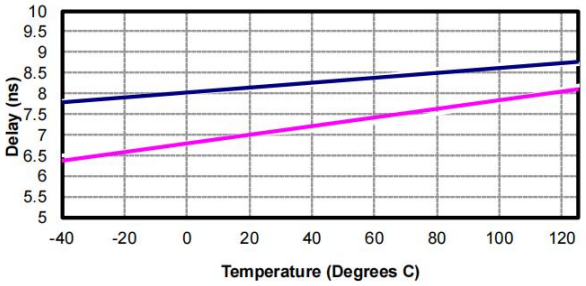


Figure 6.5. Propagation Delay vs. Temperature

7. ELECTRICAL SPECIFICATIONS

Table 7.1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature[1]	T_A	–40	25	105	C°
Supply Voltage	V_{DD1}	2.70	—	5.5	V
	V_{DD2}	2.70	—	5.5	V

Note:
1. The maximum ambient temperature is dependent upon data frequency, output loading, the number of operating channels, and supply voltage.

Table 7.2. Electrical Characteristics

(V_{DD1} = 5 V ±10%, V_{DD2} = 5 V ±10%, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	2.15	2.3	2.5	V
VDD Negative-Going Lockout Hysteresis	VDDHYS		45	75	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.6	—	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.1	—	1.4	V
Input Hysteresis	V_{HYS}		0.40	0.45	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	50	—	Ω
DC Supply Current (All inputs 0 V or at Supply)						
XLSi8422 V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 3.7 3.7 1.7 1.7	 5.6 5.6 2.6 2.6	 mA
XLSi8423 V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 5.4 1.7 1.3 1.7	 8.1 2.6 2.0 2.6	 mA

1 Mbps Supply Current (All inputs = 500 kHz square wave, C_L = 15 pF on all outputs)						
XLSi8422 V_{DD1} V_{DD2}			 — —	 2.8 2.8	 4.2 4.2	 mA
XLSi8423 V_{DD1} V_{DD2}			 — —	 3.4 1.9	 5.1 2.9	 mA
XLSi842x						
Maximum Data Rate			0	—	1.0	Mbps

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 7.1 Propagation Delay Timing on page 13	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 7.1 Propagation Delay Timing on page 13	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
XLSi842x						
Maximum Data Rate			0	—	1	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 7.1 Propagation Delay Timing on page 13	4.0	8.0	11	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 7.1 Propagation Delay Timing on page 13	—	1.5	3.0	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF	—	2.0	4.0	ns
Output Fall Time	t_f	C_L = 15 pF	—	2.0	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 5.3 Eye Diagram on page 5	—	350	—	ps
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	20	45	—	kV/µs
Start-up Time[3]	t_{SU}		—	15	40	µs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

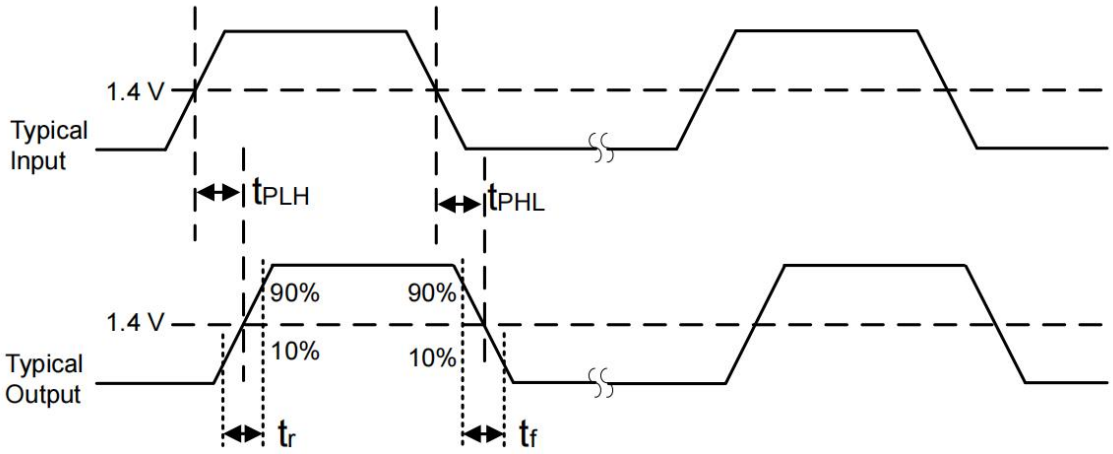


Figure 7.1. Propagation Delay Timing

Table 7.3. Electrical Characteristics

(V_{DD1} = 3.3 V ±10%, V_{DD2} = 3.3 V ±10%, T_A = –40 to 105°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	2.15	2.3	2.5	V
VDD Negative-Going Lockout Hysteresis	VDD_{HYS}		45	75	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.6	—	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.1	—	1.4	V
Input Hysteresis	V_{HYS}		0.40	0.45	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[2]	Z_O		—	50	—	Ω
DC Supply Current (All inputs 0 V or at supply)						
XLSi8422 V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 3.7 3.7 1.7 1.7	 5.6 5.6 2.6 2.6	mA
XLSi8423 V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 5.4 1.7 1.3 1.7	 8.1 2.6 2.0 2.6	mA
1 Mbps Supply Current (All inputs = 500 kHz square wave, C_L = 15 pF on all outputs)						
XLSi8422 V_{DD1} V_{DD2}			 — —	 2.8 2.8	 4.2 4.2	mA
XLSi8423 V_{DD1} V_{DD2}			 — —	 3.4 1.9	 5.1 2.9	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Timing Characteristics						
XLSi842x						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 7.1 Propagation Delay Timing on page 13	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 7.1 Propagation Delay Timing on page 13	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
XLSi842x						
Maximum Data Rate			0	—	1	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 7.1 Propagation Delay Timing on page 13	4.0	8.0	11	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 7.1 Propagation Delay Timing on page 13	—	1.5	3.0	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF	—	2.0	4.0	ns
Output Fall Time	t_f	C_L = 15 pF	—	2.0	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 5.3 Eye Diagram on page 5	—	350	—	ps
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	20	45	—	kV/µs
Start-up Time[3]	t_{SU}		—	15	40	µs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 7.4. Electrical Characteristics[1]

(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 105 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VDD Undervoltage Threshold	VDDUV+	V_{DD1}, V_{DD2} rising	2.15	2.3	2.5	V
VDD Negative-Going Lockout Hysteresis	VDD_{HYS}		45	75	95	mV
Positive-Going Input Threshold	VT+	All inputs rising	1.6	—	1.9	V
Negative-Going Input Threshold	VT–	All inputs falling	1.1	—	1.4	V
Input Hysteresis	V_{HYS}		0.40	0.45	0.50	V
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	2.3	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[2]	Z_O		—	50	—	Ω
DC Supply Current (All inputs 0 V or at supply)						
XLSi8422Ax, Bx V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 3.7 3.7 1.7 1.7	 5.6 5.6 2.6 2.6	 mA
XLSi8423Ax, Bx V_{DD1} V_{DD2} V_{DD1} V_{DD2}		 All inputs 0 DC All inputs 0 DC All inputs 1 DC All inputs 1 DC	 — — — —	 5.4 1.7 1.3 1.7	 8.1 2.6 2.0 2.6	 mA
1 Mbps Supply Current (All inputs = 500 kHz square wave, C_L = 15 pF on all outputs)						
XLSi8422 V_{DD1} V_{DD2}			 — —	 2.8 2.8	 4.2 4.2	 mA
XLSi8423 V_{DD1} V_{DD2}			 — —	 3.3 1.8	 5.0 2.8	 mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Timing Characteristics						
XLSi842x						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 7.1 Propagation Delay Timing on page 13	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 7.1 Propagation Delay Timing on page 13	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
XLSi842x						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 7.1 Propagation Delay Timing on page 13	4.0	8.0	11	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 7.1 Propagation Delay Timing on page 13	—	1.5	3.0	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.5	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF	—	2.0	4.0	ns
Output Fall Time	t_f	C_L = 15 pF	—	2.0	4.0	ns
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	See Figure 5.3 Eye Diagram on page 5	—	350	—	ps
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	20	45	—	kV/µs
Start-up Time[3]	t_{SU}		—	15	40	µs

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 5.5. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condi-tion	Value	Unit
			NB SOP-8	
Nominal Air Gap (Clearance)[1]	L(IO1)		4.9 min	mm
Nominal External Tracking (Creepage)[1]	L(IO2)		4.01 min	mm
Minimum Internal Gap (Internal Clearance)			0.008	mm
Tracking Resistance (Proof Tracking Index)	PTI		600	VRMS
Erosion Depth	ED		0.040	mm
Resistance (Input-Output)[2]	R_{IO}		10^1	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	1.0	pF
Input Capacitance[3]	C_I		4.0	pF

Notes:
1. To determine resistance and capacitance, the XLSi84xx is converted into a 2-terminal device. Pins 1–8 (1–4, NB SOP-8) are shorted together to form the first terminal and pins 5–8, NB SOP8 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 5.6. Thermal Characteristics

Parameter	Symbol	NB SOP-8	Unit
IC Junction-to-Air Thermal Resistance	θ^{JA}	140	°C/W

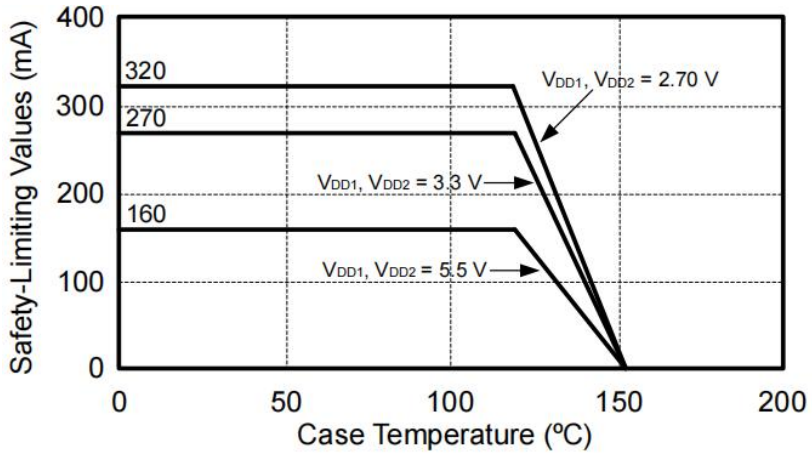


Figure 5.3. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature

Table 5.10. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature[2]	T_{STG}	–65	—	150	C°
Operating Temperature	T_A	–40	—	105	C°
Junction Temperature	T_J	—	—	150	°C
Supply Voltage	V_{DD1}, V_{DD2}	–0.5	—	6.0	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive Channel	I_O	—	—	10	mA
Lead Solder Temperature (10 s)		—	—	260	C°
Maximum Isolation Voltage (1 s) NB SOP-8		—	—	4500	V_{RMS}

Notes:
1. Permanent device damage may occur if the above absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.
2. Storage temperature from –40 to 150 °C.

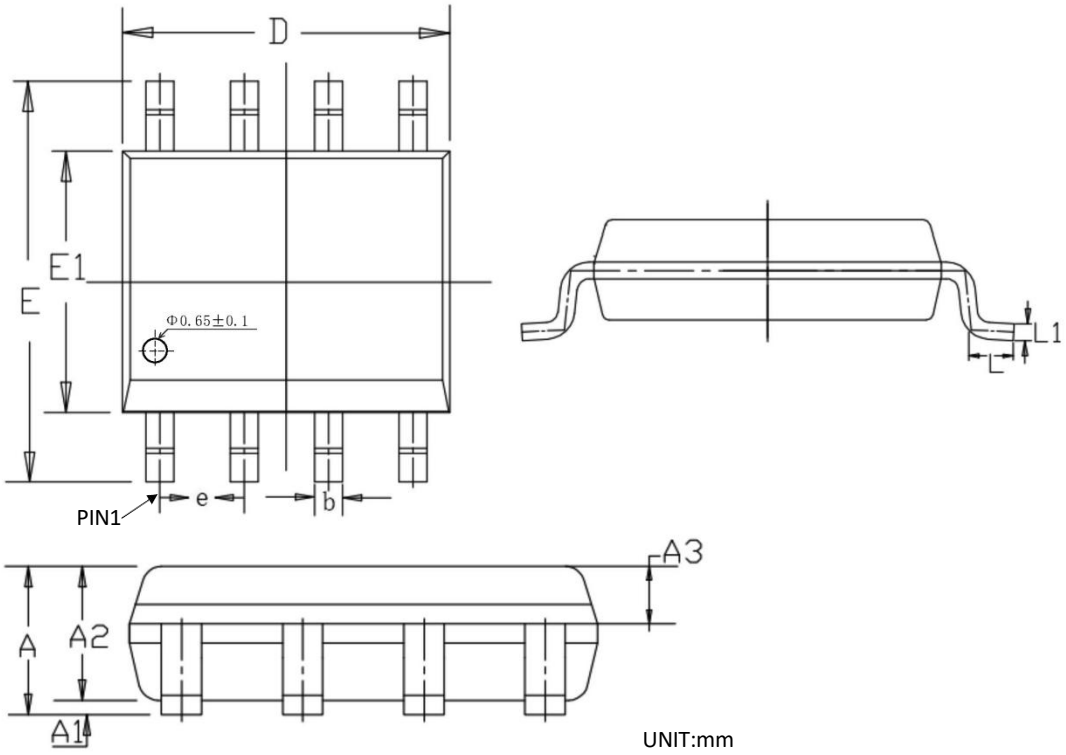
8. ORDERING INFORMATION

Ordering Information

Part Number	Device Making	Package type	Body size (mm)	Temperate (°C)	MSL	Transpo Rt	Package Quantit
XLSi8422AB-D-IS	XL8422A	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLSi8423AB-D-IS	XL8423A	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLSi8424AB-D-IS	XL8424A	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLSi8425AB-D-IS	XL8425A	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLSi8426AB-D-IS	XL8426A	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500

9. DIMENSIONAL DRAWINGS

SOP8



UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—