SK6513S High Voltage, Low Power LDO

GENERAL DESCRIPTION

The SK6513S is a high voltage, low power consumption and high performance LDO. The family uses an advanced CMOS process and a PMOSFET pass device to achieve fast start-up, with high output voltage accuracy.

The SK6513S is stable with a 1μF ~10μF ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 2% over all load, line, process, and temperature variations.

The SK6513S is available in DFN1×1-4, SOT23-3, SOT23-5, SOT89-3, and SOT89-5 package. Standard products are Pb-free and Halogen-free.

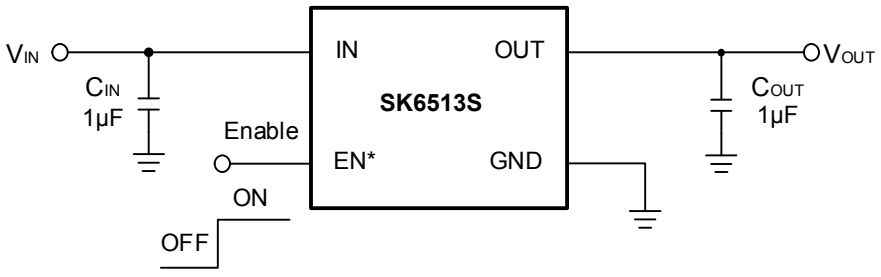
FEATURES

- Wide Input Voltage Range: 2.8~36V
- Up to 300mA Load Current
- Standard Fixed Output Voltage Options: 1.8V, 2.5V, 3.0V, 3.3V, 3.6V and 5.0V
- Other Output Voltage Options Available on Request
- Low IQ: 2.5μA
- Low Dropout Voltage: 330mV@100mA, when $V_{OUT=}$ 3.0V
- High PSRR: 60dB @1KHz
- Excellent Load/Line Transient Response

APPLICATION

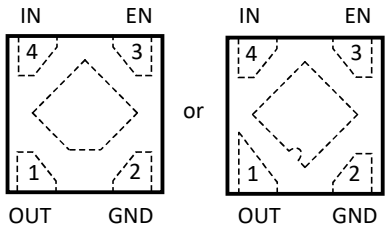
- Battery powered equipment
- Voltage regulator for LAN cards
- Wireless communication equipment
- Audio/Video equipment

TYPICAL APPLICATION CIRCUIT

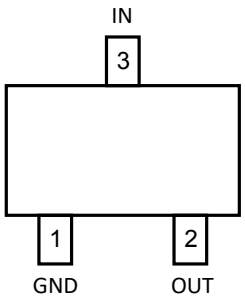


*: EN for SOT23-5, SOT89-5, and DFN1x1-4 only

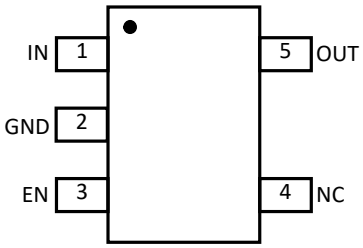
PIN CONFIGURATION (TOP VIEW)



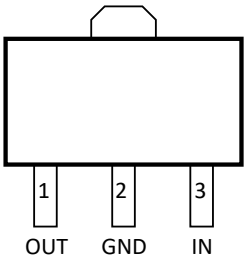
DFN1×1-4 (SK6513SD4)



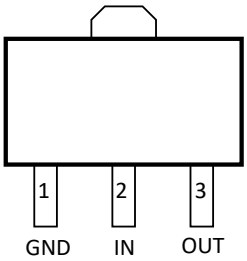
SOT23-3 (SK6513SS3)



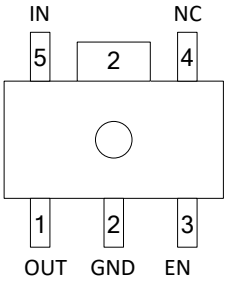
SOT23-5 (SK6513SS5E)



SOT89-3 (SK6513ST3A)



SOT89-3 (SK6513ST3B)



SOT89-5 (SK6513ST5)

PIN DESCRIPTIONS

Pin						Symbol	Description
DFN1×1-4	SOT23-3	SOT23-5	SOT89-3		SOT89-5		
(SK6513SD4-XX)	(SK6513SS3-XX)	(SK6513SS5E-XX)	(SK6513ST3A-XX)	(SK6513ST3B-XX)	(SK6513ST5-XX)		
1	2	5	1	3	1	OUT	Output pin.
2	1	2	2	1	2	GND	Ground.
3		3			3	EN	Enable control input, active high.
4	3	1	3	2	5	IN	Supply input pin.
		4			4	NC	No connection.

ORDERING INFORMATION

Part Number	Package	Tape and Reel
SK6513SD4-XX	DFN1×1-4	10000/Reel
SK6513SS3-XX	SOT23-3	3000/Reel
SK6513SS5E-XX	SOT23-5	3000/Reel
SK6513ST3A-XX	SOT89-3	1000/Reel
SK6513ST3B-XX	SOT89-3 (L-Type)	1000/Reel
SK6513ST5-XX	SOT89-5	1000/Reel

*XX: When expressed as 18, the output voltage is 1.8V; when expressed as 30 the output voltage is 3.0V.
The SK6513S devices are Pb-free and RoHS compliant.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{IN}	Input Voltage(1)	0~44	V
V_{OUT}	Output Voltage	0.8~6	V
V_{EN}	Chip Enable Input	-0.3~44	V
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55~150	°C
ESD (2)	HBM Capability	2000	V
	CDM Capability	1500	V
I_{LU} (2)	Latch up Current Maximum Rating	200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: Refer to Electrical Characteristics and Application Information for Safe Operating Area.

Note2: This device series incorporates ESD protection and is tested by the following methods:

ESD Human Body Model tested per EIA/JESD22-A114 ;

CDM tested per JESD22-C101;

Latch up Current Maximum Rating tested per JEDEC78.

THERMAL CHARACTERISTICS

Symbol	Package	Ratings	Value	Unit
$R_{\theta JA}$	SOT89-3L	Thermal Characteristics, Thermal Resistance, Junction-to-Air	135	°C/W
	SOT23-5L		250	
	SOT23-3L		360	
	DFN-4L		250	
	SOT89-5		80	
Power Dissipation @25°C	SOT89-3L	PCB board dimension : 40mm x 40mm (2layer) Copper :1OZ	0.92	W
	SOT23-5L		0.5	
	SOT23-3L		0.4	
	DFN-4L		0.5	
	SOT89-5		1.5	

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	2.8 to 36	V
I_{OUT}	Output Current	0 to 300	mA
T_A	Operating Ambient Temperature	-40 to 85	°C
C_{IN}	Effective Input Ceramic Capacitor Value	1 to 10	µF
C_{OUT}	Effective Output Ceramic Capacitor Value	1 to 10	µF
ESR	Input and Output Capacitor Equivalent Series Resistance (ESR)	5 to 100	mΩ

ELECTRICAL CHARACTERISTICS

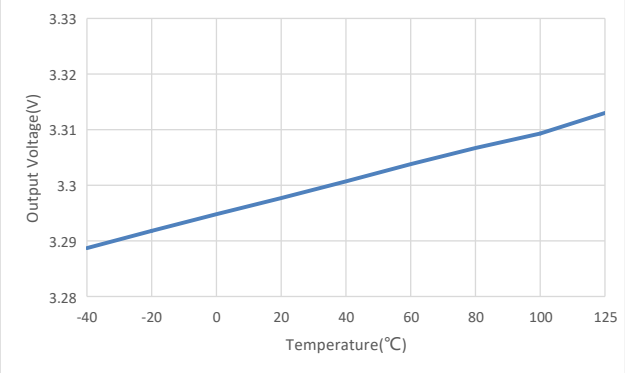
V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1.0µF, unless otherwise noted. Typical values are at T_A = +25°C.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Input Voltage	V_{IN}		2.8		36	V
Output Voltage	V_{OUT}	I_{OUT}=1mA, T_A = +25°C	-2%		+2%	V
		I_{OUT}=1mA, T_A = -40~85°C	-3%		+3%	
Line Regulation	Reg_{LINE}	2.8V ≤ V_{IN} ≤ 36V, I_{OUT} = 10mA		0.05	0.20	%/V
Dropout Voltage	V_{DROP}	V_{OUT} = 3.3V, I_{OUT} = 300mA		1	1.5	V
		V_{OUT} = 5.0V, I_{OUT} = 300mA		0.9	1.4	
Load Regulation	Reg_{LOAD}	1mA ≤ I_{OUT} ≤ 300mA, V_{IN} = V_{OUT} + 2V			40	mV
Current Limit	I_{LMT}	V_{IN} = V_{OUT} + 2V	350	450		mA
Quiescent Current	I_Q	I_{OUT} = 0mA		2.5	4.5	µA
Standby Current	I_{Q_OFF}	V_{EN} = 0V, T_A = 25°C		0.1	1	µA
EN Pin Threshold Voltage	V_{ENH}	EN Input Voltage “H”	1.4			V
EN Pin Threshold Voltage	V_{ENL}	EN Input Voltage “L”			0.3	V
EN Pin Current	I_{EN}	V_{EN} = 0V to 36V		1		µA
Power Supply Rejection Ratio	PSRR	V_{IN} = V_{OUT} + 1V, I_{OUT} = 20mA f = 1 kHz		60		dB
Output Noise Voltage	e_N	V_{IN} = V_{OUT} + 2V, I_{OUT} = 1mA f = 10Hz to 100kHz V_{OUT} = 3V, C_{OUT} = 1µF		100		μV_{RMS}
Output discharge resistance	R_{LOW}	V_{IN}=4V, EN=0V, V_{OUT}=0.5V		5		KΩ
Thermal Shutdown Temperature	T_{SD}	Temperature Increasing from T_A = +25°C		155		℃
Thermal Shutdown Hysteresis	T_{SDH}	Temperature Falling from TSD		30		℃

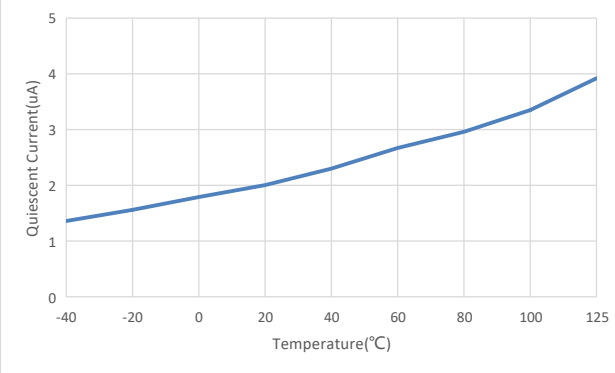
TYPICAL PERFORMANCE CHARACTERISTICS

(V_{OUT} = 3.3V, V_{IN} = V_{OUT}+2V, I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1.0μF, unless otherwise noted. Typical values are at T_A = +25°C.)

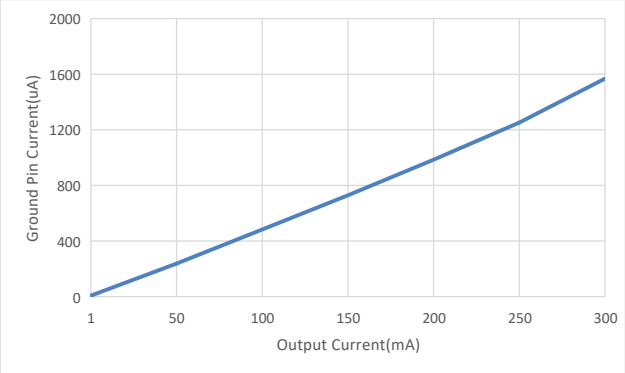
Output Voltage vs. Temperature



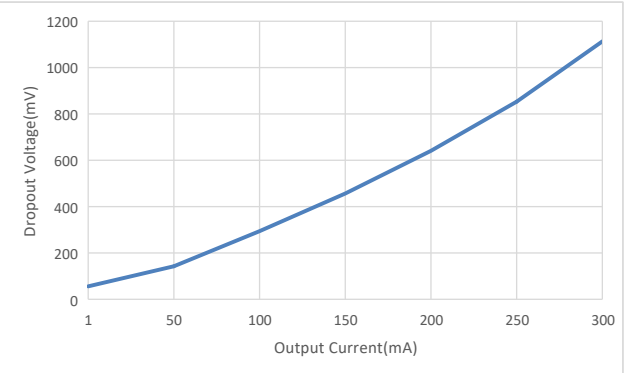
Quiescent Current vs. Temperature



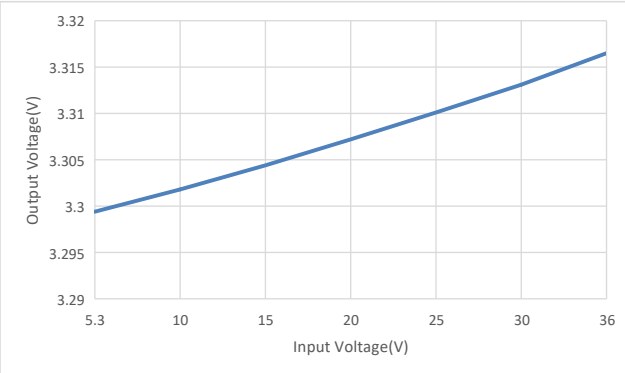
Ground Current vs. Output Current



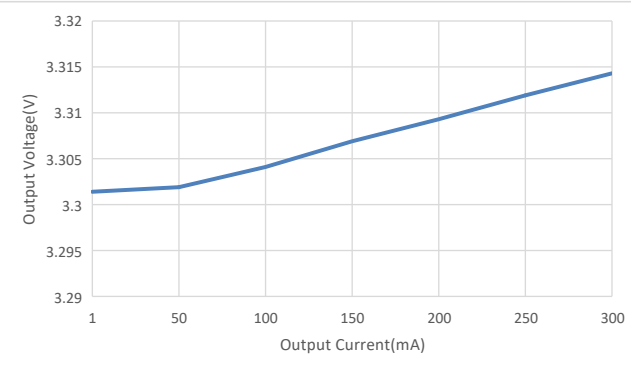
Dropout Voltage vs. Output Current



Output Voltage vs. Input Voltage

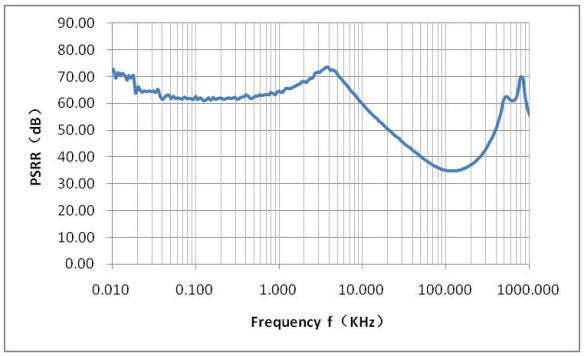


Output Voltage vs. Output Current

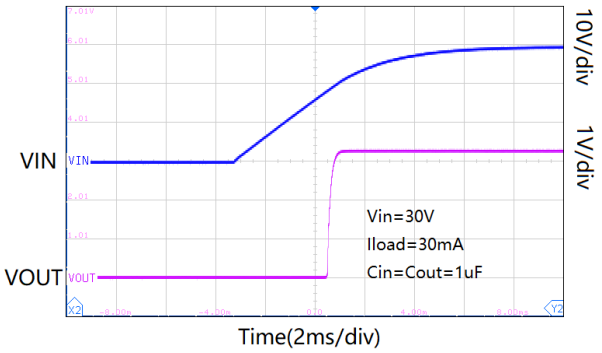


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

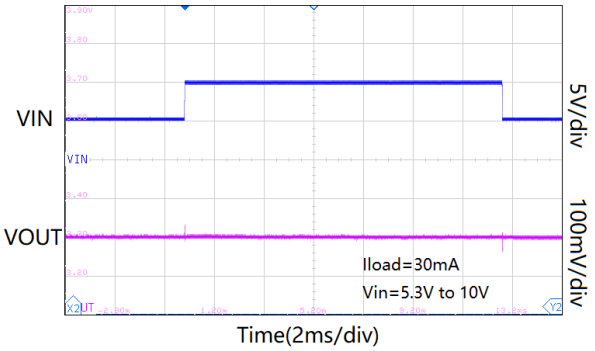
PSRR



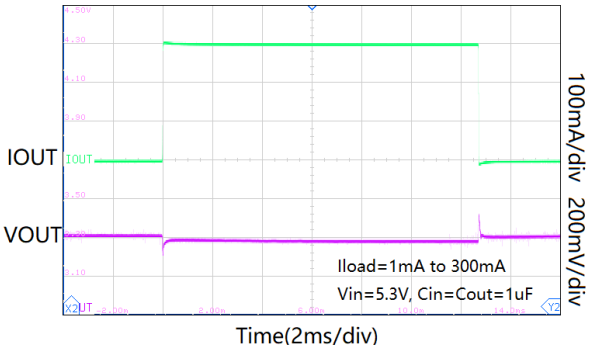
Start-up Response



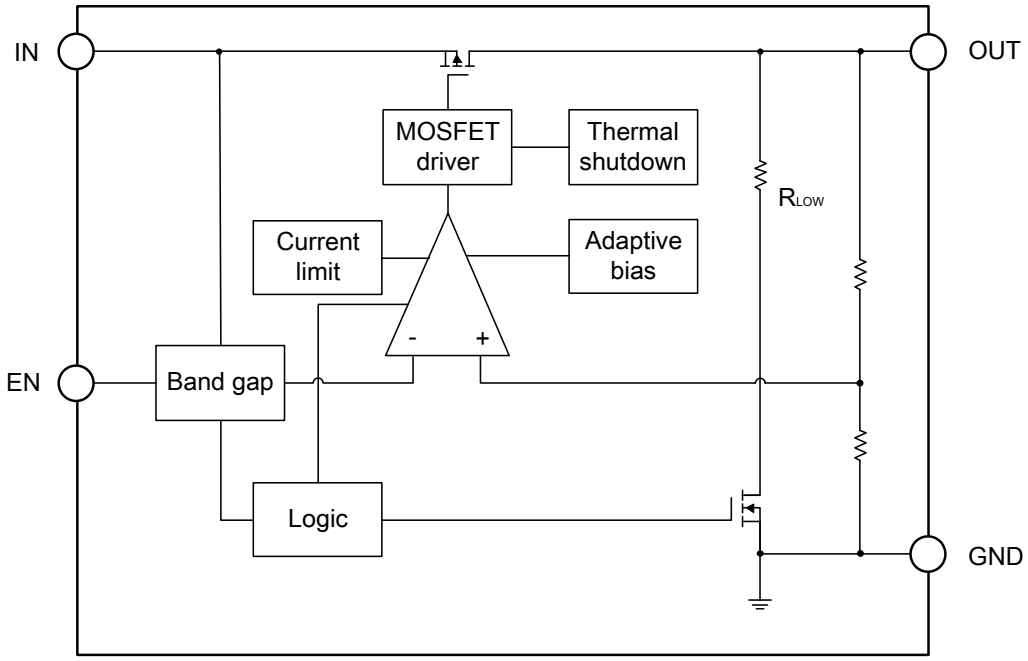
Line-Transient Response



Load-Transient Response



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Input Capacitor

A 1μF ~ 10μF ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1μF to 10μF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load / line transient response. The output capacitance may be increased to keep low undershoot / overshoot. Place output capacitor as close as possible to OUT and GND pins.

Enable

The SK6513S delivers the output power when it is set to enable state. When it works in disable state, there is no output power and the operation quiescent current is almost zero. The enable pin (EN) is active high.

Dropout Voltage

The SK6513S uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DROP}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DROP} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation.

Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 155°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 125°C, the output circuitry is again enabled.

Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating. Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} – V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$\mathbf{P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}}$$

Where,

$T_{J(MAX)}$ is the maximum junction temperature;

T_A is the ambient temperature;

θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications the maximum junction temperature is 150°C and T_A is the ambient temperature. The junction to ambient thermal resistance (θ_{JA}) is layout dependent.

For SOT89-3 package, the thermal resistance (θ_{JA}) is 135°C/W on the test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula:

$P_{D(MAX)}$ = (150°C - 25°C) / (135°C /W) = 0.925W (SOT89-3 package)

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance (θ_{JA}).

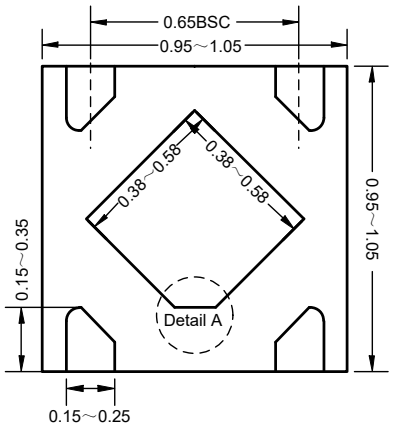
Current-Limit Protection

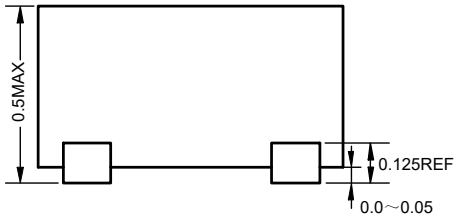
The SK6513S provides current limit function to prevent the device from damages during over-load or shorted-circuit condition. This current is detected by an internal sensing transistor.

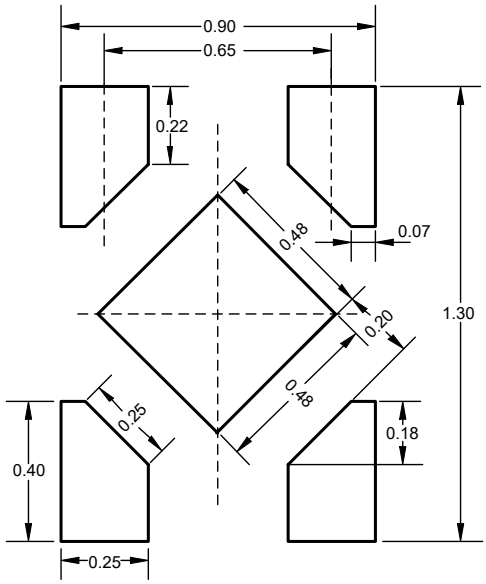
PCB LAYOUT GUIDELINES

1) Place input and output capacitors as close to the device as possible.
2) Use copper planes for device connections in order to optimize thermal performance.
3) Place thermal vias around the device to distribute heat.
4) Do not place a thermal via directly beneath the thermal pad of the DRV package. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

PACKAGE DIMENSIONS: DFN1×1-4L

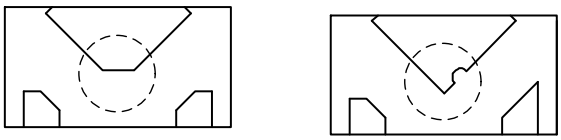






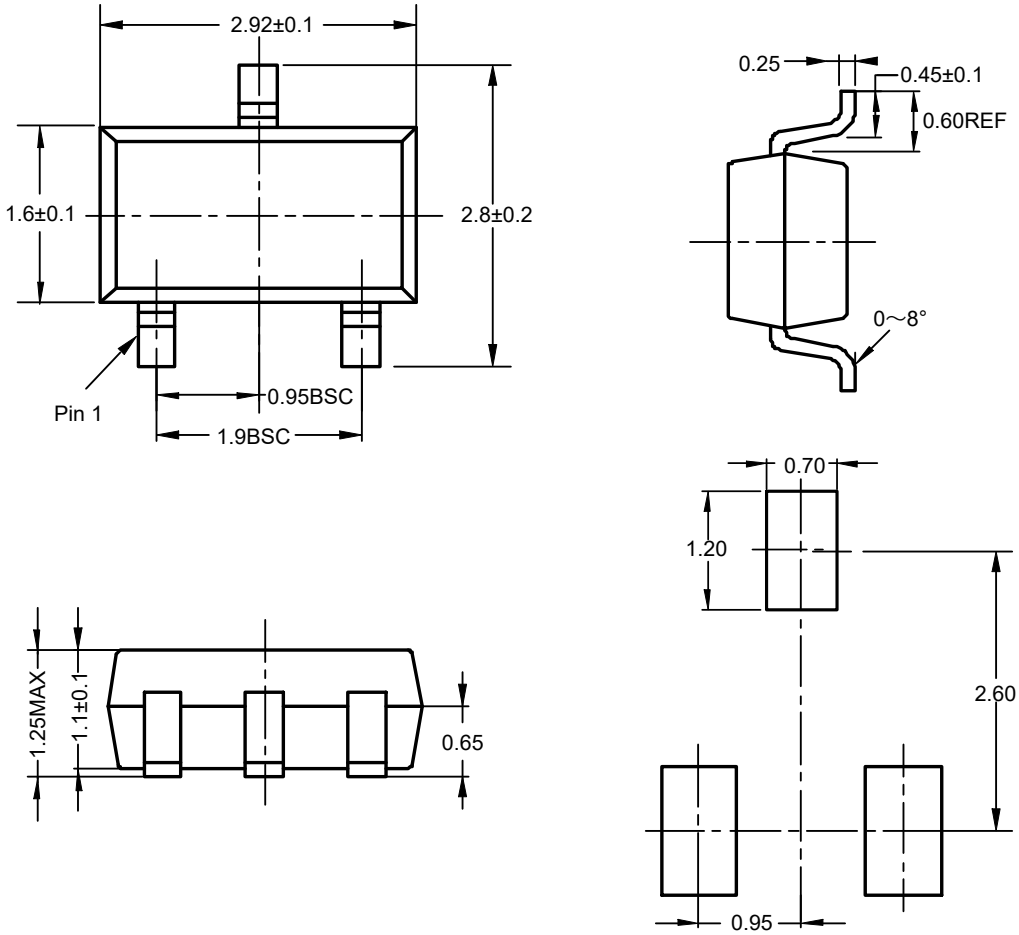
Recommended Land Pattern

Detail A: (PIN1 shape)



Unit: mm

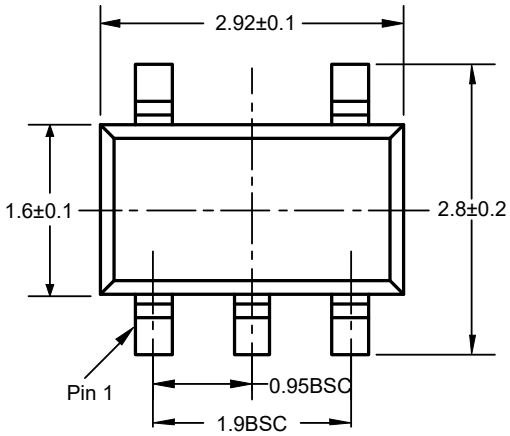
PACKAGE DIMENSIONS: SOT23-3L

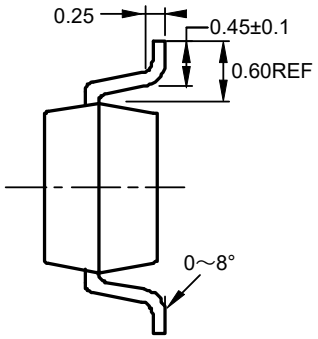


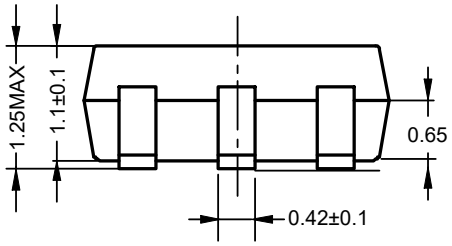
Recommended Land Pattern

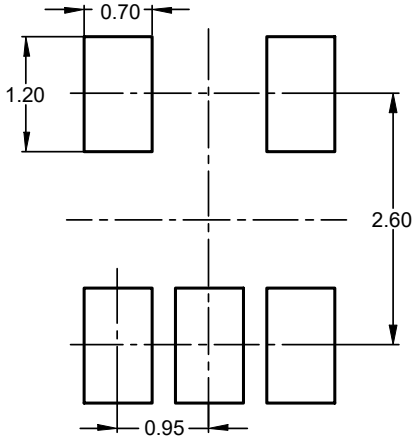
Unit: mm

PACKAGE DIMENSIONS: SOT23-5L





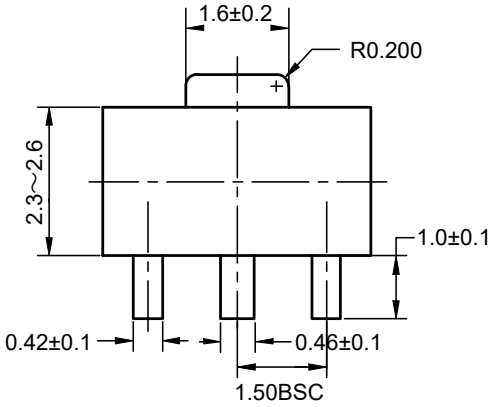




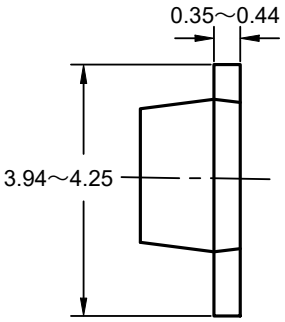
Recommended Land Pattern

Unit: mm

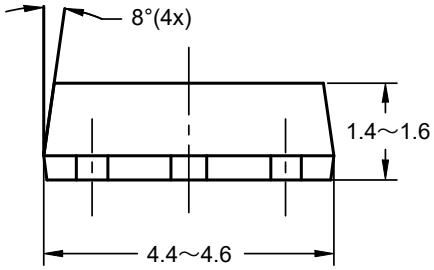
PACKAGE DIMENSIONS: SOT89-3L



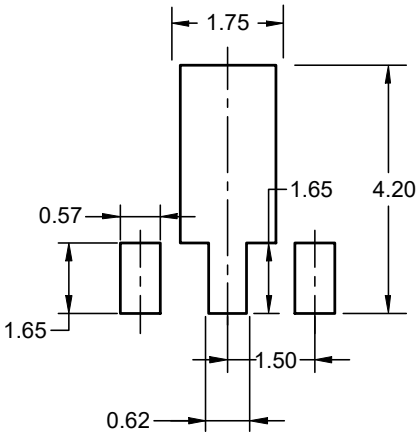
Top View



Side View



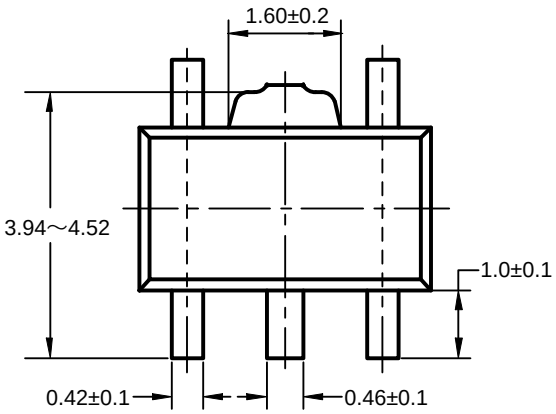
Side View



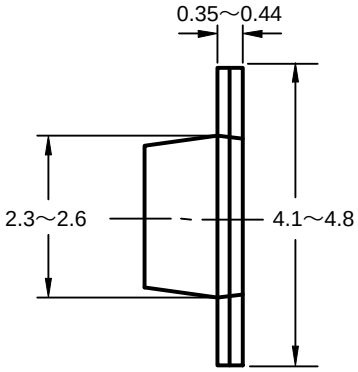
Recommended Land Pattern

Unit: mm

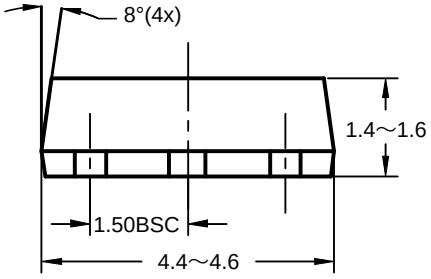
PACKAGE DIMENSIONS: SOT89-5L



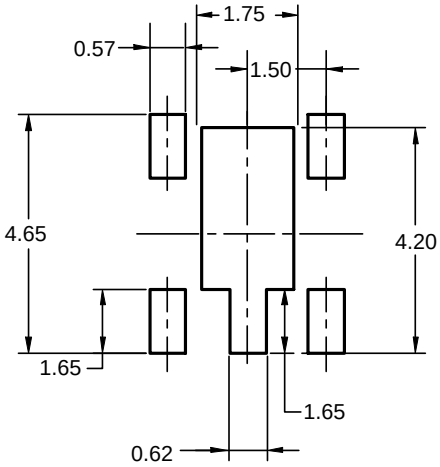
Top View



Side View



Side View



Recommended Land Pattern

Unit: mm