1. DESCRIPTION

XLISO732x provide galvanic isolation up to 3000 V_{RMS} for 1 minute per UL and 4242 V_{PK} per VDE. These devices have two isolated channels comprised of logic input and output buffers separated by silicon dioxide (SiO_2) insulation barriers. XLISO7320 has both channels in the same direction while XLISO7321 has the two channels in opposite direction. In case of input power or signal loss, default output is 'low' for devices with suffix 'F' and 'high' for devices without suffix 'F'. See Device Functional Modes for further details. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. XLISO732x have integrated noise filters for harsh industrial environment where short noise pulses may be present at the device input pins. XLISO732x have TTL input thresholds and operate from 3 V to 5.5 V supply levels. Through innovative chip design and layout techniques, electromagnetic compatibility of XLISO732x have been significantly enhanced to enable system-level ESD, EFT, Surge and Emissions compliance.

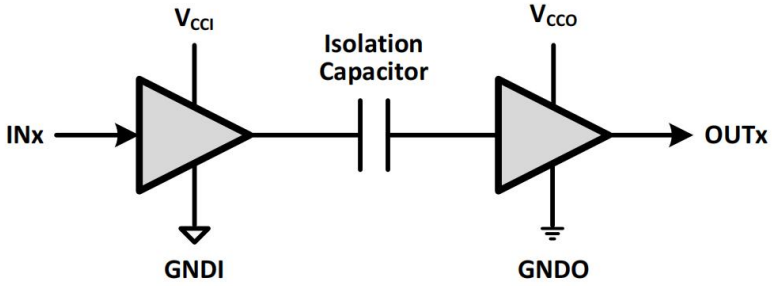
2. FEATURES

- Signaling Rate: 25 Mbps
- Integrated Noise Filter on the Inputs
- Default Output 'High' and 'Low' Options
- Low Power Consumption: Typical I_{CC} per Channel at 1 Mbps:
  - XLISO7320: 1.2 mA (5 V Supplies),
- 0.9 mA (3.3 V Supplies)
  - XLISO7321: 1.7 mA (5 V Supplies),
- 1.2 mA (3.3 V Supplies)
- Low Propagation Delay: 33 ns Typical (5V Supplies)
- 3.3 V and 5 V Level Translation
- Wide Temperature Range: –40°C to 105°C
- 65 KV/μs Transient Immunity, Typical (5V Supplies)
- Robust Electromagnetic Compatibility (EMC)
  - System-level ESD, EFT, and Surge Immunity
  - Low Emissions
- Isolation Barrier Life: > 25 Years
- Operates from 3.3 V and 5 V Supplies
- Narrow Body SOIC-8 Package

3. APPLICATIONS

- Opto-Coupler Replacement in:
  - Industrial FieldBus
  - ProfiBus
  - ModBus
  - DeviceNet™ Data Buses
  - Servo Control Interface
  - Motor Control
  - Power Supplies
  - Battery Packs

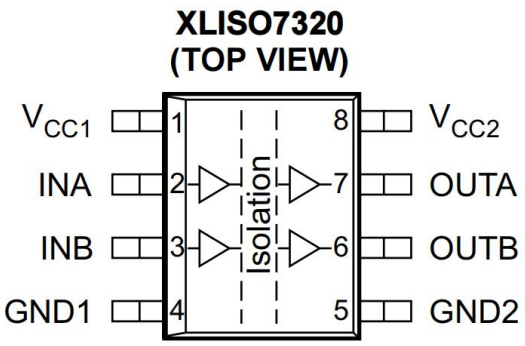
Simplified Schematic

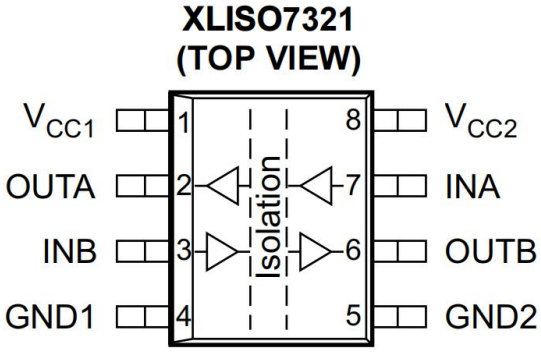


(1) V_{CCI} and GNDI are supply and ground connections respectively for the input channels.

(2) V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

4. PIN CONFIGURATION AND FUNCTIONS





Pin Functions

PIN			I/O	DESCRIPTION
NAME	XLISO7320	XLISO7321		
INA	2	7	I	Input, channel A
INB	3	3	I	Input, channel B
GND1	4	4	–	Ground connection for V_{CC1}
GND2	5	5	–	Ground connection for V_{CC2}
OUTA	7	2	O	Output, channel A
OUTB	6	6	O	Output, channel B
V_{CC1}	1	1	–	Power supply, V_{CC1}
V_{CC2}	8	8	–	Power supply, V_{CC2}

5. SPECIFICATIONS

5.1. Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC1} , V_{CC2}		-0.5	6	V
Voltage	INx, OUTx	-0.5	V_{CC}+ 0.5(3)	V
Output current, I_O			±15	mA
Junction temperature, T_J			150	℃
Storage temperature, T_{stg}		-40	150	℃

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operatingconditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

5.2. ESD Ratings

		VALUE	UNIT
V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3. Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	3		5.5	V
I_{OH}	High-level output current	-4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage	0		0.8	V
t_{ui}	Input pulse duration	40			ns
$1/t_{ui}$	Signaling rate	0		25	Mbps
T_J(1)	Junction temperature			135	℃
T_A	Ambient temperature	-40	25	105	℃

(1) To maintain the recommended operating conditions for T_J, see the Thermal Information table.

5.4. Thermal Information

THERMAL METRIC			D PACKAGE (8) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance		121	℃/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance		67.9	
$R_{\theta JB}$	Junction-to-board thermal resistance		61.6	
ψ_{JT}	Junction-to-top characterization parameter		21.5	
ψ_{JB}	Junction-to-board characterization parameter		61.1	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance		N/A	
P_D (XLISO7320)	Maximum power dissipation by XLISO7320	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 12.5 MHz 50% duty-cycle square wave	56	mW
P_{D1} (XLISO7320)	Maximum power dissipation by side-1 of XLISO7320		15	
P_{D2} (XLISO7320)	Maximum power dissipation by side-2 of XLISO7320		41	
P_D (XLISO7321)	Maximum power dissipation by XLISO7321	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 12.5 MHz 50% duty-cycle square wave	67	mW
P_{D1} (XLISO7321)	Maximum power dissipation by side-1 of XLISO7321		33.5	
P_{D2} (XLISO7321)	Maximum power dissipation by side-2 of XLISO7321		33.5	

5.5. Electrical Characteristics, 5 V

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 11		V_{CCO}(1) – 0.5	4.7		V
		I_{OH} = –20 µA; see Figure 11		V_{CCO}(1) – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 11			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 11			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				460		mV
I_{IH}	High-level input current	$I_N = V_{CC}$				10	µA
I_{IL}	Low-level input current	I_N = 0 V		-10			µA
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V; see Figure 13.		25	65		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
XLISO7320							
I_{CC1}	Supply current for I_{CC1} and I_{CC2}	DC to 1 Mbps	DC Input: $V_I = V_{CC}$ or 0 V, A_C Input: C_L = 15pF		0.4	0.9	mA
I_{CC2}					2	3.2	
I_{CC1}		10 Mbps	C_L = 15pF		0.8	1.4	
I_{CC2}					3.2	4.4	
I_{CC1}		25 Mbps	C_L = 15pF		1.4	2.3	
I_{CC2}					4.9	6.8	
XLISO7321							
I_{CC1} , I_{CC2}	Supply current for I_{CC1} and I_{CC2}	DC to 1 Mbps	DC Input: $V_I = V_{CC}$ or 0 V, A_C Input: C_L = 15pF		1.7	2.8	mA
I_{CC1} , I_{CC2}		10 Mbps	C_L = 15pF		2.5	3.7	
I_{CC1} , I_{CC2}		25 Mbps	C_L = 15pF		3.7	5.4	

(1) V_{CCO} is supply voltage, V_{CC1} or V_{CC2}, for the output channel being measured.

5.6. Electrical Characteristics, 3.3 V

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 11		V_{CCO}(1) – 0.5	3		V
		I_{OH} = –20 µA; see Figure 11		V_{CCO}(1) – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 11			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 11			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				450		mV
I_{IH}	High-level input current	$I_N = V_{CC}$				10	µA
I_{IL}	Low-level input current	I_N = 0 V		-10			µA
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V; see Figure 13.		25	50		kV/µs
SUPPLY CURRENT (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
XLISO7320							
I_{CC1}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: $V_I = V_{CC}$ or 0 V, A_C Input: C_L = 15pF		0.2	0.5	mA
I_{CC2}					1.5	2.5	
I_{CC1}		10 Mbps	C_L = 15pF		0.5	0.8	
I_{CC2}					2.2	3.2	
I_{CC1}		25 Mbps	C_L = 15pF		0.9	1.4	
I_{CC2}					3.3	4.7	
XLISO7321							
I_{CC1} , I_{CC2}	Supply current for V_{CC1} and V_{CC2}	DC to 1 Mbps	DC Input: $V_I = V_{CC}$ or 0 V, A_C Input: C_L = 15pF		1.2	2	mA
I_{CC1} , I_{CC2}		10 Mbps	C_L = 15pF		1.7	2.5	
I_{CC1} , I_{CC2}		25 Mbps	C_L = 15pF		2.5	3.6	

(1) V_{CCO} is supply voltage, V_{CC1} or V_{CC2}, for the output channel being measured.

5.7. Switching Characteristics, 5 V

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		See Figure 11	20	33	57	ns
$P_{WD(1)}$	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$					4	ns
$t_{sk(o)}$(2)	Channel-to-channel output skew time	XLISO7320				2	ns
		XLISO7321				17	
$t_{sk(pp)}$(3)	Part-to-part skew time					23	ns
t_r	Output signal rise time		See Figure 11		2.4		ns
t_f	Output signal fall time				2.1		ns
t_{fs}	Fail-safe output delay time from input power loss		See Figure 12		7.5		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.8. Switching Characteristics, 3.3 V

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		See Figure 11	22	37	66	ns
$P_{WD(1)}$	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$					3	ns
$t_{sk(o)}$(2)	Channel-to-channel output skew time	XLISO7320				3	ns
		XLISO7321				16	
$t_{sk(pp)}$(3)	Part-to-part skew time					28	ns
t_r	Output signal rise time		See Figure 11		3.1		ns
t_f	Output signal fall time				2.6		ns
t_{fs}	Fail-safe output delay time from input power loss		See Figure 12		7.4		µs

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

5.9. Typical Characteristics

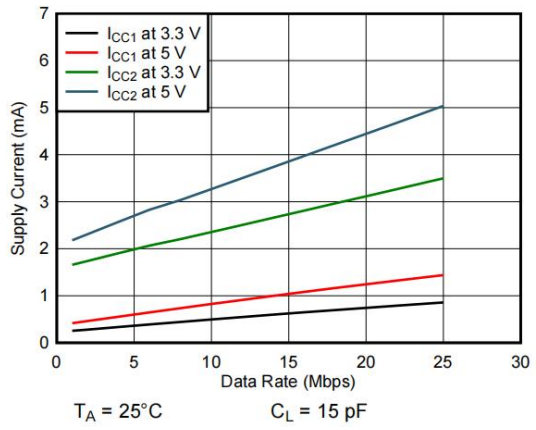


Figure 1. XLISO7320 Supply Current vs Data Rate

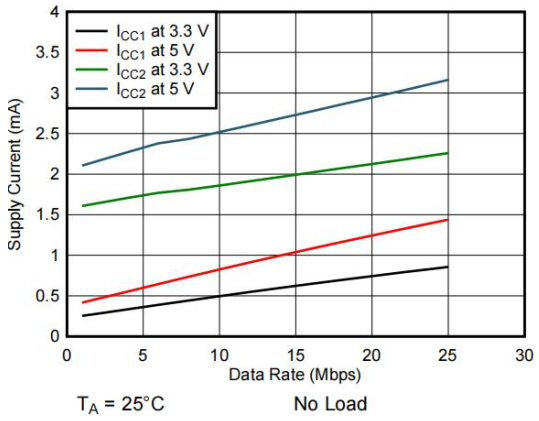


Figure 2. XLISO7320 Supply Current vs Data Rate

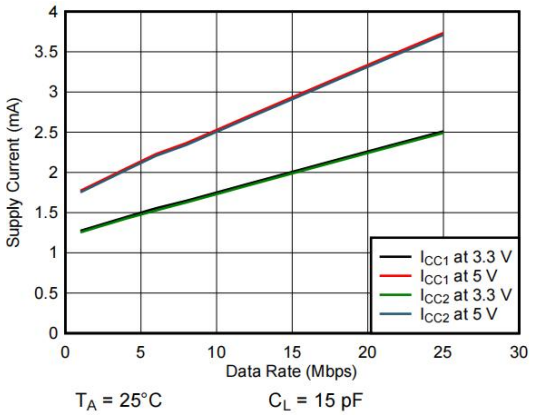


Figure 3. XLISO7321 Supply Current vs Data Rate

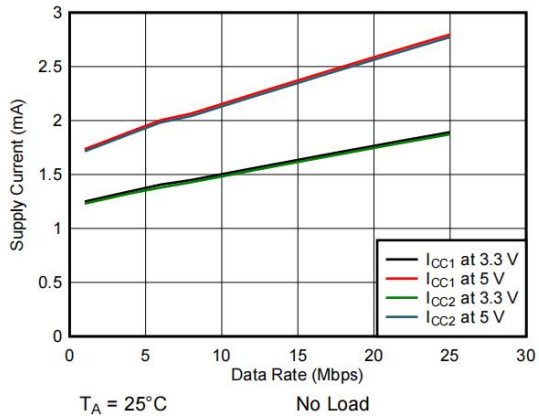


Figure 4. XLISO7321 Supply Current vs Data Rate

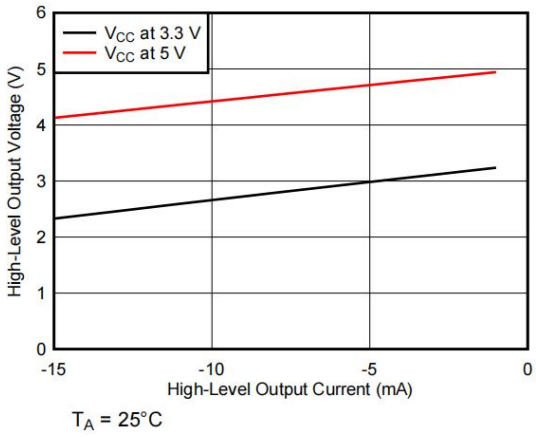


Figure 5. High-Level Output Voltage vs High-Level Output Current

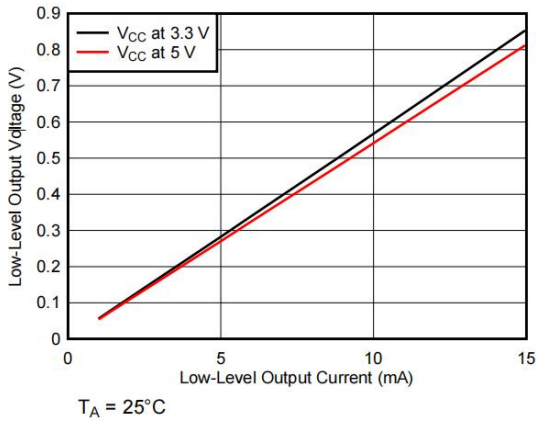


Figure 6. :Low-Level Output Voltage vs Low-Level Output Curren

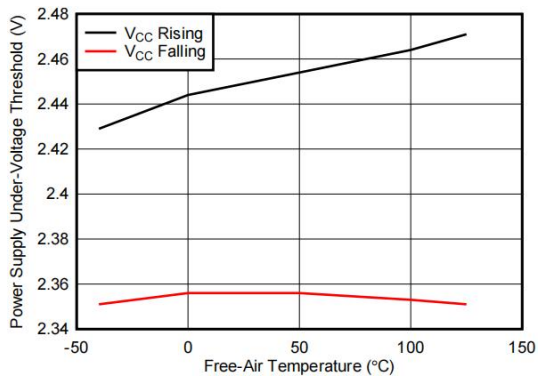


Figure 7. Power Supply Under Voltage Threshold vs Free- Air Temperature

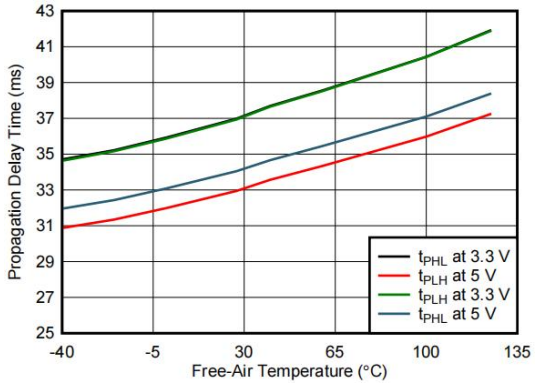


Figure 8. Propagation Delay Time vs Free-Air Temperature

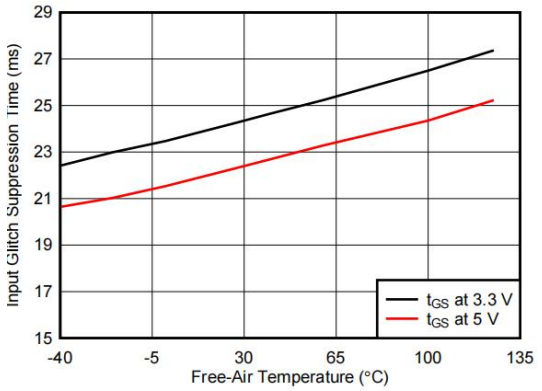


Figure 9. Input Glitch Suppression Time vs Free-Air Temperature

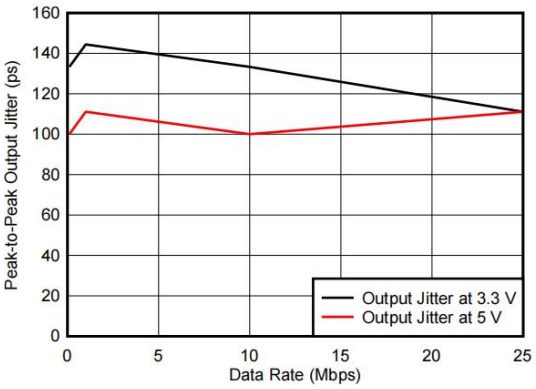
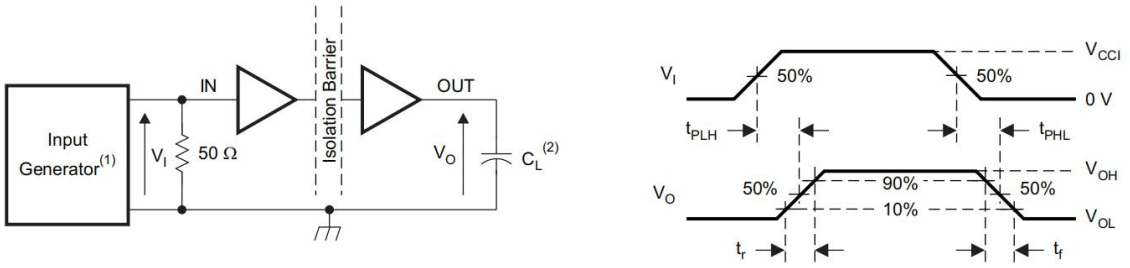


Figure 10. Peak-to-Peak Output Jitter vs Data Rate

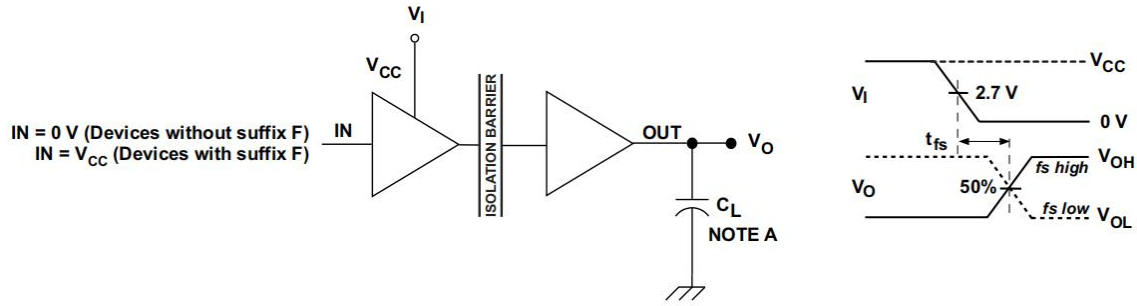
6. PARAMETER MEASUREMENT INFORMATION



(1) The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, a 50-Ω resistor is required to terminate the Input Generator signal. It is not needed in actual application.

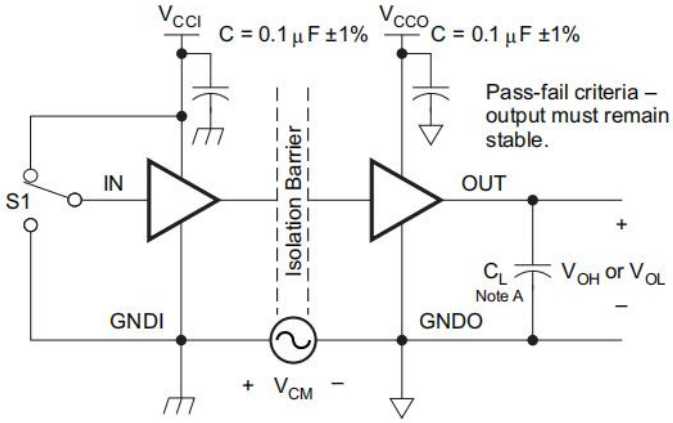
(2) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 11. Switching Characteristic Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 12. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 13. Common-Mode Transient Immunity Test Circui

7. Detailed Description

7.1. Overview

The isolator in Figure 14 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency (HF) channel with a bandwidth from 100 kbps up to 25 Mbps, and a low-frequency (LF) channel covering the range from 100 kbps down to DC.

In principle, a single-ended input signal entering the HF channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transient pulses, which then are converted into CMOS levels by a comparator. The transient pulses at the input of the comparator can be either above or below the common mode voltage VREF depending on whether the input bit transitioned from 0 to 1 or 1 to 0. The comparator threshold is adjusted based on the expected bit transition. A decision logic (DCL) at the output of the HF channel comparator measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high-frequency to the low-frequency channel.

7.2. Functional Block Diagram

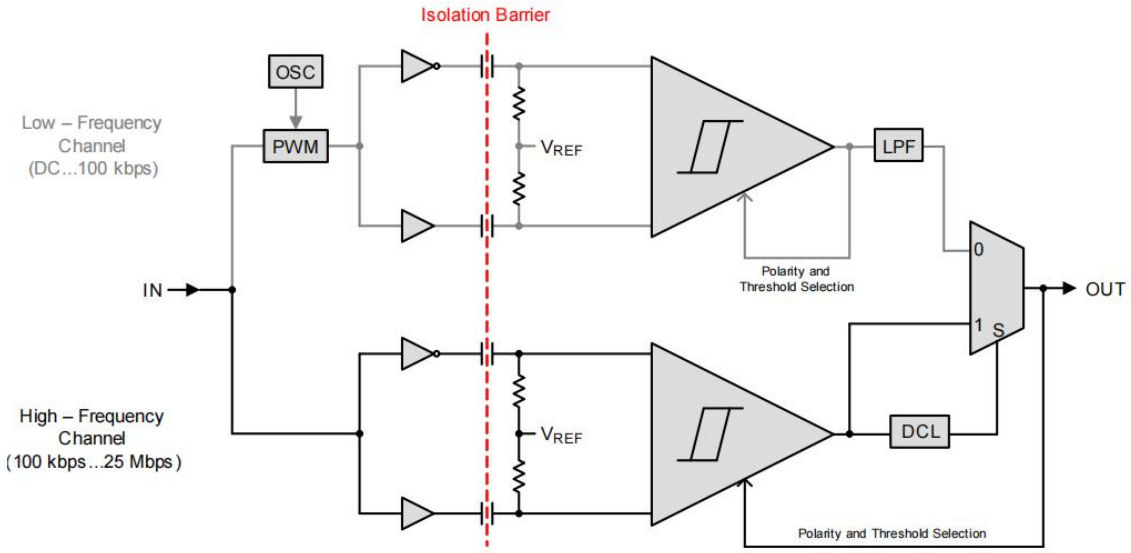


Figure 14. Conceptual Block Diagram of a Digital Capacitive Isolator

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

7.3. Feature Description.

PRODUCT	CHANNEL DIRECTION	RATED ISOLATION	MAX DATA RATE	DEFAULT OUTPUT
XLISO7320C	Same	3000 V_{RMS} / 4242 V_{PK} (1)	25 Mbps	High
XLISO7320FC				Low
XLISO7321C	Opposite			High
XLISO7321FC				Low

(1) See the Regulatory Information section for detailed Isolation Ratings

7.3.1. High Voltage Feature Description

7.3.1.1. Insulation and Safety-Related Specifications for D-8 Package

over recommended operating conditions (unless otherwise noted)

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	4			mm
L(I02)	Minimum external tracking (clearance)	Shortest terminal-to-terminal distance across the package surface	4			mm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 ; IEC 60112	400			V
DTI	Minimum internal gap (internal clearance)	Distance through insulation	13			μm
R_{IO}	Isolation resistance, input to output(1)	V_{IO} = 500 V, T_A = 25°C	10^{12}			Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 105°C	10^{11}			Ω
C_{IO}	Isolation capacitance, input to output(1)	V_{IO} = 0.4 sin (2πft), f = 1 MHz		1.5		pF
CI	Input capacitance(2)	$V_I = V_{CC}/2$ + 0.4 sin (2πft), f = 1 MHz, V_{CC} = 5 V		1.8		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

NOTE:Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to elp increase these specifications.

7.3.1.2. nsulation Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IOWM}	Maximum isolation working voltage		400	V_{RMS}
V_{IORM}	Maximum repetitive peak voltage		566	V_{PK}
V_{PR}	Input-to-output test voltage	After Input/Output safety test subgroup 2/3, V_{PR} = V_{IORM} x 1.2, t = 10 s, Partial discharge < 5 pC	680	V_{PK}
		Method a, After environmental tests subgroup 1, V_{PR} = V_{IORM} x 1.6, t = 10 s, Partial Discharge < 5 pC	906	
		Method b1,VPR = VIORM x 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC	1062	
V_{IOTM}	Maximum transient overvoltage	V_{TEST} = V_{IOTM} t = 60 sec (qualification) t = 1 sec (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	Test method per IEC 60065, 1.2/50 µs waveform, V_{TEST} = 1.3 x V_{IOSM} = 7800 V_{PK} (qualification)	6000	V_{PK}
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 3000 V_{RMS}, t = 60 sec (qualification); V_{TEST} = 1.2 x V_{ISO} = 3600 V_{RMS}, t = 1 sec (100% production)	3000	V_{RMS}
R_S	Insulation resistance	V_{IO} = 500 V at TS	>10^9	Ω
	Pollution degree		2	

Table 1. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150 VRMS	I–IV
	Rated mains voltage ≤ 300 VRMS	I–III

7.3.1.3. Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 121 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			188	mA
		$R_{\theta JA}$ = 121 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			287	
T_S	Maximum case temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the Absolut Maximun Ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Information table is that of a device installed on a High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

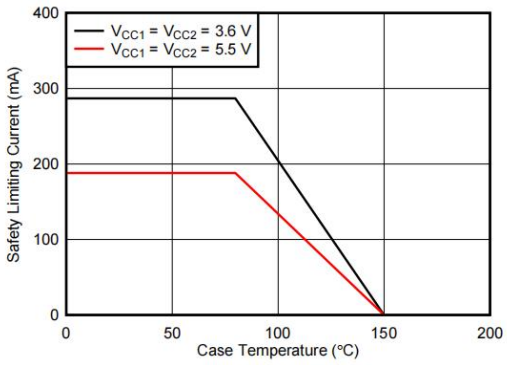


Figure 15. θ_{JC} Thermal Derating Curve

7.4. Device Functional Modes

Table 2. Function Table(1)

V_{CCI}	V_{CCO}	INA, INB	OUTA, OUTB	
			XLISO7320C, XLISO7321C	XLISO7320FC, XLISO7321FC
PU	PU	H	H	H
		L	L	L
		Open	H(2)	L(3)
PD	PU	X	H(2)	L(3)
X	PD	X	Undetermined	Undetermined

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 3 V); P_D = Powered down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High level; L = Low level; Open = Not connected

(2) In fail-safe condition, output defaults to high level

(3) In fail-safe condition, output defaults to low level

7.4.1. Device I/O Schematics

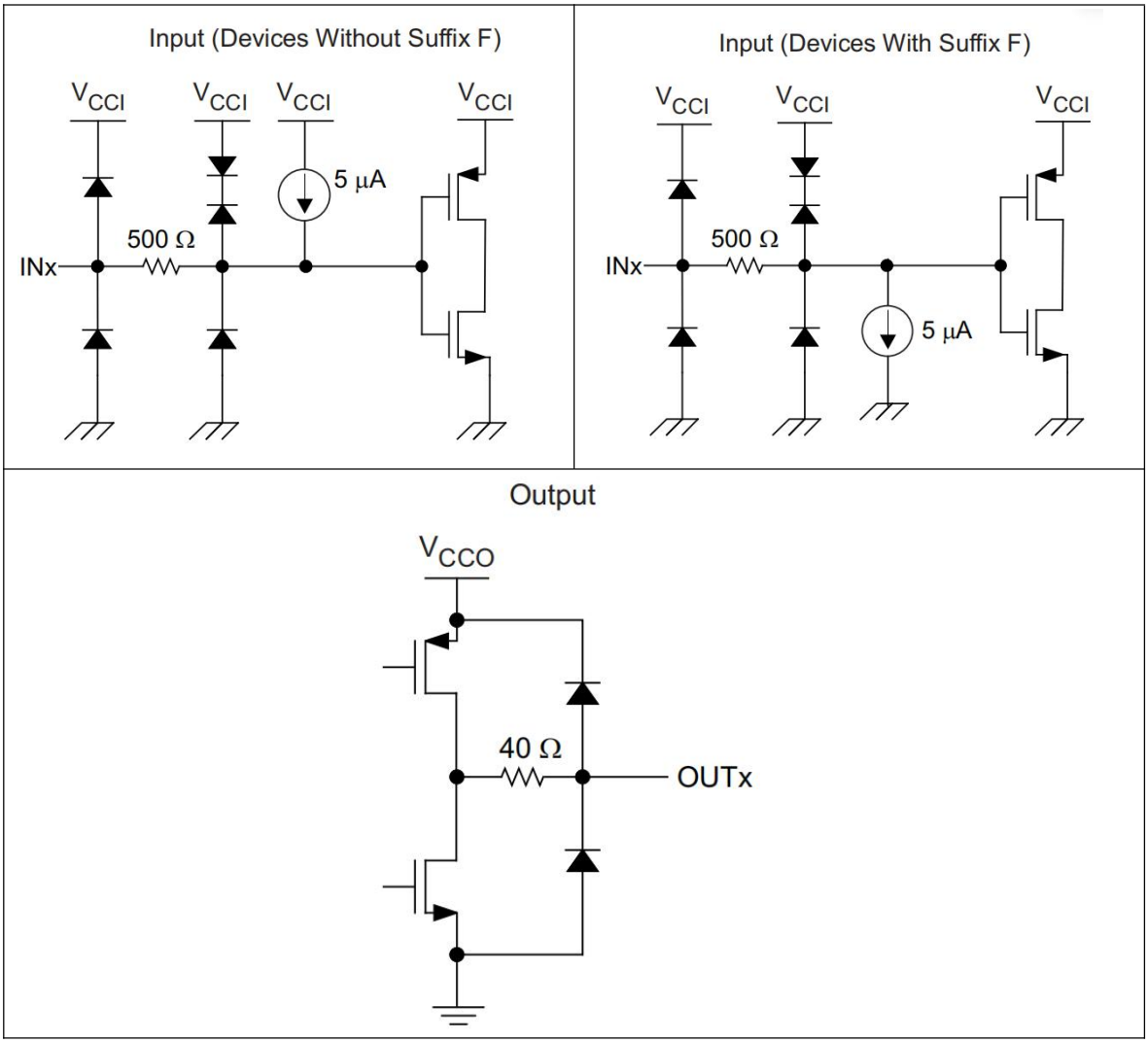


Figure 16. Device I/O Schematics

7.4.2. Design Requirements

7.4.2.1. Typical Supply Current Equations

XLISO7320:

At $V_{CC1} = V_{CC2} = 5$ V
- $I_{CC1} = 0.3838 + (0.0431 \times f)$
- $I_{CC2} = 2.74567 + (0.08433 \times f) + (0.01 \times f \times C_L)$

At $V_{CC1} = V_{CC2} = 3.3$ V
- $I_{CC1} = 0.2394 + (0.02355 \times f)$
- $I_{CC2} = 2.10681 + (0.04374 \times f) + (0.007045 \times f \times C_{L)}$

XLISO7321:

At $V_{CC1} = V_{CC2} = 5$ V
- I_{CC1} and $I_{CC2} = 1.5877 + (0.066 \times f) + (0.00123 \times f \times C_L)$

At $V_{CC1} = V_{CC2} = 3.3$ V
- I_{CC1} and $I_{CC2} = 1.187572 + (0.019399 \times f) + (0.0019029 \times f \times C_L)$

I_{CC1} and I_{CC2} are typical supply currents measured in mA, f is data rate measured in Mbps, CL is the capacitive load measured in pF.

7.4.3. Detailed Design Procedure

7.4.3.1. Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x . Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the XLISO732x incorporate many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

7.4.4. Application Performance Curves

Typical eye diagrams of XLISO732x below indicate low jitter and wide open eye at the maximum data rate of 25 Mbps.

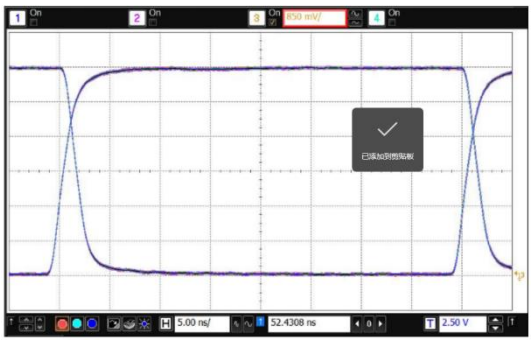


Figure 18. Eye Diagram at 25 Mbps, 5 V and 25°C

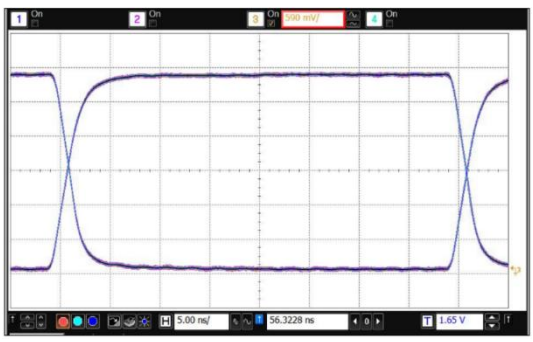


Figure 19. Eye Diagram at 25 Mbps, 3.3 V and 25°C

8. LAYOUT

8.1. PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its selfextinguishing flammability-characteristics.

8.2. Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 20). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in2 .
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

8.3. Layout Example

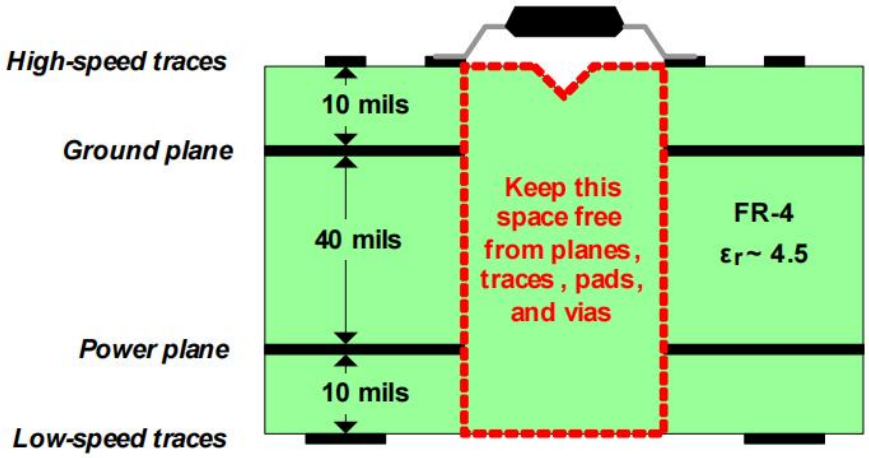


Figure 20. Recommended Layer Stack

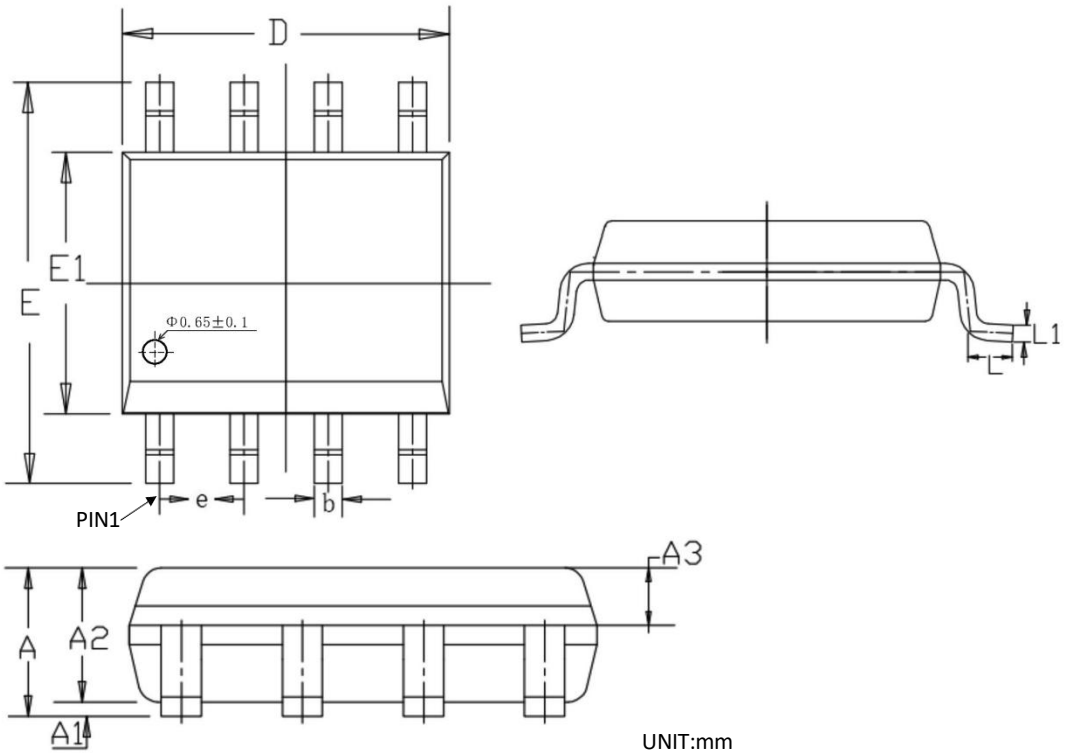
9. ORDERING INFORMATION

Ordering Information

Part Number	Device Making	Package type	Body size (mm)	Temperate (°C)	MSL	Transpo Rt	Package Quantit
XLIS07320CDR	XL7320C	SOP-8	4.90*3.90	-40to +105	MSL3	T&R	2500
XLIS07320FCDR	XL7320F	SOP-8	4.90*3.90	-40to +105	MSL3	T&R	2500
XLIS07321CDR	XL7321C	SOP-8	4.90*3.90	-40to +105	MSL3	T&R	2500
XLIS07321FCDR	XL7321F	SOP-8	4.90*3.90	-40to +105	MSL3	T&R	2500

10. DIMENSIONAL DRAWINGS

SOP8



UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—