1. DESCRIPTION

The XLADuM1280/1281/1285/1286 are dual-channel digital isolators based on XINLUDA technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives, such as optocoupler devices and other integrated couplers.

The two channels ofthe XLADuM1280/1281/1285/1286 are independent isolation channels and are available in two channel configurations with three different data rates up to 25 Mbps (see the Ordering Guide). Industrial grade models operate with the supply voltage on either side ranging from 3.135 V to 5.5 V and the automotive grades operate from 3.135 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. Unlike other optocoupler alternatives, the XLADuM1280/1281/1285/1286 isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions. When power is first applied or is not yet applied to the input side, the XLADuM1280 and XLADuM1281 have a default high output, and the XLADuM1285 and XLADuM1286 have a default low output.

2. FEATURES

- Up to 100 Mbps data rate (NRZ)
- Low propagation delay: 23 ns typical Low dynamic power consumption
- Bidirectional communication
- 3.3 V to 5 V level translation
- High temperature operation: 105°C
- High common-mode transient immunity: >25 kV/μs
- Default high output:XLADuM1280/1281
- Default low output:XLADuM1285/1286
- Narrow body, RoHS-compliant, 8-lead SOIC
- VIORM = 560 V peak
- Qualified for automotive applications

3. Applications

- General-purpose multichannel isolation
- Data converter isolation
- Industrial field bus isolation
- Hybrid electric vehicles, battery monitor, and motor drive

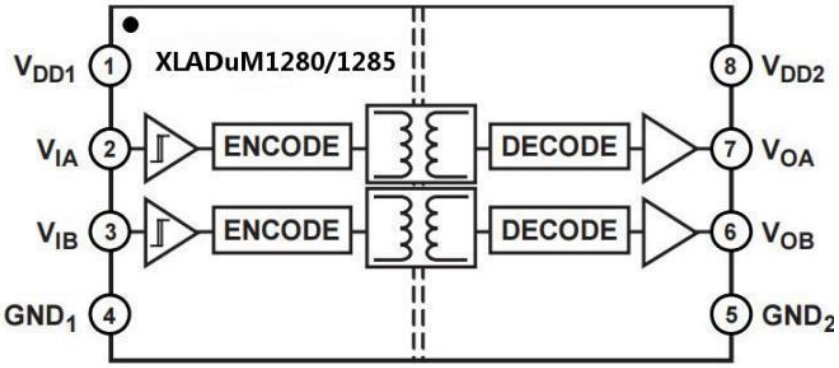


Figure 1 XLADuM1280/1285

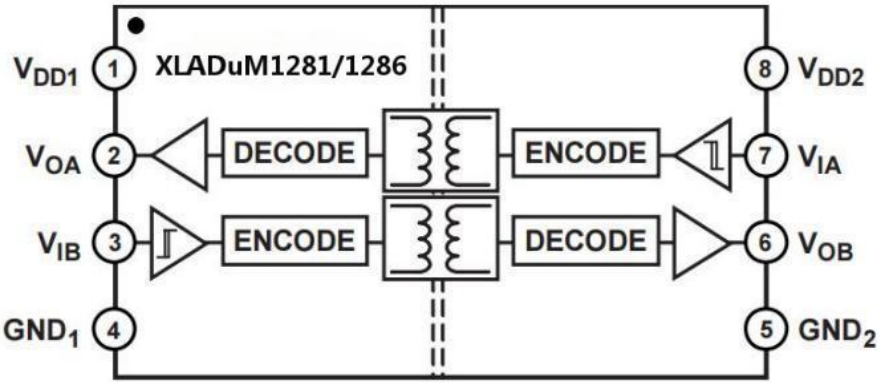


Figure 2 XLADuM1281/1286

4. SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications appl y over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, −40°C ≤ T_A ≤ 105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS s ignal levels, unless otherwise noted.

Table 1.

Parameter	Symbol	A, WA Grades			B, WB Grades			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS									
Pulse Width	PW	1000			40			ns	Within PWD limit
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			50			35	ns	50% input to 50% output
Pulse Width Distortion	PWD			10			3	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature			7			3		ps/°C	
Propagation Delay Skew	t_{PSK}			38			12	ns	Between any two units at same Operating conditions
Channel Matching [1]									
Codirectional	t_{PSKCD}			5			3	ns	
Opposing-Direction	t_{PSKOD}			10			6	ns	
Jitter			2			2		ns	

1.Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-direction channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

Table 2.

Parameter	Symbol	1 Mbps—A, B, WA, WB Grades			25 Mbps—B, WB Grades			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT									
XLADuM1280/1285	I_{DD1}		1.1	1.6		6.2	7.0	mA	No load
	I_{DD2}		2.7	4.5		4.8	7.0	mA	
XLADuM1281/1286	I_{DD1}		2.1	2.6		4.9	6.0	mA	
	I_{DD2}		2.3	2.9		4.7	6.4	mA	

Table 3. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	5.0		V	I_{OX} = −20 µA, V_{IX} = V_{IxH}
		V_{DDx} − 0.4	4.8		V	I_{OX} = −3.2 mA, V_{IX} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{OX} = 20 µA, V_{IX} = V_{IxL}
			0.2	0.4	V	I_{OX} = 3.2 mA, V_{IX} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.54	0.8	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		1.6	2.0	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.09		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.04		mA/Mbps	
Undervoltage Lockout						
Positive V_{DDx} Threshold	V_{DDxUV+}		2.75		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		2.65		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise / Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800V
Refresh Period	tr		1.6		µs	

1.|CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining Vo > 0.8 V_{DDx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at TA = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.135 V ≤ V_{DD1} ≤ 3.6 V, 3.135 V ≤ V_{DD2} ≤ 3.6 V, −40°C ≤ TA ≤ 105°C, unless otherwise noted. Switching specifications are tested with CL = 15 pF and CMOS signal levels, unless otherwise noted.

Table 4.

Parameter	Symbol	A, WA Grades			B, WB Grades			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS									
Pulse Width	PW	1000			40			ns	Within PWD limit
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			50			35	ns	50% input to 50% output
Pulse Width Distortion	PWD			10			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			7			3		ps/°C	
Propagation Delay Skew	t_{PSK}			38			16	ns	Between any two units at same Operating conditions
Channel Matching [1]									
Codirectional	t_{PSKCD}			5			3	ns	
Opposing-Direction	t_{PSKOD}			10			6	ns	
Jitter			2			2		ns	

1.Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-direction channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

Table 5.

Parameter	Symbol	1 Mbps—A, B, WA, WB Grades			25 Mbps—B, WB Grades			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT									
XLADuM1280/1285	I_{DD1}		0.75	1.4		5.1	9.0	mA	No load
	I_{DD2}		2.0	3.5		2.7	4.6	mA	
XLADuM1281/1286	I_{DD1}		1.6	2.1		3.8	5.0	mA	
	I_{DD2}		1.7	2.3		3.9	6.2	mA	

Table 6. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Input Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	3.0		V	I_{OX} = −20 µA, V_{IX} = V_{IxH}
		V_{DDx} − 0.4	2.8		V	I_{OX} = −3.2 mA, V_{IX} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{OX} = 20 µA, V_{IX} = V_{IxL}
			0.2	0.4	V	I_{OX} = 3.2 mA, V_{IX} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.6	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		1.2	1.7	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.08		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.015		mA/Mbps	
Undervoltage Lockout						
Positive V_{DDx} Threshold	V_{DDxUV+}		2.75		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		2.65		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise / Fall Time	t_R/t_F		3		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800V
Refresh Period	tr		1.6		µs	

1. |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining Vo > 0.8 V_{DDX}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3V OPERATION

All typical specifications are at TA = 25°C, V_{DD1} = 5 V, V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.135 V ≤ V_{DD2} ≤ 3.6 V; and −40°C ≤ TA ≤ 105°C, unless otherwise noted. Switching specifications are tested with CL = 15 pF and CMOS signal levels unless otherwise noted.

Table 7.

Parameter	Symbol	A, WA Grades			B, WB Grades			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS									
Pulse Width	PW	1000			40			ns	Within PWD limit
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			50			35	ns	50% input to 50% outut
Pulse Width Distortion	PWD			10			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			7			3		ps/°C	
Propagation Delay Skew	t_{PSK}			38			16	ns	Between any two units at same Operating conditions
Channel Matching [1]									
Codirectional	t_{PSKCD}			5			3	ns	
Opposing-Direction	t_{PSKOD}			10			6	ns	
Jitter			2			2		ns	

1. Codirectional channel matching is the absolute value of the difference in propagation delays betwee n any two channels with inputs on the same side of the isolation barrier. Opposingdirection channel m atching is the absolute value of the difference in propagation delays between any two channels with in putson opposing sides of the isolation barrier.

Table 8.

Parameter	Symbol	1 Mbps—A, B, WA, WB Grades			25 Mbps—B, WB Grades			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT									
XLADuM1280/1285	I_{DD1}		1.1	1.6		6.2	7.0	mA	No load
	I_{DD2}		2.0	3.5		2.7	4.6	mA	
XLADuM1281/1286	I_{DD1}		2.1	2.6		4.9	6.0	mA	
	I_{DD2}		1.7	2.3		3.9	6.2	mA	

Table 9. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Intput Threshold	V_{IH}	0.7 V_{DDx}			V	
Logic Low Intput Threshold	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{OX} = −20 µA, V_{IX} = V_{IxH}
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{OX} = −3.2 mA, V_{IX} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{OX} = 20 µA, V_{IX} = V_{IxL}
			0.2	0.4	V	I_{OX} = 3.2 mA, V_{IX} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.54	0.75	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		1.2	2.0	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.09		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.02		mA/Mbps	
Undervoltage Lockout						
Positive V_{DDx} Threshold	V_{DDxUV+}		2.75		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		2.65		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	
AC SPECIFICATIONS						
Output Rise / Fall Time	tR/tF		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDx}, VCM = 1000 V, transient magnitude = 800V
Refresh Period	tr		1.6		µs	

1. |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining Vo > 0.8 V_{DDX}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V OPERATION

All typical specifications are at TA = 25°C, V_{DD1} = 3.3 V, V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.135 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; and −40°C ≤ TA ≤ 105°C; unless otherwise noted. Switching specifications are tested with CL = 15 pF and CMOS signal levels, unless otherwise noted.

Table 10.

Parameter	Symbol	A, WA Grades			B, WB Grades			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
SWITCHING SPECIFICATIONS									
Pulse Width	PW	1000			40			ns	Within PWD limit
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			50			35	ns	50% input to 50% output
Pulse Width Distortion	PWD			10			3	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			7			3		ps/°C	
Propagation Delay Skew	t_{PSK}			38			16	ns	Between any two units at same Operating conditions
Channel Matching [1]									
Codirectional	t_{PSKCD}			5			3	ns	
Opposing-Direction	t_{PSKOD}			10			6	ns	
Jitter			2			2		ns	

1. Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-direction channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

Table 11.

Parameter	Symbol	1 Mbps—A, B, WA, WB Grades			25 Mbps—B, WB Grades			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
SUPPLY CURRENT									
XLADuM1280/1285	I_{DD1}		0.75	1.4		5.1	9.0	mA	No load
	I_{DD2}		2.7	4.5		4.8	7.0	mA	
XLADuM1281/1286	I_{DD1}		1.6	2.1		3.8	5.0	mA	
	I_{DD2}		1.7	2.3		3.9	6.2	mA	

Table 12. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Logic High Output Voltages	V_{IH}	0.7 V_{DDx}			V	
Logic Low Output Voltages	V_{IL}			0.3 V_{DDx}	V	
Logic High Output Voltages	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{OX} = −20 µA, V_{IX} = V_{IxH}
		V_{DDx} − 0.4	V_{DDx} − 0.2		V	I_{OX} = −3.2 mA, V_{IX} = V_{IxH}
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	I_{OX} = 20 µA, V_{IX} = V_{IxL}
			0.2	0.4	V	I_{OX} = 3.2 mA, V_{IX} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Input Supply Current	$I_{DDI(Q)}$		0.4	0.75	mA	
Quiescent Output Supply Current	$I_{DDO(Q)}$		1.6	2.0	mA	
Dynamic Input Supply Current	$I_{DDI(D)}$		0.08		mA/Mbps	
Dynamic Output Supply Current	$I_{DDO(D)}$		0.03		mA/Mbps	
Undervoltage Lockout						
Positive V_{DDx} Threshold	V_{DDxUV+}		2.75		V	
Negative V_{DDx} Threshold	V_{DDxUV-}		2.65		V	
V_{DDx} Hysteresis	V_{DDxUVH}		0.1		V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
AC SPECIFICATIONS						
Output Rise / Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800V
Refresh Period	tr		1.6		µs	

1. |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining Vo > 0.8 V_{DDX}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 13.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JA}		85		°C/W	Thermocouple located at center of package underside

[1] The device is considered a 2-terminal device; Pin 1 through Pin 4 are shorted together and Pin 5 through Pin 8 are shorted together.

[2] Input capacitance is from any input data pin to ground.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 14.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		3000	V rms	1-minute duration
Clearance in the Plane of the PCB	CL_{PCB}	4.5	mm min	Measured from input terminals to output terminals, shortest line of sight distance through air in theplane of the PCB
Minimum External Air Gap (Clearance)	L(I01)	4.0	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.0	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017	mm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	
Isolation Group		II		Material Group

RECOMMENDED OPERATING CONDITIONS

Table 15.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	TA	−40	+105	°C
Supply Voltages [1]	V_{DD1}, V_{DD2}			
A and B Grades		3.135	5.5	V
WA and WB Grades		3.135	5.5	V
Input Signal Rise and Fall Times			1.0	ms

[1] See theDC Correctness and Magnetic Field Immunitysection.

5. ABSOLUTE MAXIMUM RATINGS

TA = 25°C, unless otherwise noted.

Table 16.

Parameter	Rating
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +105°C
Supply Voltages (V_{DD1}, V_{DD2})	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB})	−0.5 V to V_{DDI} + 0.5 V
Output Voltages (V_{OA}, V_{OB})	−0.5 V to V_{DD2} + 0.5 V
Average Output Current per Pin[1]	
Side 1 (I_{O1})	−10 mA to +10 mA
Side 2 (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[2]	−100 kV/µs to +100 kV/µs

[1] SeeFigure 3for maximum rated current values for various temperatures.
[2] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may causelatch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD Precautions should be taken to avoid performance degradation or loss of functionality·

Table 17. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform AC Voltage, Unipolar Waveform	565	V peak	50-year minimum lifetime
Basic Insulation	1131	V peak	Maximum approved working voltage
Reinforced Insulation	560	V peak	Maximum approved working voltage
DC Voltage Basic Insulation	1131	V peak	Maximum approved working voltage
Reinforced Insulation	560	V peak	Maximum approved working voltage

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See theInsulation Lifetimesection for more details.

6. PIN CONFIGURATIONAND FUNCTION DESCRIPTIONS



Figure 4.XLADuM1280/1285Pin Configuration

Table 18.XLADuM1280/1285Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1 (3.135 V to 5.5 V).
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2 (3.135 V to 5.5 V).

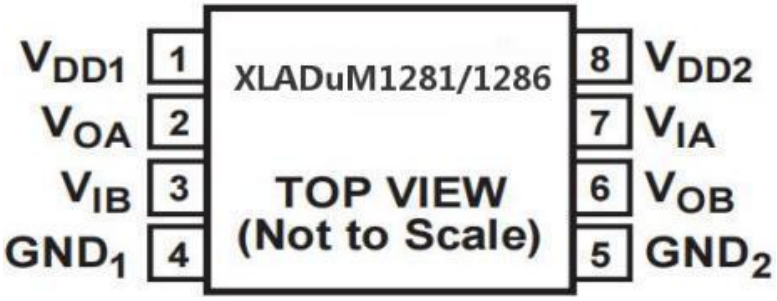


Figure 5. XLADuM1281/1286 Pin Configuration

Table 19.XLADuM1281/1286Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1 (3.135 V to 5.5 V).
2	V_{OA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{IA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2 (3.135 V to 5.5 V).

Table 20.XLADuM1280Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
L	L	Unpowered	Powered	H	H	Outputs return to the input state within 1.6 µs of VDDI power restoration.
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1.6 µs of VDDI power restoration.

Table 21.XLADuM1281Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	L	Unpowered	Powered	Indeterminate	H	Outputs return to the input state within 1.6 µs of V_{DD}I power restoration.
L	X	Powered	Unpowered	H	Indeterminate	Outputs return to the input state within 1.6 µs of VDDI power restoration.

Table 22.XLADuM1285Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
L	L	Unpowered	Powered	L	L	Outputs return to the input state within 1.6 µs of VDDI power restoration.
X	X	Powered	Unpowered	Indeterminate	Indeterminate	Outputs return to the input state within 1.6 µs of VDDI power restoration.

Table 23.XLADuM1286Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
H	H	Powered	Powered	H	H	
L	L	Powered	Powered	L	L	
H	L	Powered	Powered	H	L	
L	H	Powered	Powered	L	H	
X	L	Unpowered	Powered	Indeterminate	L	Outputs return to the input state within 1.6 µs of VDDI power restoration.
L	X	Powered	Unpowered	L	Indeterminate	Outputs return to the input state within 1.6 µs of VDDI power restoration.

7. TYPICAL PERFORMANCE CHARACTERISTICS

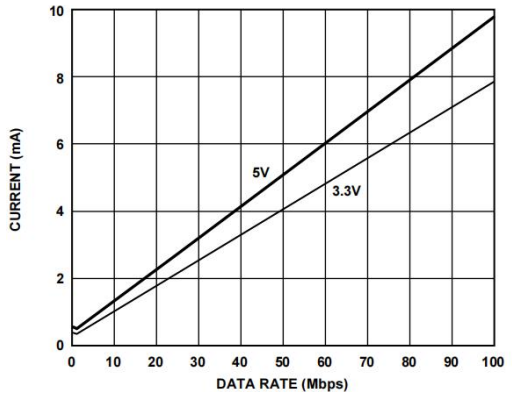


Figure 6. Typical Supply Current per Input Channel vs. Data Rate for 5 V and 3.3 V Operation

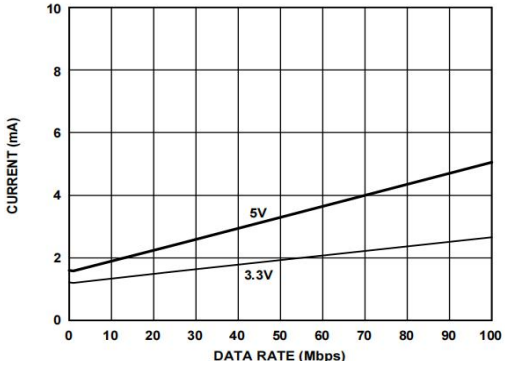


Figure 7. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3.3 V Operation (No Output Load)

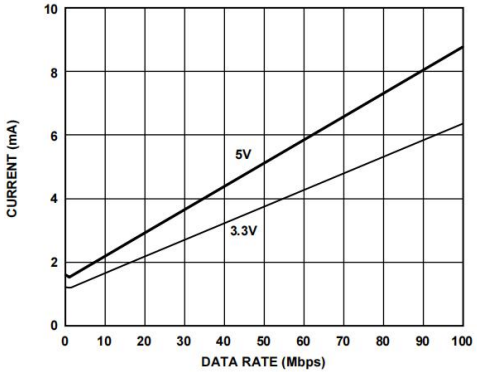


Figure 8. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3.3 V Operation (15 pF Output Load)

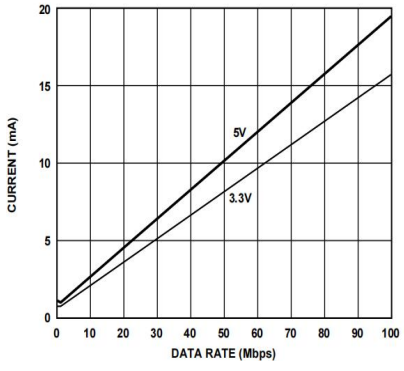


Figure 9. Typical XLADuM1280 or XLADuM1285 V_{DD1} Supply Current vs.Data Rate for 5 V and 3.3 V Operation

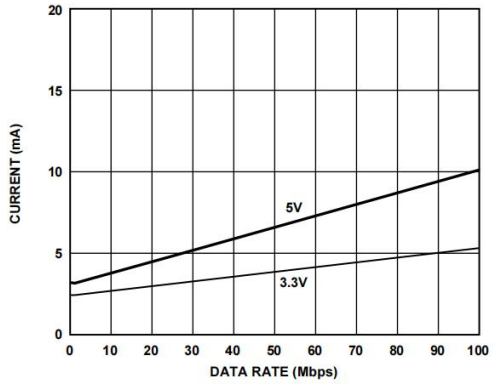


Figure 10. Typical XLADuM1280 or XLADuM1285 V_{DD2} Supply Current vs. Data Rate for 5 V and 3.3 V Operation

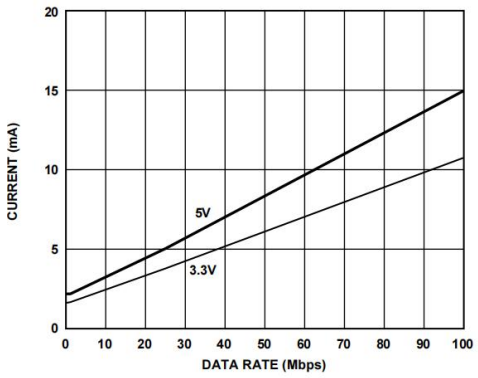


Figure 11. Typical XLADuM1281 or XLADuM1286 V_{DD1} or V_{DD2} Supply Current vs.Data Rate for 5 V and 3.3 V Operation

8. APPLICATIONS INFORMATION

PRINTED CIRCUIT BOARD LAYOUT

The XLADuM1280/1281/1285/1286 digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at both input and output supply pins V_{DD1} and V_{DD2} (seeFigure 12). The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The input-to-output propagation delay time for a high-to-low transition may differ from the propagation delay time of a low-to-high transition.

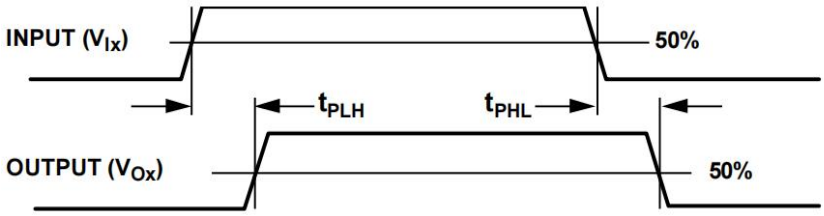


Figure 12. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single XLADuM1280/1281/1285/1286 component. Propagation delay skew refers to the maximum amount the propagation delay differs between multiple XLADuM1280/1281/1285/1286components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent via the transformer to the decoder. The decoder is bistable and is, therefore, either set or reset by the pulses indicating input logic transitions. In the absence of logic transitions at the input for more than ~1.6 µs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output.

If the decoder receives no pulses for more than about 6.4 µs, the input side is assumed tobe unpowered or nonfunctional, in which case, the isolator output is forced to a default low state by the watchdog timer circuit.

The limitation on the device's magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines such conditions. The XLADuM1280 is examined in a 3.3 V operating condition because it represents the most susceptible mode of operation of this product.

The pulses at the transformer output have an amplitude greater than 1.5 V. The decoder has a sensing threshold of about 1.0 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\pi r_n^2; \; n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density.
r_n is the radius of the n^{th} turn in the receiving coil.
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the XLADuM1280 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 13.

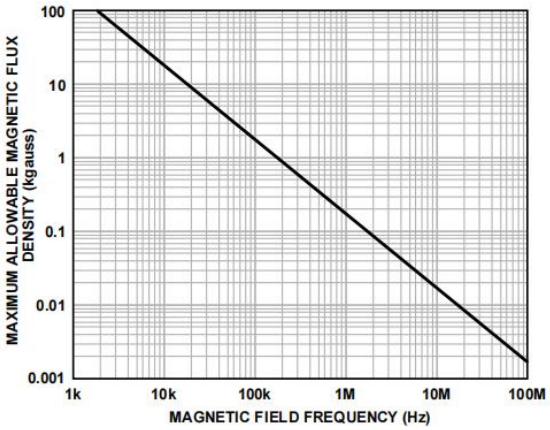


Figure 13. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.08 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. If such an event occurs, with the worst-case polarity, during a transmitted pulse, it would reduce the received pulse from >1.0 V to 0.75 V.

This is still well above the 0.5 V sensing threshold of the decoder. The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the XLADuM1280 transformers.Figure 14 expresses these allowable current magnitudes as a function of frequency for selected distances. The XLADuM1280 is very insensitive to external fields. Only extremely large, high frequency currents, very close to the component could potentially be a concern. For the 1 MHz example noted, place a 0.2 kA current 5 mm away from the XLADuM1280 to affect component operation.

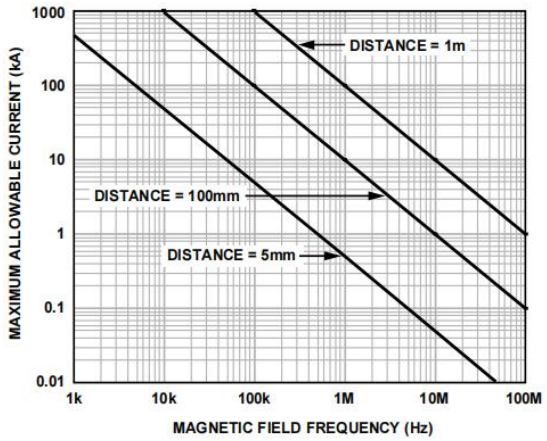


Figure 14. Maximum Allowable Current for Various Current to XLADuM1280 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Take care to avoid PCB structures that form loops.

POWER CONSUMPTION

The supply current at a given channel of the XLADuM1280/ 1281/1285/1286 isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.For each in put channel,

the supply current is given by

$I_{DDI} = I_{DDI(Q)}$ $f \leq 0.5fr$

$I_{DDI} = I_{DDI(D)} \times (2f - fr) + I_{DDI(Q)}$ $f > 0.5fr$

For each output channel, the supply current is given by

$I_{DDO} = I_{DDO(Q)}$ $f \leq 0.5fr$

$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10-3) \times CL \times V_{DDO}) \times (2f - fr) + I_{DDO(Q)}$ $f > 0.5fr$

where: $I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

CL is the output load capacitance (pF)

V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz); it is half the input data rate, expressed in units of Mbps.

fr is the input stage refresh rate (Mbps) = 1/tr (μs).

$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

supply currents (mA).

To calculate the total V_{DD1} and V_{DD2} supply current, the supply currents for each input and output channel corresponding to V_{DD1} and V_{DD2} are calculated and totaled.Figure 6 and Figure 7 show per-channel supply currents as a function of data rate for an unloaded output condition.Figure 8 shows the per-channel supply current as a function of data rate for a 15 pF output condition.Figure 9 through Figure 11 show the total VDD1 and VDD2 supply current as a function of data rate for XLADuM1280/1281channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, XINLUDA carries out an extensive set of evaluations to determine the lifetime of the insulation structure with in the XLADuM1280/1281/ 1285/1286.

XINLUDA performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 17 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition.

The insulation lifetime of the XLADuM1280/1281/1285/1286depends on the voltage waveform typ e imposed across the isolation barrier. The iCoupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac,or dc.Figure 15, Figure 16, and Figure 17 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the XINLUDA recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed inTable 17 can be applied while maintaining the 50-year minimum lifetime provided the voltage conforms to either the unipolar ac or dc voltage case. Any cross-insulation voltage waveform that does not conform to Figure 16 or Figure 17 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 17.

Note that the voltage presented in Figure 17 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

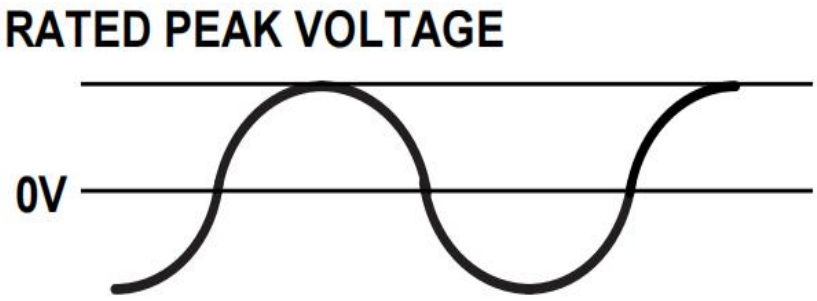


Figure 15. Bipolar AC Waveform

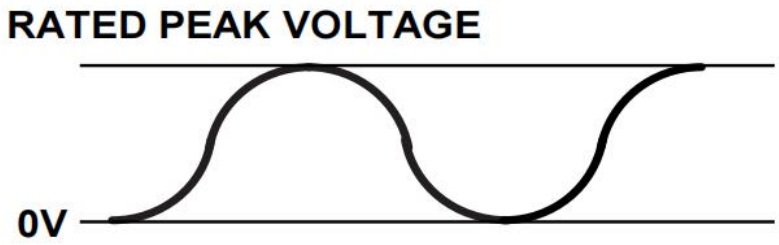


Figure 16. Unipolar AC Waveform

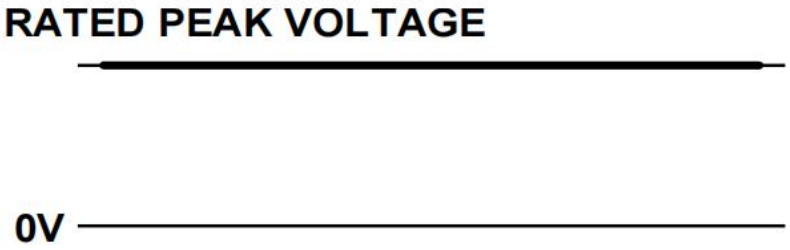


Figure 17. DC Waveform

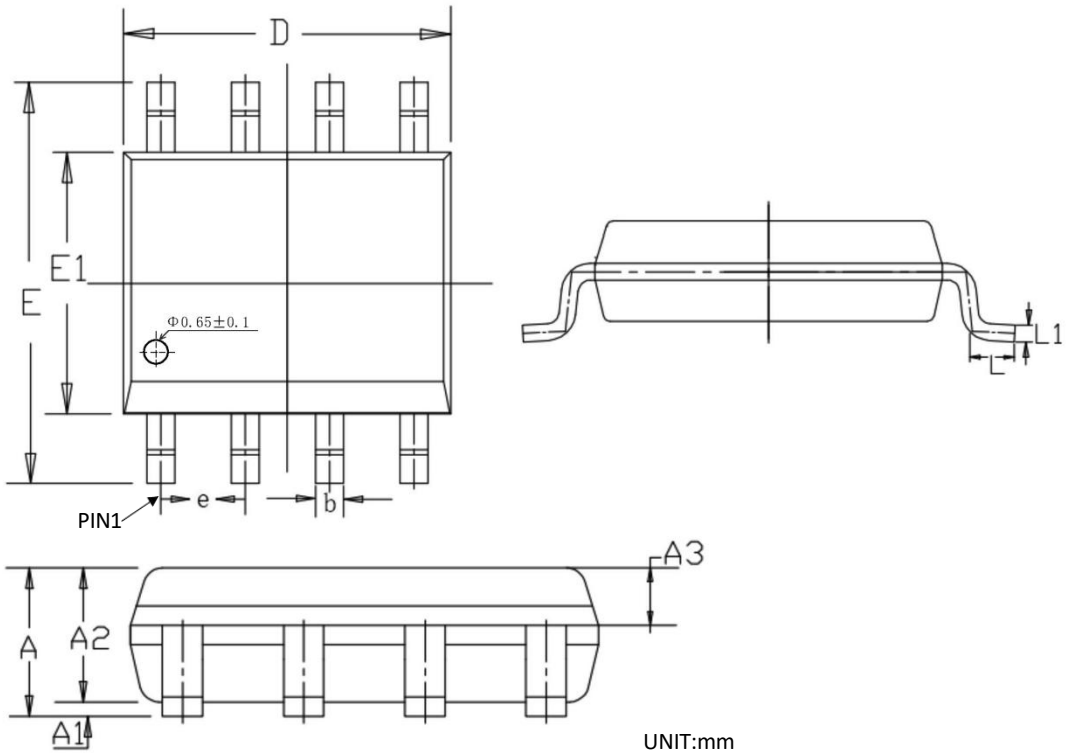
9. ORDERING INFORMATION

Ordering Information

Part Number	Device Making	Package type	Body size (mm)	Temperate (℃)	MSL	Transpo Media	Package Quantit
XLADUM1280ARZ-RL7	XL1280A	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLADUM1280BRZ-RL7	XL1280B	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLADUM1285ARZ-RL7	XL1285A	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLADUM1285BRZ-RL7	XL1285B	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLADUM1281ARZ-RL7	XL1281A	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLADUM1281BRZ-RL7	XL1281B	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLADUM1286ARZ-RL7	XL1286A	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500
XLADUM1286BRZ-RL7	XL1286B	SOP-8	4.90*3.90	-40 to +105	MSL3	T&R	2500

10. DIMENSIONAL DRAWINGS

SOP8



UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—