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PRODUCT SPECIFICATION

Customer: _____

Product Name: 8 Channel SMBus and I2C Switch

Part NO: FCA9548

Issue Date: _____

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Prepared	Checked	Customer Check
ChenTT	Zelig	

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1 Features

- I²C Bus and SMBus compatible
- SCL Frequency: 0 ~ 1MHz
- 1-of-8 Bidirectional translating switches
- Active-low reset input RESET
- Three address pins, allowing up to eight FCA954 8 devices on the I²C Bus
- Allows voltage-level translation between 1.8V, 2.5V, 3.3V, 5V buses
- Low on-resistance, low standby current
- Supply voltage: 1.65V ~ 5.5V
- Operating temperature : -40~ 125℃
- Support hot insertion

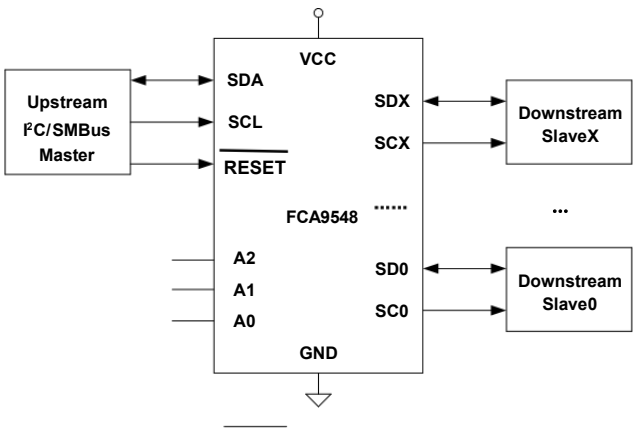
Package information:

PART NUMBER	PACKAGE	BODY SIZE(mm2)
FCA9548T	TSSOP-24	7.80 × 4.40
FCA9548Q	QFN-24	4.00 × 4.00

2 Applications

- Servers
- Routers
- Products with I²C slave address conflicts

Figure 1 Simplified Diagram of FCA9548



3 Description

The FCA9548 is an I2C-controlled device that incorporates four bidirectional voltage-level translation switches. It enables a single upstream SCL/SDA pair to be expanded into four downstream channels. The selection of any individual SCx/SDx channel, or any combination thereof, is accomplished by writing the appropriate values to the programmable control register.

The FCA9548 incorporates an active-low reset input (RESET) to address fault conditions where a downstream I2C bus becomes locked in a low state. Asserting RESET low initiates a reset of the internal I2C state machine and deselects all channels, an effect also achieved by the built-in power-on reset circuitry. The switch pass-gate architecture enables the VCC pin to serve as a clamp for the maximum high-level voltage passed by the device, thereby accommodating mixed-voltage system designs. This allows 1.8V, 2.5V, or 3.3V components to interface directly with 5V devices without requiring external protection circuitry. Bus voltages for each channel are set independently via external pull-up resistors tied to the desired supply levels. Furthermore, all I/O pins are rated to withstand up to 5.5V.

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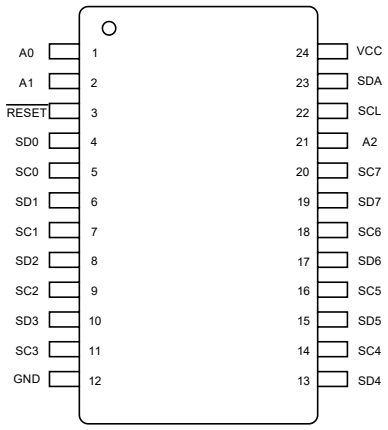
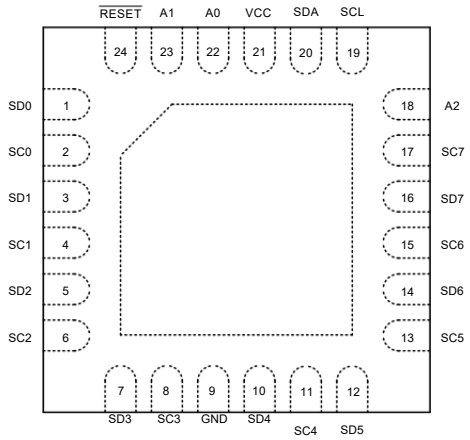
4 Pin Configuration and Functions

FCA9548 24-PIN TSSOP Top View



FCA9548 24-PIN QFN Top View



Pin Functions of TSSOP / QFN Package

PIN			TYPE	DESCRIPTION
NAME	TSSOP	QFN		
A0	1	22	I	Address input 0. Connect directly to VCC or ground.
A1	2	23	I	Address input 1. Connect directly to VCC or ground.
A2	21	18	I	Address input 2. Connect directly to VCC or ground.
GND	12	9	—	Ground.
$\overline{\text{RESET}}$	3	24	I	Active low reset input. Connect to VCC or V_{DPUM} through a pull-up resistor, if not used.
SD0	4	1	I/O	Serial data 0. Connect to V_{DPU0} through a pull-up resistor.
SC0	5	2	I/O	Serial clock 0. Connect to V_{DPU0} through a pull-up resistor.
SD1	6	3	I/O	Serial data 1. Connect to V_{DPU1} through a pull-up resistor.
SC1	7	4	I/O	Serial clock 1. Connect to V_{DPU1} through a pull-up resistor.
SD2	8	5	I/O	Serial data 2. Connect to V_{DPU2} through a pull-up resistor.
SC2	9	6	I/O	Serial clock 2. Connect to V_{DPU2} through a pull-up resistor.
SD3	10	7	I/O	Serial data 3. Connect to V_{DPU3} through a pull-up resistor.
SC3	11	8	I/O	Serial clock 3. Connect to V_{DPU3} through a pull-up resistor.
SD4	13	10	I/O	Serial data 4. Connect to V_{DPU4} through a pull-up resistor.
SC4	14	11	I/O	Serial clock 4. Connect to V_{DPU4} through a pull-up resistor.
SD5	15	12	I/O	Serial data 5. Connect to V_{DPU5} through a pull-up resistor.
SC5	16	13	I/O	Serial clock 5. Connect to V_{DPU5} through a pull-up resistor.
SD6	17	14	I/O	Serial data 6. Connect to V_{DPU6} through a pull-up resistor.
SC6	18	15	I/O	Serial clock 6. Connect to V_{DPU6} through a pull-up resistor.
SD7	19	16	I/O	Serial data 7. Connect to V_{DPU7} through a pull-up resistor.
SC7	20	17	I/O	Serial clock 7. Connect to V_{DPU7} through a pull-up resistor.
SCL	22	19	I/O	Serial clock line. Connect to V_{DPUM} through a pull-up resistor.
SDA	23	20	I/O	Serial data line. Connect to V_{DPUM} through a pull-up resistor.
VCC	24	21	Power	Supply power.

Note: VCC is the supply of FCA9548, V_{DPUM} is the supply of the master, and $V_{DPU7\sim0}$ is the supply of the channel 7~0.

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5 Specifications

5.1 Absolute Maximum Ratings

	MIN	MAX	UNIT
Supply voltage VCC	-0.5	7	V
Input voltage V_I	-0.5	7	V
Input current I_I		±20	mA
Output current I_O		±25	mA
Continuous current through VCC/GND pin		±100	mA
Total power dissipation		400	mW
Operating free-air temperature range	-40	125	℃
Storage temperature range	-60	150	℃

All parameters listed in the preceding table are valid within the specified ambient temperature range unless explicitly noted otherwise. Exposure to conditions exceeding this range may result in irreversible damage to the device.

5.2 ESD Ratings

		Value	UNIT
Electrostatic Discharge	Human-body mode (HBM), per ANSI/ESDA/JEDEC JS-001-2017.	±8000	V
	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002-2022	±1400	V
Latch-up Effect	Latch-up (LU), per JESD 78F (2022)	±200	mA

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage VCC		1.65		5.5	V
High-level input voltage V_{IH}	SCL, SDA	0.7*VCC		6	V
	A2, A1, A0, $\overline{\text{RESET}}$	0.7*VCC		VCC+0.5	
Low-level input voltage V_{IL}	SCL, SDA	-0.5		0.3*VCC	V
	A2, A1, A0, $\overline{\text{RESET}}$	-0.5		0.3*VCC	
Operating temperature range		-40		125	℃

Unless otherwise specified, the specifications in the above table apply within the atmospheric temperature range.

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5.4 Electrical Characteristics

Unless otherwise specified, the following data are characteristics at +25℃ and the power supply voltage is in the range of 1.65 V to 5.5 V.

Parameter	Test Conditions	MIN	TYP	MAX	UNIT
Power-on Reset V_{PORR}	VCC rising, No Load		1.20	1.50	V
Power-on Reset V_{PORR}	VCC falling, No Load	0.80	1.05		V
VCC(1) at transmission across voltage domains	V_{PASS}=1V, R_P=4.7kohm(2)			2.2	V
	V_{PASS}=1.8V, R_P=4.7kohm			3.2	
	V_{PASS}=2.5V, R_P=4.7kohm			4.1	
	V_{PASS}=3.3V, R_P=4.7kohm			5.1	
I_{OL}	SDA, V_{OL}=0.4V	3	6.5		mA
	SDA, V_{OL}=0.6V	6	9.7		
F_{SCL}(3)	Standard-Mode			100	kHz
	Fast Mode			400	kHz
	Fast Mode Plus			1000	kHz
Switch on-state resistance R_{ON}	V_O=0.4V, I_O=10mA, VCC=1.8V		52		ohm
	V_O=0.4V, I_O=10mA, VCC=3.3V		10		
	V_O=0.4V, I_O=10mA, VCC=5.5V		7		
	V_O=0.4V, I_O=15mA, VCC=3.3V		10		
	V_O=0.4V, I_O=15mA, VCC=5.5V		7		
C_I	A2, A1, A0, $\overline{RESET}$		4.5	6	pF
I_{CC}	VCC=1.65V, F_{SCL}=100kHz		2		μA
	VCC=3.3V, F_{SCL}=100kHz		4		
	VCC=5.5V, F_{SCL}=100kHz		10		
	VCC=1.65V, F_{SCL}=400kHz		3		
	VCC=3.3V, F_{SCL}=400kHz		6		
	VCC=5.5V, F_{SCL}=400kHz		17		
	VCC=1.65V, SCL=SDA=VDPUM		0.4	0.6	
	VCC=2.7V, SCL=SDA=VDPUM		0.7	1.1	
	VCC=3.3V, SCL=SDA=VDPUM		1.0	1.3	
	VCC=5.5V, SCL=SDA=VDPUM		1.6	2	
$\overline{RESET}$ Pin reset pulse time		20			ns

Note:

1) For details on transmission across voltage domains, seeSection 6.2.3.

2) R_P is the pull-up resistor of the corresponding channel. All channel pull-up resistors have equal values.

3) When F_{SCL} ≥400kHz, the pull-up resistance RP should be ≤1kohm, depending on the bus load capacitance.

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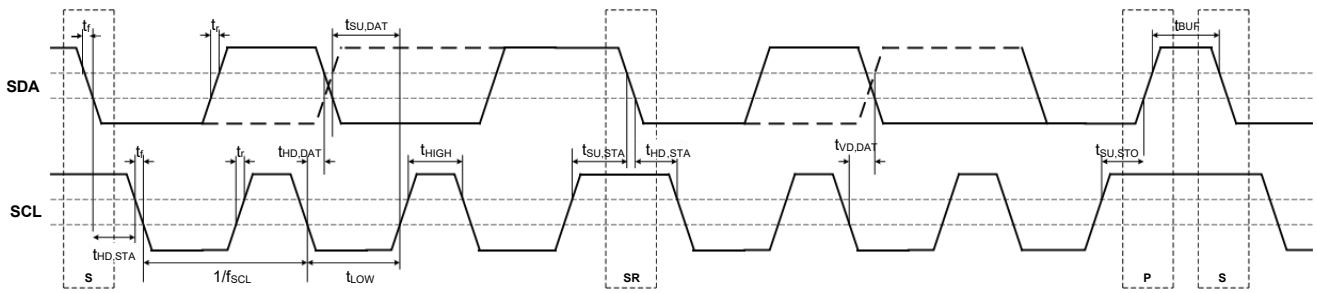
5.5 I2C Timing Requirements

Unless otherwise specified, the following data are the characteristics of the chip in the range of -40 to +125° C.

	Description	Standard-Mode		Fast-Mode		Fast-Mode Plus		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{SCL}	SCL operating frequency	0	100	0	400	0	1000	kHz
$t_{HD,STA}$	hold time after repeated start condition; After this period, the first clock is generated	4.0		0.6		0.26		μs
t_{LOW}	SCL clock low period	4.7		1.3		0.5		μs
t_{HIGH}	SCL clock high period	4.0		0.6		0.26		μs
$t_{SU,STA}$	repeated start condition setup time	4.7		0.6		0.26		μs
$t_{HD,DAT}$	data hold time	0		0		0		ns
$t_{SU,DAT}$	data setup time	250		100		50		ns
t_r	rise time of SDA and SCL		1000	20	300		120	ns
t_f	fall time of SDA and SCL		300	20*VCC /5.5	300	20*VCC /5.5	120	ns
$t_{SU,STO}$	stop condition setup time	4.0		0.6		0.26		μs
t_{BUF}	bus free time between stop and start condition	4.7		1.3		0.5		μs
$t_{VD,DAT}$	data valid time		3.45		0.9		0.45	μs
C_b	capacitive load for each bus line		400		400		550	pF



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6 Detailed Description

6.1 I2C Serial Interface

6.1.1 Bus Overview

The I2C interface employs the serial data line (SDA) and the serial clock line (SCL) to facilitate bidirectional communication among interconnected IC devices. Both SDA and SCL require external pull-up resistors (RP) to the supply voltage. Data transfer is permitted only when the bus is idle, meaning both SDA and SCL remain in a high state. Under the I2C protocol, each SCL clock pulse accommodates exactly one data bit. While the clock signal is high, the logic state on SDA must be held stable; any transition on SDA during this interval is interpreted as a control signal rather than data. When the bus is idle and SCL is high, a falling edge on SDA signifies a start condition, whereas a rising edge on SDA under the same conditions indicates a stop condition, as illustrated in Figure 2.

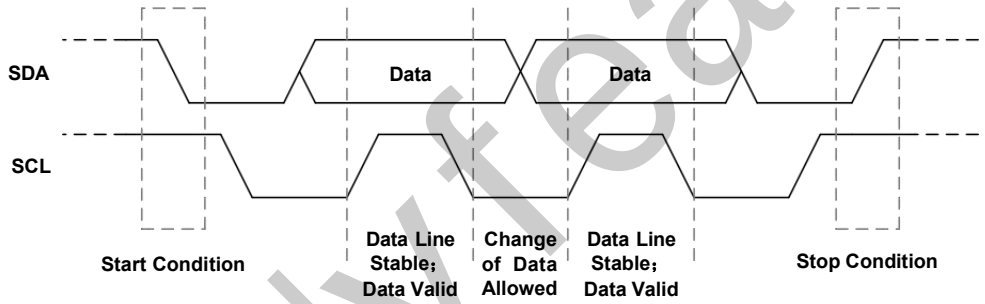

Figure 2. Start Condition, Stop Condition, and Data Bit Transmission in I²C Communication

In I2C communication, the device that initiates a message acts as the transmitter, while the target device serves as the receiver. The device orchestrating the transaction is designated as the master, and the devices responding to the master are slaves. Between the start and stop conditions, an unrestricted number of data bytes can be transmitted between master and slave. Each 8-bit data byte must be followed by an acknowledgment (ACK) bit. When the master transmits data to a slave, it must release the SDA line after each byte, allowing the slave to pull SDA low to generate the ACK and confirm successful reception. Conversely, when the slave returns data to the master, it releases SDA after each byte so that the master can produce the ACK bit. During the high period of the ninth SCL clock pulse used for the ACK, SDA must remain stable low, with proper setup and hold times observed per the I2C protocol. Upon receiving the last byte from the slave, the master must issue a NACK bit by releasing SDA and allowing it to go high. The master then generates a stop condition, terminating the data transfer.

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6.1.2 Control Register

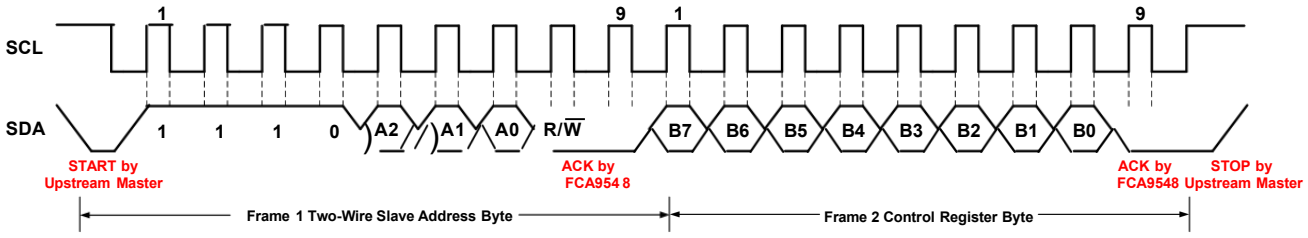

Figure 3 Diagram of Control Register Write Operation

During device operation, the upstream host can program the internal control registers of the FCA9548 to govern data routing between the host and one or more downstream slave devices. Figure 3 illustrates the host's write sequence to the control register. The host initiates the transaction by transmitting a slave address byte with the LSB cleared (read/write bit = 0) to target the specific FCA9548 on the bus. The lower three bits of this slave address serve as address selection bits, allowing the FCA9548 to be assigned one of eight distinct slave addresses via the A2, A1, and A0 pins. These bits reflect the pin connection states: tying an address pin to the supply voltage sets the corresponding bit to logic 1, while grounding the pin sets it to logic 0. Detailed address assignments are provided in Table 1.

Table 1 Address Reference

ADDRESS PIN CONNECTION			I²C SLAVE ADDRESS
A2	A1	A0	
GND	GND	GND	112d / 70h
GND	GND	VCC	113d / 71h
GND	VCC	GND	114d / 72h
GND	VCC	VCC	115d / 73h
VCC	GND	GND	116d / 74h
VCC	GND	VCC	117d / 75h
VCC	VCC	GND	118d / 76h
VCC	VCC	VCC	119d / 77h

After the addressed FCA9548 successfully responds to the slave address byte, the upstream host proceed s to send the Control register configuration byte.

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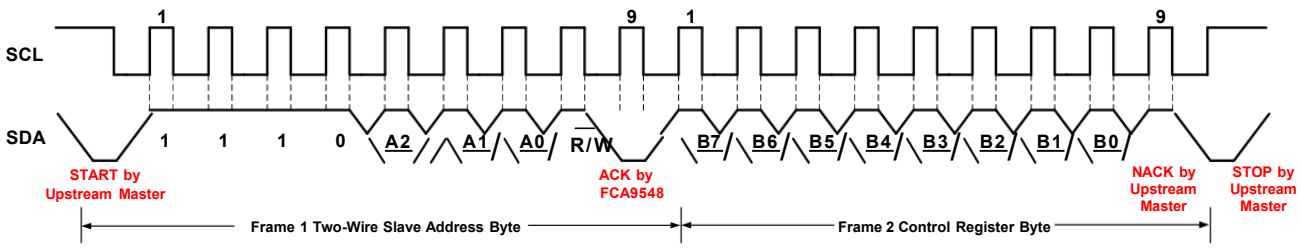

Figure 4 Diagram of Control Register Read Operation

Figure 4 illustrates the read sequence employed by the upstream host to access the FCA9548 Control registers. Table 2 provides the bit definitions for these registers. All bits (B7 through B0) are fully readable and writable, and their settings govern data routing between the upstream master and one or more downstream channel slaves. When any bit within B7~B0 is set to 1, the corresponding downstream channel's SCX/SDX buses are internally connected to the upstream master's SDA/SCL lines. This connection is established upon the Stop Condition that terminates the control register write operation. The register powers up to a default value of 00h, meaning all downstream channels are disabled at initial power-on. The FCA9548 supports simultaneous activation of multiple downstream channels, provided that the total bus capacitive load does not exceed the maximum specified in Section 5.5.

Table 2 The definition of Control register

B7	B6	B5	B4	B3	B2	B1	B0	Description
X	X	X	X	X	X	X	0	Channel 0 disabled
							1	Channel 0 enabled
X	X	X	X	X	X	0	X	Channel 1 disabled
						1		Channel 1 enabled
X	X	X	X	X	0	X	X	Channel 2 disabled
					1			Channel 2 enabled
X	X	X	X	0	X	X	X	Channel 3 disabled
				1				Channel 3 enabled
X	X	X	0	X	X	X	X	Channel 4 disabled
			1					Channel 4 enabled
X	X	0	X	X	X	X	X	Channel 5 disabled
		1						Channel 5 enabled
X	0	X	X	X	X	X	X	Channel 6 disabled
	1							Channel 6 enabled
0	X	X	X	X	X	X	X	Channel 7 disabled
1								Channel 7 enabled
0	0	0	0	0	0	0	0	No channel selected

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6.2 Device Functional Modes

6.2.1 Power-On Reset

Upon power-up of the FCA9548 VCC supply, the internal control registers and I2C state machine are initialized to their default states. In this condition, all downstream channels are disabled, and all register bits are cleared to 0. This initialized state persists until VCC exceeds the VPORR threshold, at which point the device becomes fully operational and responds according to system configuration. Should the supply voltage fall below VPORF, the device reverts to its initial reset state.

6.2.2 RESETN

The FCA9548 provides an active-low reset pin (RESET) for global device reset in the event of a bus fault condition. To ensure a reliable reset, the low pulse applied to the RESET pin must have a duration exceeding 20 ns. When this function is not required, the pin should be tied to the supply voltage via a pull-up resistor to avoid unintended device resets.

6.2.3 Data Transmission Across Voltage Domains

The FCA9548 family enables data transmission between the upstream host and downstream channel slaves across different voltage domains. In this configuration, the device's VCC supply voltage establishes the minimum allowable level for both upstream and downstream communication. This capability facilitates direct data exchange between upstream and downstream nodes across 1.8V, 3.3V, and 5.0V domains without requiring additional protection circuitry. When utilizing this feature, each upstream and downstream I2C bus must be connected to its respective supply voltage via an external pull-up resistor RP, as illustrated in Figure 5.

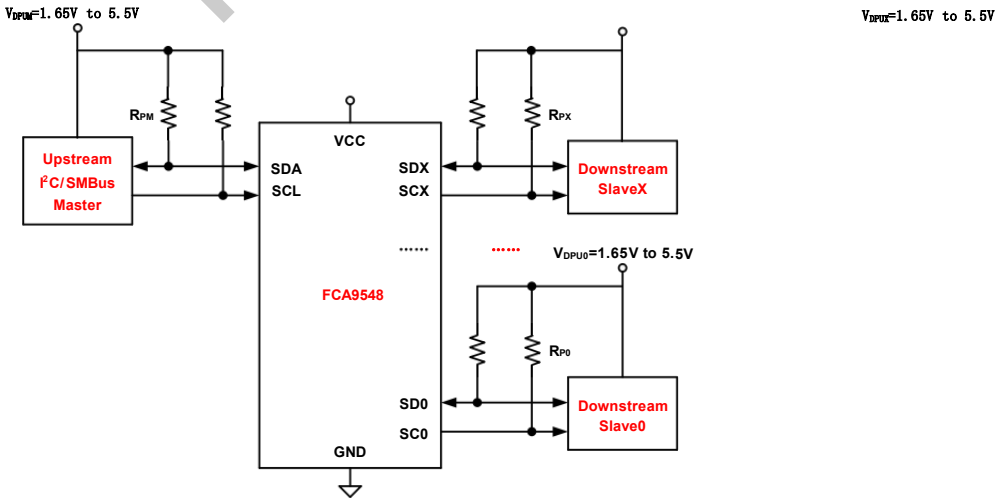

Figure 5 Diagram of Data Transmission Across Voltage Domains

In Figure 5, the upstream host operates from supply VDPUM, while each downstream channel slave is powered by VDPUX. The SDA/SCL lines are pulled up to VDPUM via resistors RPM, and the SDX/SCX lines

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are pulled up to VDPUX via resistors RPX. The minimum pass-through voltage for transmission is given by VPASS = min(VDPUM, VDPUX).(V_{DPUM} , V_{DPUO} , …, V_{DPUX}) is defined.

When the FCA9548 Control register is programmed to enable channel X, the resulting data transmission behavior on the bus is depicted in Figure 6 and Figure 7 (using the SDA and SDX lines as examples). Figure 6 illustrates high-level transmission, while Figure 7 illustrates low-level transmission. Given the symmetry of the circuit topology, the analysis focuses on the case where VDPUM > VDPUX, resulting in VPASS = VDPUX, with VDPUM fixed at 5.5V.

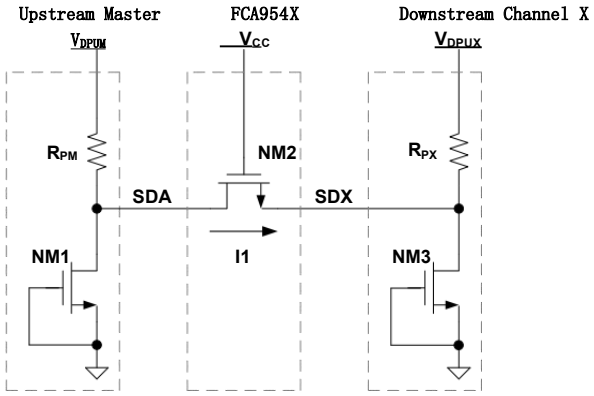

Figure 6 Diagram of High-level Bus Transmission

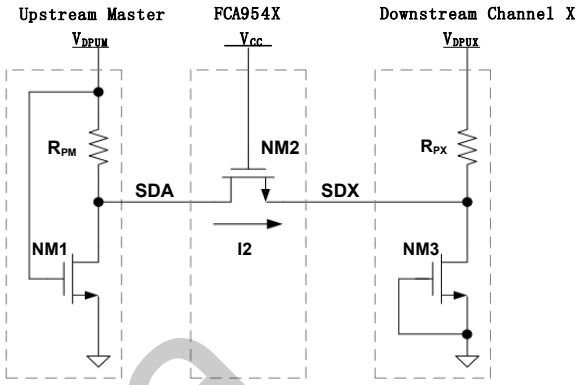

Figure 7 Diagram of Low-level Bus Transmission

For proper high-level transmission in the system shown in Figure 6, two conditions must be satisfied:

1) SDA > 0.7 × VDPUM, ensuring that the upstream host consistently recognizes SDA as a logic-high state;

2) SDX < 1.1 × VDPUX, guaranteeing that the voltage on SDX remains within the absolute maximum rating of the downstream slave's I/O ports.

When VPASS = VDPUX, condition 2) imposes the primary constraint on system operation. Based on this limitation, the maximum allowable VCC for the FCA9548 can be derived for various VPASS levels, as plotted in Figure 8 (with RPM = RPX and VDPUM = 5.5V).

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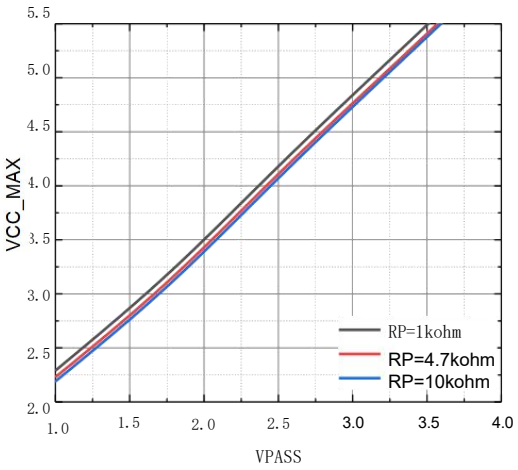

Figure 8 Relation Between Maximum VCC and V_{PASS} during Cross-Voltage Data Transmission

When low-level transmission is performed , the value of |SDA-SDX| mainly depends on the on-resistance R_{ON} of NM2 in Figure 7, as shown inSection 5.4 for details.

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7 Detailed Application

NOTE

The following content comprises precautions and usage recommendations provided by NYFEA for the FCA9548 in specific applications. NYFEA does not warrant the accuracy or completeness of this information. Customers are solely responsible for evaluating the suitability of the components for their intended purposes, based on their own application requirements and use cases. It is the customer's responsibility to test and validate their design implementation to ensure proper system operation and to mitigate any potential losses.

The FCA9548 supports simultaneous enablement of multiple downstream channels via the Control register. In this configuration, any I2C command issued by the upstream master is broadcast to all active downstream slaves. Careful attention must be paid to the total current drawn through the SDA and SCL pins during such operations—particularly in cross-voltage-domain data transmission—and the limits specified in Section 5.1 must not be exceeded.

The device also permits multiple downstream slaves to share the same I2C address across different channels. When the upstream master issues a read command targeting a slave address that appears on multiple active channels, a bus conflict may occur if the read-back register values differ among those slaves. Under such conditions, the data returned on SDA represents the logical AND combination of the values from all responding slaves. Users should evaluate the potential risks associated with this scenario before deploying such configurations in their systems.

The FCA9548 permits downstream slave devices to be assigned the same I2C address as the FCA9548 itself. However, this configuration may give rise to communication conflicts, and users should conduct a thorough risk assessment prior to implementation.

The FCA9548 is fully compliant with Standard-Mode, Fast-Mode, and Fast-Mode Plus specifications of the I2C protocol, supporting bus operation up to 1MHz. When operating in any of these three modes, the pull-up resistor RP on the SCL and SDA lines must be selected to meet the following requirements:

$$R_P(min) = \frac{VCC - V_{OL}(max)}{I_{OL}} \text{、} R_P(max) = \frac{t_r}{(0.8473 \times C_b)}$$

The specific indicators in the formula are detailed in sections 5.4 and section 5 .5.

For typical applications, a 4.7kΩ pull-up resistor (RP) is recommended when the FCA9548 operates in Standard-Mode or Fast-Mode (fSCL ≤ 400kHz). For Fast-Mode Plus operation (400kHz < fSCL ≤ 1000kHz), a 500Ω resistor is suggested. In practice, the optimal RP value should be determined by the user based on the actual bus capacitance and operating frequency to ensure error-free I2C communication.

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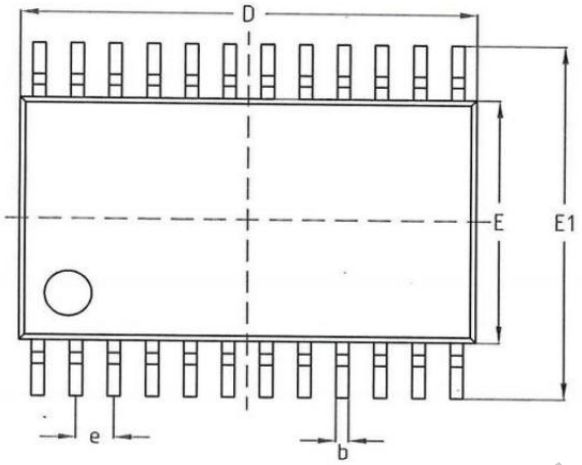
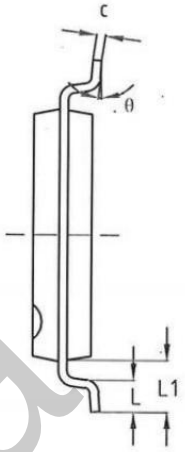
8 Package Informations

8.1 TSSOP-24

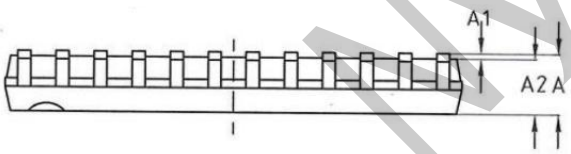
TOP VIEW



SIDE VIEW



SIDE VIEW



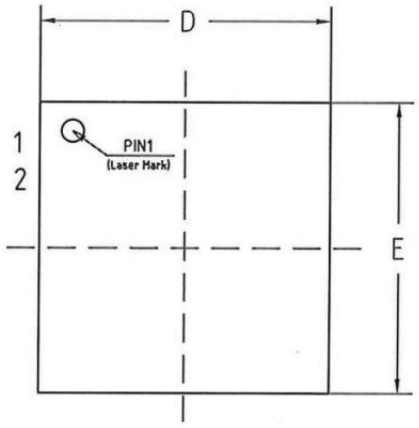
Dimensions			
SYMBOL	MIN	NOMINAL	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	7.70	7.80	7.90
E	4.30	4.40	4.50
E1	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
θ	0°	–	8°

Nyfea

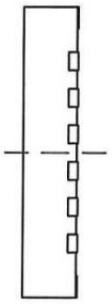
NYFEA

8.2 QFN-24

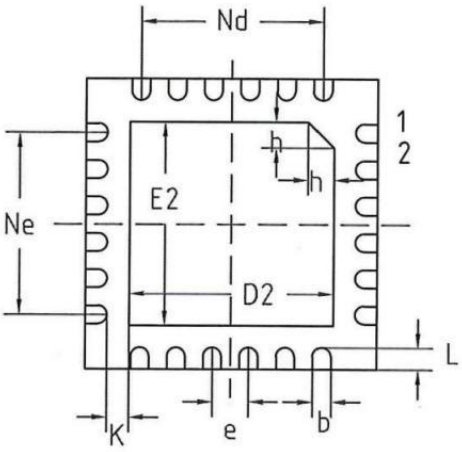
TOP VIEW



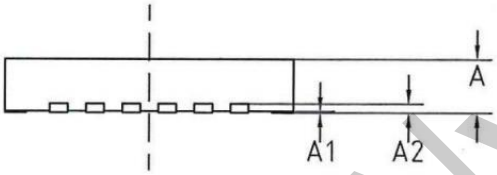
SIDE VIEW



BOTTOM VIEW



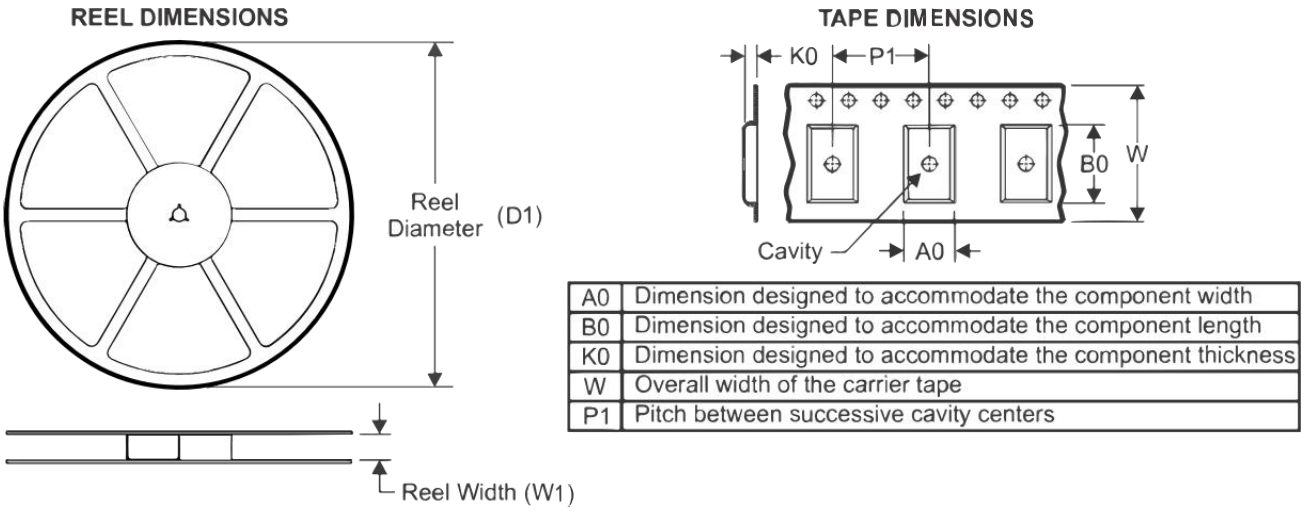
SIDE VIEW



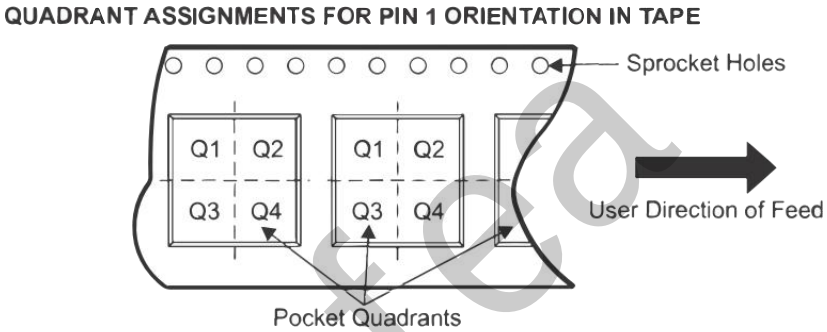
Dimensions mm			
SYMBOL	MIN	NOMINAL	MAX
A	0.45	0.50	0.55
A1	-	0.02	0.05
A2	0.127 REF		
b	0.2	0.25	0.30
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
e	0.50 BSC		
K	0.25	0.30	0.35
L	0.25	0.30	0.35
h	0.30	0.35	0.40
Ne	2.50 BSC		
Nd	2.50 BSC		

Nyfea

8.3 Reel and Tape Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 quadrant
TSSOP-24	330	16.40	6.95	8.30	1.60	8.00	16.00	Q1
QFN-24	330	12.40	4.30	4.30	1.00	8.00	12.00	Q2

9 Ordering Information

Order Number	Chip Model	Package	Standard Quantity	Note
FCA9548T-T&R	FCA9548T	TSSOP-24	4000	Tape & Reel
FCA9548Q-T&R	FCA9548Q	QFN-24	4000	Tape & Reel