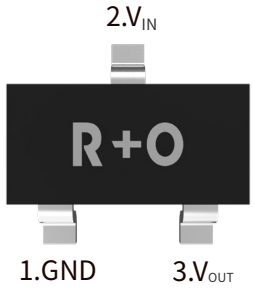
100mA CMOS Voltage Regulators

Features

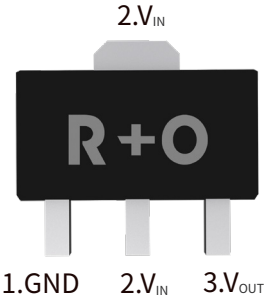
- Quiescent Current: 1μA
- Input Voltage Range: 30V
- Output Current: 100mA
- Low Dropout Voltage: 100mV(Max.)@1mA)
- Output Voltage: 2.1V, 2.3V, 2.5V, 2.7V, 3.0V, 3.3V, 3.6V, 4.0V, 4.4V, 5.0V
- Output Voltage Accuracy: ±2%（Typ.）
- Low Power Consumption

Output Current
100mA
Input Voltage
30V

SOT-23(-3L)



SOT-89



Applications

- Battery Power Supply Equipment
- Communication Equipment
- Audio/Video Equipment
- Monitor Equipment

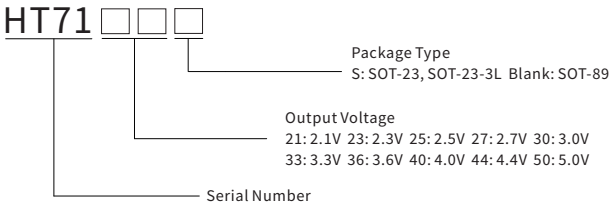
General Description

The HT71 Series consists of a current limiter circuit,a driver transistor, a precision reference voltage and an error correction circuit. The series is compatible with low ESR ceramic capacitors. The current limiter's foldback circuit operates as a short circuit protection as well as the output current limiter for the output pin.

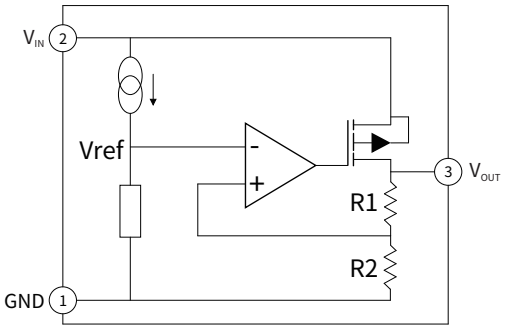
Reference News

SOT-23 Marking:	SOT-23-3L Marking:	SOT-89 Marking:
HT7121S: HT21	HT7121S: HT21	HT7121: 7520-1
HT7123S: HT23	HT7123S: HT23	HT7123: 7524-1
HT7125S: HT25	HT7125S: HT25	HT7125: 7525-1
HT7127S: HT27	HT7127S: HT27	HT7127: 7528-1
HT7130S: HT30	HT7130S: HT30	HT7130: 7530-1
HT7133S: HT33	HT7133S: HT33	HT7133: 7533-1
HT7136S: HT36	HT7136S: HT36	HT7136: 7536-1
HT7140S: HT40	HT7140S: HT40	HT7140: 7540-1
HT7144S: HT44	HT7144S: HT44	HT7144: 7544-1
HT7150S: HT50	HT7150S: HT50	HT7150: 7550-1

Part Numbering



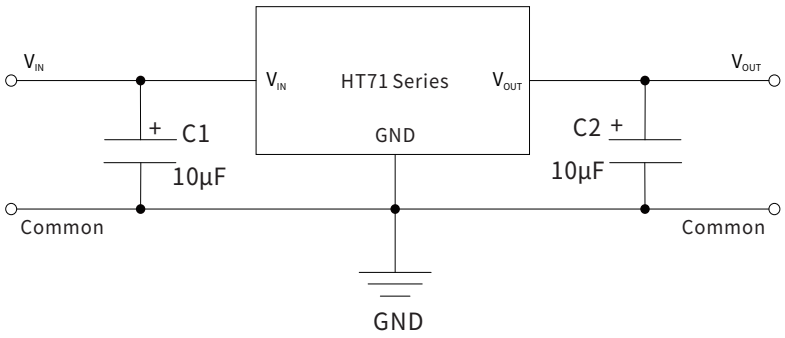
Block Diagram



Ordering Information

Package	Package Code	Unit Weight(g)	Reel(pcs)	Box(pcs)	Carton(pcs)	Delivery Mode	MSL
SOT-23	R1	0.008	3000	30000	180000	7''	3
SOT-23-3L	R1	0.0132	3000	30000	180000	7''	3
SOT-89	R1	0.045	1000	8000	48000	7''	3

Typical Application Circuit



Absolute Maximum Ratings (T_A = 25°C Unless otherwise specified)

Parameter	Symbol	Value	Unit
Input Voltage Limit	V_{IN}	30	V
Operating Current	I_O	100	mA
Power Dissipation	P_D(SOT-23(-3L))	200	mW
	P_D(SOT-89)	500	
Thermal Resistance Junction-Ambient	$R_{\theta JA}$(SOT-23(-3L))	500	°C /W
	$R_{\theta JA}$(SOT-89)	200	
Solder Temperature/Time	T_d	260/10	°C /S
Operating Ambient Temperature	T_A	-25~+85	°C
Junction and Storage Temperature	T_J,T_{stg}	-50~+125	°C

Note: Exceed these limits to damage to the device, exposure to absolute maximum rating conditions may affect the reliability of the chip.

Electrical Characteristics(T_A = 25°C Unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V_{OUT}	I_{OUT} = 10mA, V_{IN} = V_{OUT} + 2V	V_{OUT} × 0.98	V_{OUT}	V_{OUT} × 1.02	V
Output Current	I_O	V_{IN} = V_{OUT} + 2V	20	30	--	mA
Dropout Voltage	V_D	V_{OUT} ⩾ 3.3V, I_{OUT} = 1mA, △V_{OUT} = 2%	--	35	55	mV
		V_{OUT} < 3.3V, I_{OUT} = 1mA, △V_{OUT} = 2%	--	35	100	mV
Quiescent Current	I_Q	V_{IN} = V_{OUT} + 2V, R_L = ∞	--	1	3	μA
Line Regulation	△V_{OUT} / △V_{IN}·V_{OUT}	I_{OUT} = 1mA, V_{OUT} + 1V ⩽ V_{IN} ⩽ 30V	--	0.1	0.2	%/V
Load Regulation	△V_{OUT}	1mA ⩽ I_{OUT} ⩽ 30mA V_{IN} = V_{OUT} + 2V, V_{OUT} ⩾ 3.3V	--	15	45	mV
		1mA ⩽ I_{OUT} ⩽ 20mA V_{IN} = V_{OUT} + 2V, V_{OUT} < 3.3V	--	15	45	mV
Output Voltage Temperature Coefficient	△V_{OUT} / △T_A·V_{OUT}	V_{IN} = V_{OUT}+2V, I_{OUT} = 10mA	--	±100	--	ppm/°C

Note: The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} is 98% of the normal value of V_{OUT}.

Functional Description

Input Capacitor

A 10μF ceramic capacitor is recommended to connect between V_{IN} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended minimum output capacitance is 10μF, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot.
Place output capacitor as close as possible to V_{OUT} and GND pins.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA.}$
Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C , T_A is the ambient temperature and the $R_{\theta JA}$ is the junction to ambient thermal resistance.The power dissipation definition in device is： $P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$.

Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the HT71 Series ground pin using as wide and as short of a copper trace as is practical.Connections using long trace lengths, narrow trace widths, and connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

Ratings And Characteristics Curves(HT7133(S))(T_A = 25 °C Unless otherwise specified)

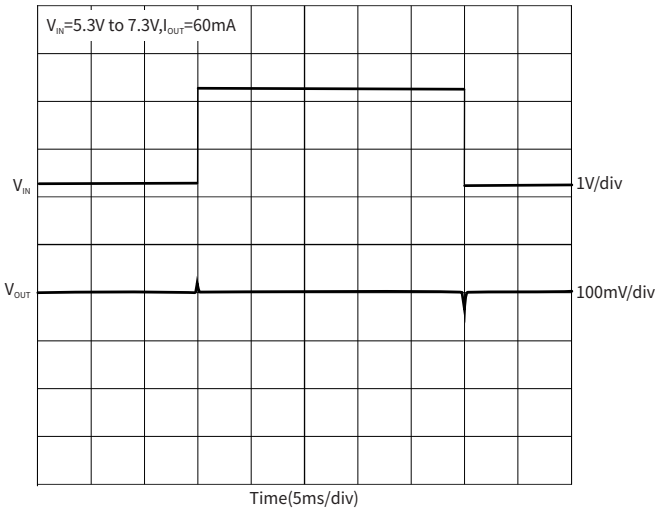


Fig.1 Line -Transient Response

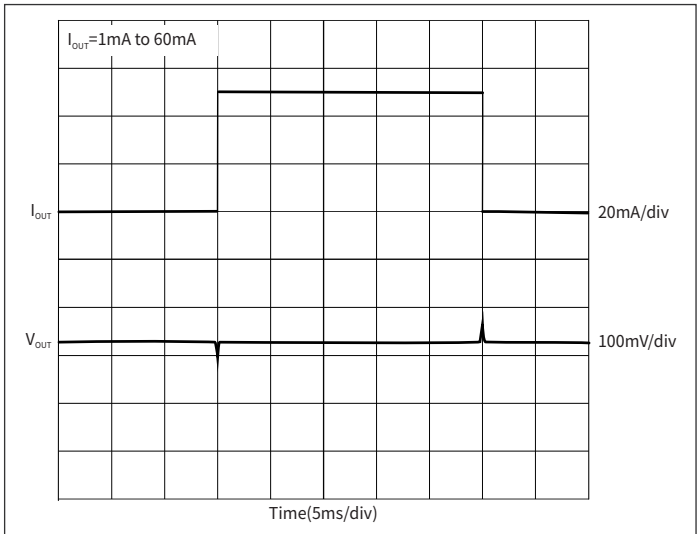


Fig.2 Load -Transient Response

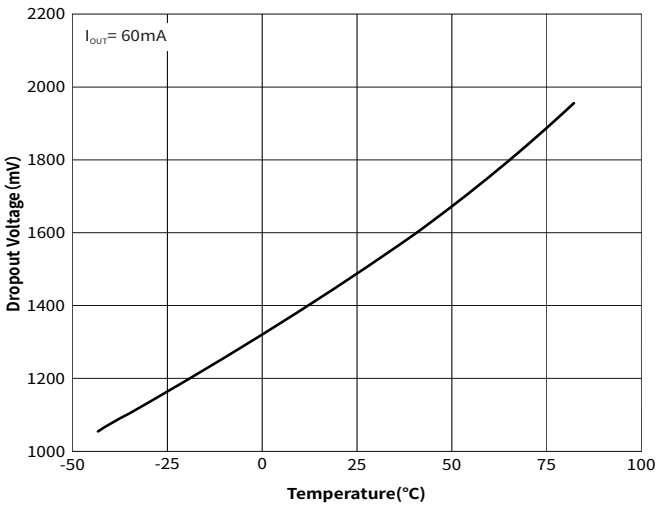


Fig.3 Dropout Voltage vs. Temperature

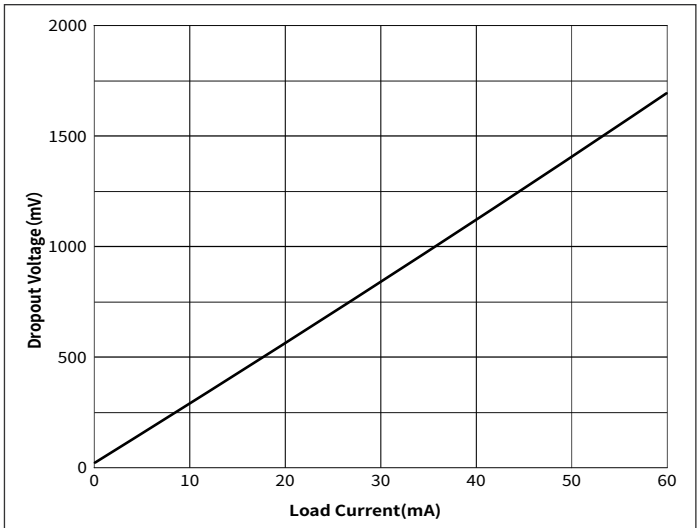


Fig.4 Dropout Voltage vs. Output Current

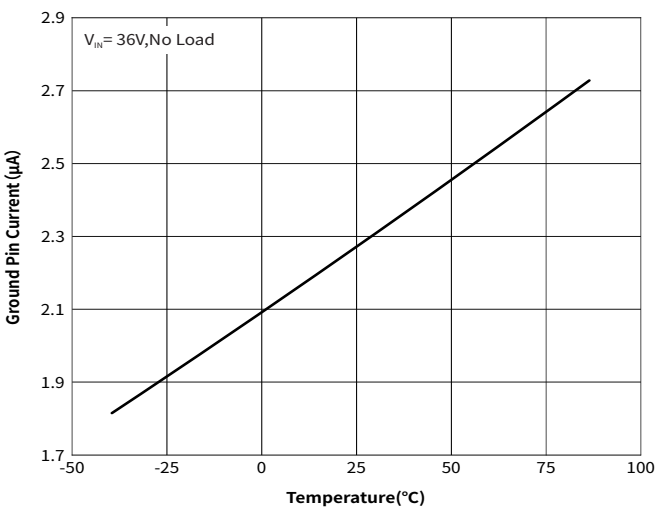


Fig.5 Ground Pin Current vs. Temperature

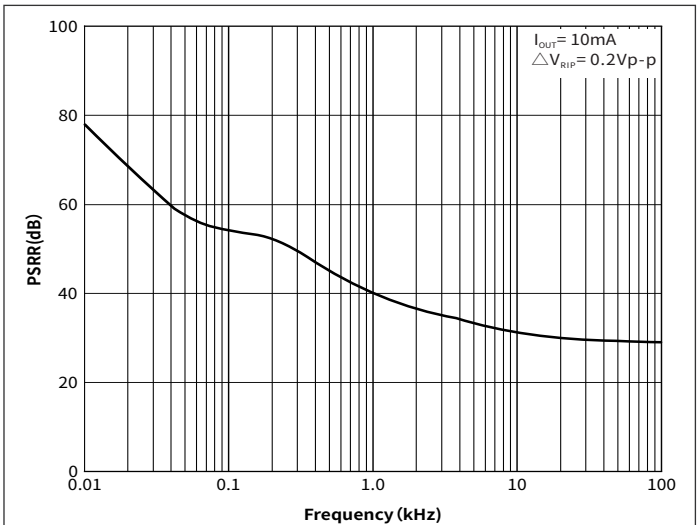
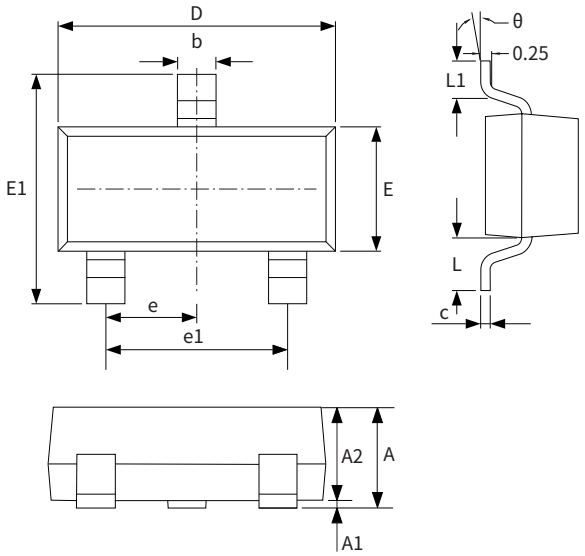


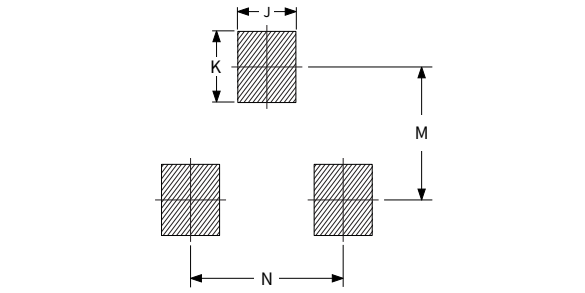
Fig.6 Power Supply Rejection Ratio vs. Frequency

Package Outline Dimensions (SOT-23)



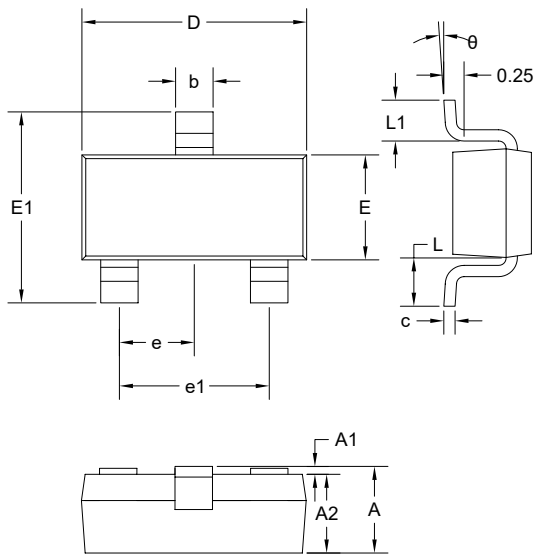
Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.90	1.15	0.035	0.045
A1	-	0.10	-	0.004
A2	0.90	1.05	0.035	0.041
b	0.30	0.50	0.012	0.020
c	0.10	0.20	0.004	0.008
D	2.80	3.00	0.110	0.118
E	1.20	1.40	0.047	0.055
E1	2.25	2.55	0.089	0.100
e	0.950TYP		0.037TYP	
e1	1.80	2.00	0.071	0.079
L	0.550REF		0.022REF	
L1	0.30	0.50	0.012	0.020
θ	-	8°	-	8°

Suggested Pad Layout



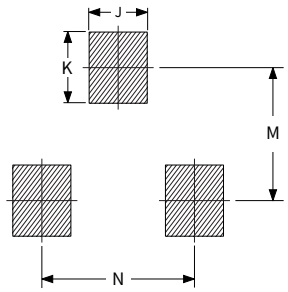
Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
J	0.80	-	0.031	-
K	-	0.90	-	0.035
M	2.00	-	0.078	-
N	-	1.90	-	0.074

Package Outline Dimensions (SOT-23-3L)



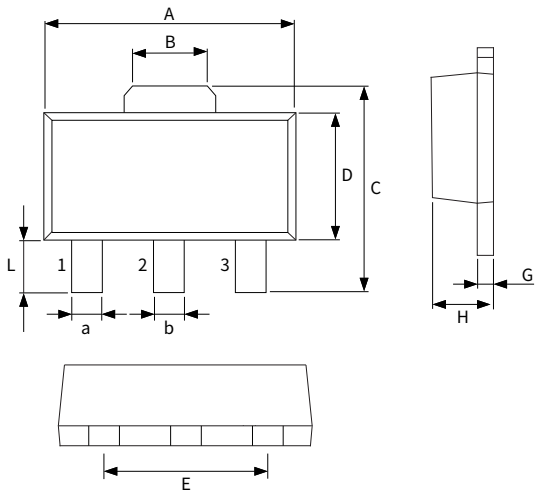
Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.05	1.25	0.041	0.049
A1	-	0.10	-	0.004
A2	1.05	1.15	0.041	0.045
b	0.30	0.50	0.012	0.020
c	0.10	0.20	0.004	0.008
D	2.82	3.02	0.111	0.119
E	1.50	1.70	0.059	0.067
E1	2.65	2.95	0.104	0.116
e	0.90	1.00	0.035	0.039
e1	1.80	2.00	0.071	0.079
L	0.45	0.65	0.018	0.026
L1	0.30	0.60	0.012	0.024
θ	-	8°	-	8°

Suggested Pad Layout



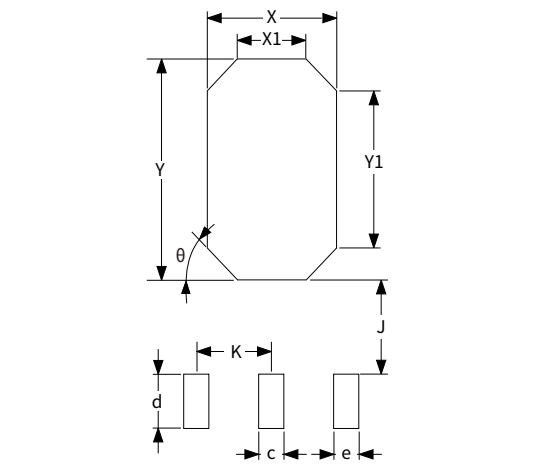
Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
J	0.80	-	0.031	-
K	-	0.95	-	0.037
M	2.00	-	0.078	-
N	-	2.0	-	0.079

Package Outline Dimensions (SOT-89)



Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	4.40	4.60	0.173	0.181
B	1.35	1.83	0.053	0.072
C	3.75	4.25	0.148	0.167
D	2.29	2.60	0.090	0.102
E	2.95	3.05	0.116	0.120
a	0.35	0.48	0.014	0.019
b	0.40	0.56	0.016	0.022
L	0.80	1.20	0.031	0.047
G	0.35	0.44	0.014	0.017
H	1.40	1.60	0.055	0.063

Suggested Pad Layout



Symbol	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
c	0.80	1.00	0.032	0.04
d	1.30	1.50	0.052	0.060
e	0.70	0.90	0.028	0.036
J	1.80	2.00	0.072	0.080
K	1.40	1.60	0.056	0.064
X	2.50	2.70	0.100	0.108
X1	1.30	1.50	0.052	0.060
Y	4.30	4.50	0.172	0.180
Y1	3.10	3.30	0.124	0.132
θ	-	45°	-	45°