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74AHC00S14-TP
Quad 2-input NAND gate

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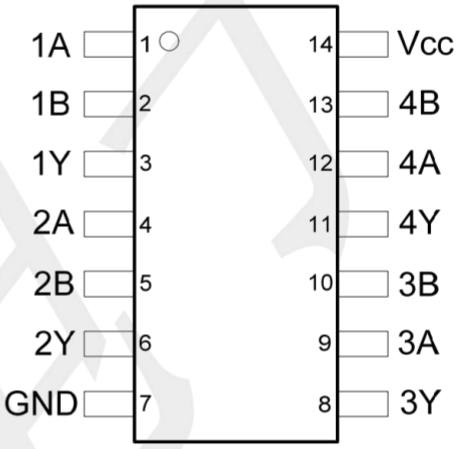
Features

- Wide supply voltage range from 2.0 V to 5.5 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 250 mA
- CMOS level
- ESD protection:
  HBM ANSI/ESDA/JEDEC JS-00
  Class 3A exceeds 6000 V
  CDM ANSI/ESDA/JEDEC JS-002
  Class C3 exceeds 2000 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Complies with JEDEC standard:
  JESD8C (2.7 V to 3.6 V)
  JESD36 (4.5 V to 5.5 V)
- Packaging: SOP-14

General Description

The is a quad 2-input NAND gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of VCC

PIN CONFIGURATIONS (Top view)



SOP-14

PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION	PIN NO.	PIN NAME	DESCRIPTION
1	1A	Data input	8	3Y	Data output
2	1B	Data input	9	3A	Data input
3	1Y	Data output	10	3B	Data input
4	2A	Data input	11	4Y	Data output
5	2B	Data input	12	4A	Data input
6	2Y	Data output	13	4B	Data input
7	GND	ground (0 V)	14	V_{CC}	supply voltage

Functional diagram

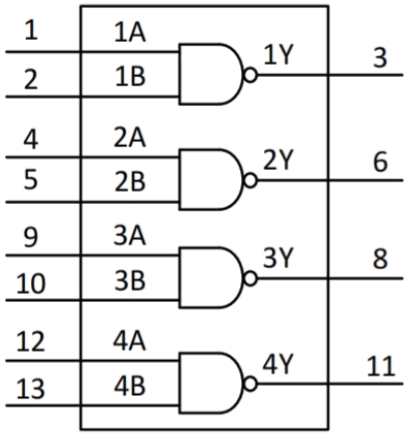


Fig. 1. Logic symbol

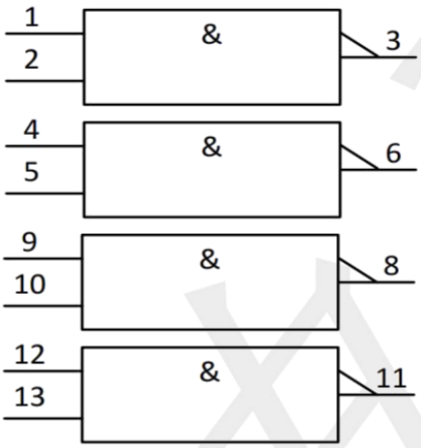


Fig. 2. IEC logic symbol

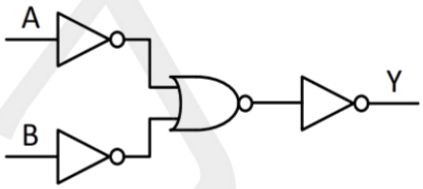


Fig. 3. Logic diagram (one gate)

Functional Description

Function table

Input nA	Input nB	Output nY
L	X	H
X	L	H
H	H	L

H = HIGH voltage level; L = LOW voltage level; X = don't care.

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System. Voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	7.0	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	--	mA
V_I	input voltage	(1)	-0.5	7.0	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	--	±50	mA
V_O	output voltage	Active mode (1)	0	V_{CC} + 0.5	V
		Power-down mode; V_{CC} = 0 V (1)	0	7.0	V
I_O	output current	V_O = 0 V to V_{CC}	--	±50	mA
I_{CC}	supply current		--	100	mA
I_{GND}	ground current		-100	--	mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C	--	500	mW
T_{stg}	storage temperature		-65	150	°C

Note:1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.0	5.5	V
		functional	1.65	--	V
V_I	input voltage		0	5.5	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	5.5	V
T_{amb}	ambient temperature		-40	125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V to 2.7 V	0	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	10	ns/V
		V_{CC} = 4.5 V to 5.5 V	0	5	ns/V

Static characteristics

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	--	--	1.5	--	V
		V_{CC} = 4.5 V	3.15	--	--	3.15	--	V
		V_{CC} = 5.5 V	3.85	--	--	3.85	--	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	--	--	0.5	--	0.5	V
		V_{CC} = 4.5 V	--	--	1.35	--	1.35	V
		V_{CC} = 6.0 V	--	--	1.65	--	1.65	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -20 μA; V_{CC} = 2.0 V	1.9	--	--	1.9	--	V
		I_O = -20 μA; V_{CC} = 4.5 V	4.4	--	--	4.4	--	V
		I_O = -20 μA; V_{CC} = 5.5 V	5.4	--	--	5.4	--	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.84	--	--	3.7	--	V
		I_O = -5.2 mA; V_{CC} = 5.5 V	4.74	--	--	4.7	--	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20 μA; V_{CC} = 2.0 V	--	--	0.1	--	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	--	--	0.1	--	0.1	V
		I_O = 20 μA; V_{CC} = 5.5 V	--	--	0.1	--	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	--	--	0.33	--	0.4	V
		I_O = 5.2 mA; V_{CC} = 5.5 V	--	--	0.33	--	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND ; V_{CC} = 5.5 V	--	--	±1	--	±1	μA
I_{CC}	supply current	V_I = V_{CC} or GND ; I_O = 0 A ; V_{CC} = 5.5 V	--	--	20	--	40	μA
C_I	input capacitance		--	4	--	--	--	pF

Dynamic Characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
t_{pd}	propagation delay	nA, nB to nY; see Fig. 5 [1]						
		V_{CC} = 2.0 V	--	--	35	--	40	ns
		V_{CC} = 4.5 V	--	--	20	--	25	ns
		V_{CC} = 5.5 V	--	--	16	--	21	ns
t_t	transition time	see Fig. 5 [2]						
		V_{CC} = 2.0 V	--	--	9	--	11	ns
		V_{CC} = 4.5 V	--	--	6	--	8	ns
		V_{CC} = 5.5 V	--	--	5	--	6	ns
C_{PD}	power dissipation capacitance	C_L = 15 pF; f = 1 MHz; V_I = GND to V_{CC} [3]	--	18	--	--	--	pF

Note:

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

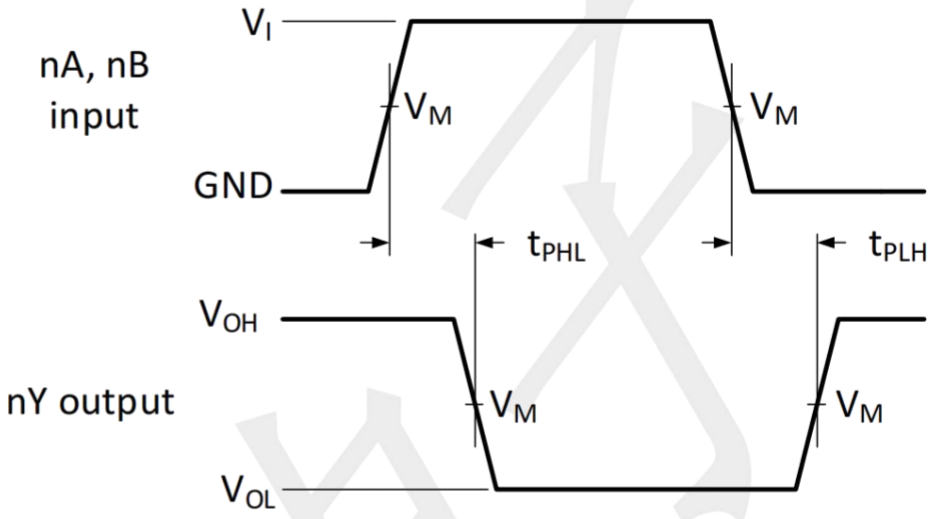
f_o = output frequency in MHz;

C_L = output load capacitance in pF; V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

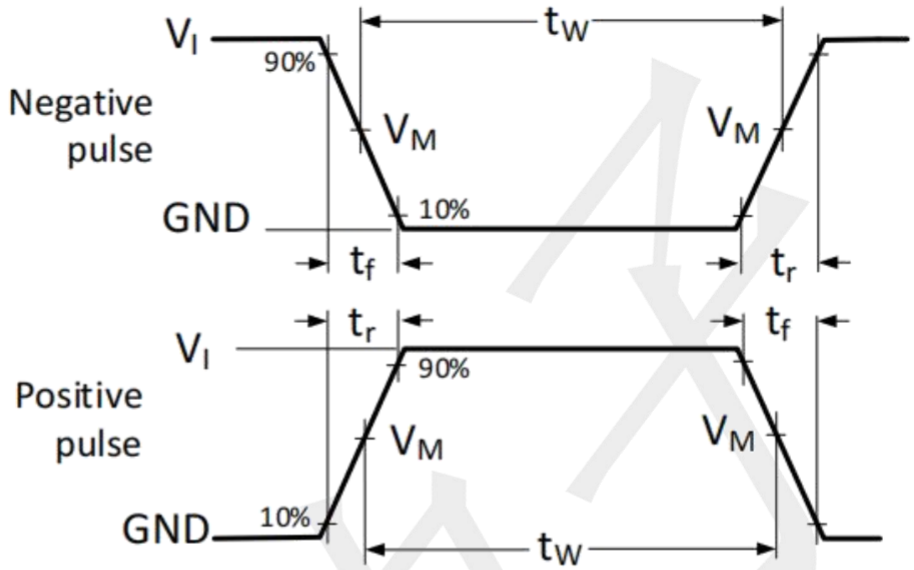
Waveforms and test circuit

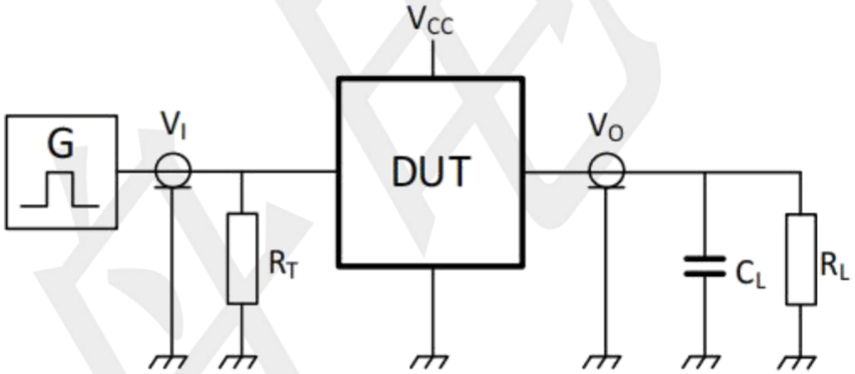


Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Measurement points

Supply voltage	Input	Output
Vcc	**VM**	**VM**
2.0 V	0.5Vcc	0.5Vcc
4.5 V	1.5 V	1.5 V
5.5 V	0.5Vcc	0.5Vcc





Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Test data

Supply voltage	Input		Load	
V_{CC}	V_I	$t_r = t_f$	C_L	R_L
2.0 V	V_{CC}	≤ 2.0 ns	15 pF	500 Ω
4.5 V	3 V	≤ 2.0 ns	15 pF	500 Ω
5.5 V	V_{CC}	≤ 2.0 ns	15 pF	500 Ω

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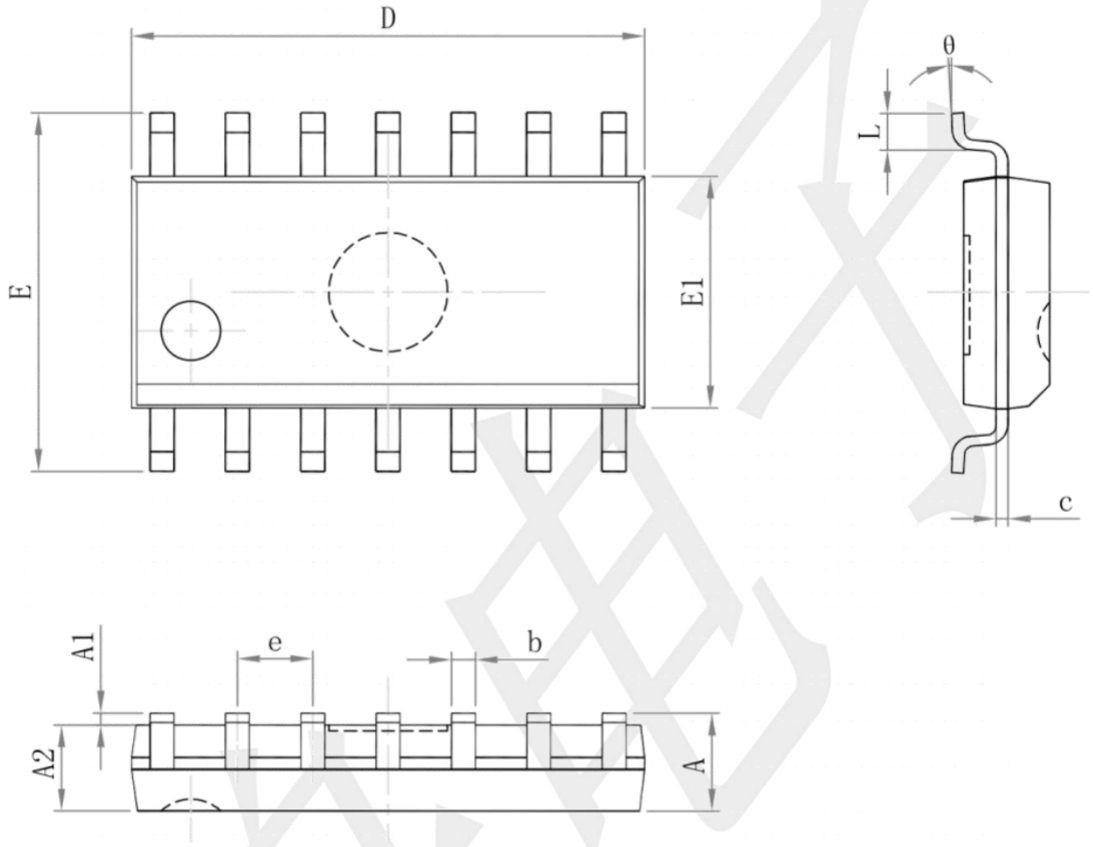

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.750	— —	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	— —	0.049	— —
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°