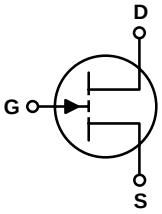
# INN100W110D

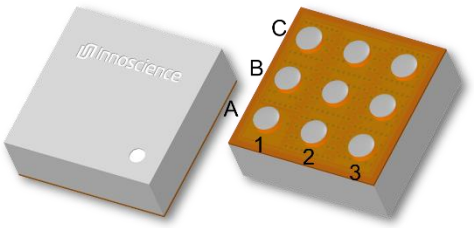
## 1. General Description

**GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in WLCSP with 1.5 mm x 1.5 mm package size.**




## 2. Features

- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Ultra-low on resistance
- Very small package size
- Zero reverse recovery charge




Top view Bottom view

## 3. Applications

- High Power Density DC-DC Converters
- Class-D Audio
- High Intensity Headlamps

## 4. Key Performance Parameters

**Table 1 Key performance parameters at $T_J$ = 25 ˚C**

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS,max}$ | 100 | V |
| $R_{DS(on),typ}$ @ $V_{GS}$ = 5 V | 8.5 | mΩ |
| $R_{DS(on),max}$ @ $V_{GS}$ = 5 V | 11 | mΩ |
| $Q_{G,typ}$ @ $V_{DS}$ = 50V | 2.3 | nC |
| $I_{DS,Pulse}$ ($T_J$ = 25 ˚C) | 105 | A |
| $Q_{OSS}$ @ $V_{DS}$ = 50 V | 13 | nC |

## 5. Pin Information

**Table 2 Pin information**

| PIN | Pin Description | Pin Function |
|---|---|---|
| A1 | Gate | Driver Gate |
| A2/B2/C2 | Drain | Power Drain |
| B1/C1/A3/B3/C3 | Source | Power Source |

**Table 3 Ordering information**

| Type/Ordering Code | Package | Product Code |
|---|---|---|
| INN100W110D | WLCSP 1.5x1.5 | J59 |

## Table of Contents

1. General Description ..... 1
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3. Applications ..... 1
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## 6. Maximum Ratings

at $T_J$ = 25 ˚C unless otherwise specified.

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscience sales office.

**Table 4 Maximum ratings**

| SYMBOL | PARAMETER | MAX | UNIT |
|---|---|---|---|
| $V_{DS}$ | Drain-to-Source Voltage | 100 | V |
| $V_{DS(tr)}$ | Drain-to-Source Voltage [1] ($V_{GS}$ = 0 V, 1h total time, $T_A = T_{JMAX}$) | 120 | V |
| $I_D$ | Continuous Current ($V_{GS}$ = 5 V, $T_C$ = 25 ˚C，$R_{\theta JC}$ = 1.9 ˚C/W) | 54 | A |
| | Continuous Current ($V_{GS}$ = 5 V, $T_C$ = 100 ˚C，$R_{\theta JC}$ = 1.9 ˚C/W) | 34 | A |
| | Continuous Current ($V_{GS}$ = 5 V, $T_C$ = 25 ˚C，$R_{\theta JC}$ = 4.33 ˚C/W) | 35 | A |
| | Continuous Current ($V_{GS}$ = 5 V, $T_C$ = 100 ˚C，$R_{\theta JC}$ = 4.33 ˚C/W) | 20 | A |
| | Continuous Current ($V_{GS}$ = 5 V, $T_A$ = 25 ˚C，$R_{\theta JA}$ = 65.88 ˚C/W) | 9 | A |
| | Pulsed ($V_{GS}$ = 5 V, $T_J$ = 25 ˚C, $T_{Pulse}$ = 100 µs) | 105 | A |
| | Pulsed ($V_{GS}$ = 5 V, $T_J$ = 150 ˚C, $T_{Pulse}$ = 100 µs) | 80 | A |
| $V_{GS}$ | Gate-to-Source Voltage | 6 | V |
| | Gate-to-Source Voltage | -4 | V |
| $V_{GS(tr)}$ | Gate-to-Source Voltage [1] ($V_{DS}$ = 0 V, 168h total time, $T_A = T_{JMAX}$) | 6.5 | V |
| $P_{tot}$ | Power Dissipation ($V_{GS}$ = 5 V, $T_C$ =25˚C，$R_{\theta JC}$ = 1.9 ˚C/W) | 65.8 | W |
| | Power Dissipation ($V_{GS}$ = 5 V, $T_A$ =25˚C，$R_{\theta JA}$ = 65.88 ˚C/W) | 1.86 | W |
| $T_J$ | Operating Temperature | -40 to 150 | ˚C |
| $T_{STG}$ | Storage Temperature | -40 to 150 | ˚C |

Note:

1. Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation.

## 7. Thermal Characteristics

**Table 5 Thermal characteristics**

| SYMBOL | PARAMETER | TYP | UNIT | Note/Test Condition |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 1.9 | ˚C/W | - |
| $R_{\theta JB}$ | Thermal Resistance, Junction to Board | 4.33 | ˚C/W | - |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient [2] | 65.88 | ˚C/W | - |
| $T_{sold}$ | Maximum Reflow Soldering Temperature | 260 | ˚C | MSL3 |

Note:

2. $R_{\theta JA}$ is determined with the device on FR4 PCB (2s2p with thermal vias) defined in accordance with JEDEC standards. PCB is mounted in horizontal position without air stream cooling.

## 8. Electric Characteristics

at $T_J$ = 25 °C unless otherwise specified.

**Table 6 Static characteristics**

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| $I_{DSS}$ | Drain Source Leakage | - | 2 | 100 | μA | $V_{GS}$ = 0 V, $V_{DS}$ =100 V |
| | Drain Source Leakage ($T_J$ = 125 ˚C) | - | 5 | - | μA | $V_{GS}$ = 0 V, $V_{DS}$ =100 V |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | - | 2 | 100 | μA | $V_{GS}$ = 6 V |
| | Gate-to-Source Forward Leakage ($T_J$ = 125 ˚C) | - | 10 | - | μA | $V_{GS}$ = 6 V |
| | Gate-to-Source Reverse Leakage | - | 0.2 | 10 | μA | $V_{GS}$ = -4 V |
| $V_{GS(TH)}$ | Gate Threshold Voltage [3] | 0.8 | 1.1 | 2.1 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 2.2 mA |
| $R_{DS(on)}$ | Drain-Source On-State Resistance [3] | - | 8.5 | 11 | mΩ | $V_{GS}$ = 5 V, $I_D$ = 2.5 A |
| $V_{SD}$ | Source-Drain Forward Voltage | - | 2.4 | - | V | $I_S$ = 11 A, $V_{GS}$ = 0 V |

Note:

3. $V_{GS(TH)}$ and $R_{DS(on)}$ are measured without prior drain bias or switching stress.

**Table 7 Dynamic characteristics [4]**

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|
| $C_{ISS}$ | Input Capacitance | - | 280 | - | pF | $V_{GS}$ = 0 V, $V_{DS}$ = 50 V |
| $C_{OSS}$ | Output Capacitance | - | 125 | - | | $V_{GS}$ = 0 V, $V_{DS}$ = 50 V |
| $C_{RSS}$ | Reverse Transfer Capacitance | - | 2.3 | - | | $V_{GS}$ = 0 V, $V_{DS}$ = 50 V |
| $C_{OSS(ER)}$ | Energy Related $C_{OSS}$ | - | 175 | - | | $V_{GS}$ = 0 V, $V_{DS}$ = 0 V to 50 V |
| $C_{OSS(TR)}$ | Time Related $C_{OSS}$ | - | 255 | - | | $V_{GS}$ = 0 V, $V_{DS}$ = 0 V to 50 V |
| $R_G$ | Gate Resistance | - | 1.3 | - | Ω | f= 5 MHz, open drain |
| $Q_G$ | Total Gate Charge | - | 2.3 | - | nC | $V_{GS}$ = 5 V, $V_{DS}$ = 0 V to 50 V, $I_D$= 11 A |
| $Q_{GS}$ | Gate to Source Charge | - | 0.6 | - | | $V_{GS}$ = 5 V, $V_{DS}$ = 0 V to 50 V, $I_D$ = 11 A |
| $Q_{GD}$ | Gate to Drain Charge | - | 0.4 | - | | $V_{GS}$ = 5 V, $V_{DS}$ = 0 V to 50 V, $I_D$ = 11 A |
| $V_{Plat}$ | Gate Plateau Voltage | - | 2.1 | - | V | $I_D$ = 11 A, $V_{DS}$ = 50 V, $V_{GS}$ = 0 V to 5 V |
| $Q_{G(TH)}$ | Gate Charge at Threshold | - | 0.3 | - | nC | $V_{GS}$ = 5 V, $V_{DS}$ = 0 V to 50 V, $I_D$ = 11 A |
| $Q_{OSS}$ | Output Charge | - | 13 | - | | $V_{GS}$ = 0 V, $V_{DS}$ = 0 V to 50 V |
| $Q_{RR}$ | Reverse Recovery Charge | - | 0 | - | | $V_{DS}$ = 50 V, $I_S$ = 11 A |

Note:

4. Guaranteed by design.

## 9. Electric Characteristics Diagrams

at $T_J$ = 25 °C, unless specified otherwise.

Fig. 1 Typ. Output Characteristics ($T_J$ = 25 ˚C)

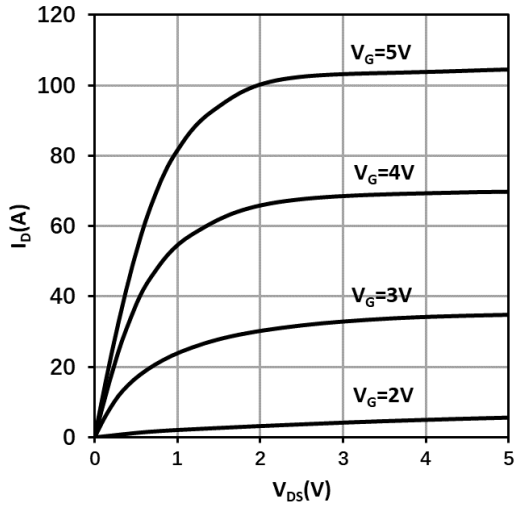



Fig. 2 Typ. Output Characteristics ($T_J$ = 125 ˚C)

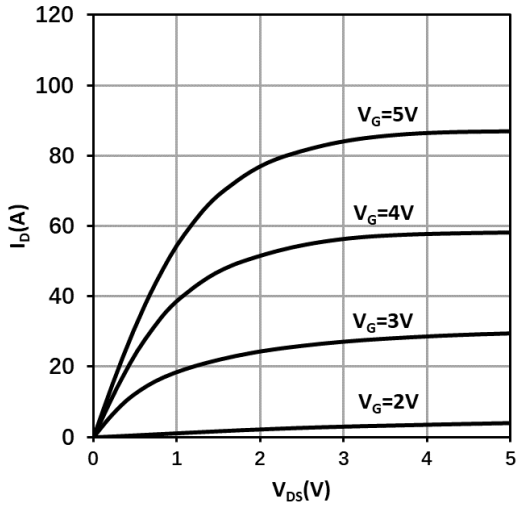



Fig. 3 Typ. Drain On-State Resistance ($T_J$ = 25 ˚C)

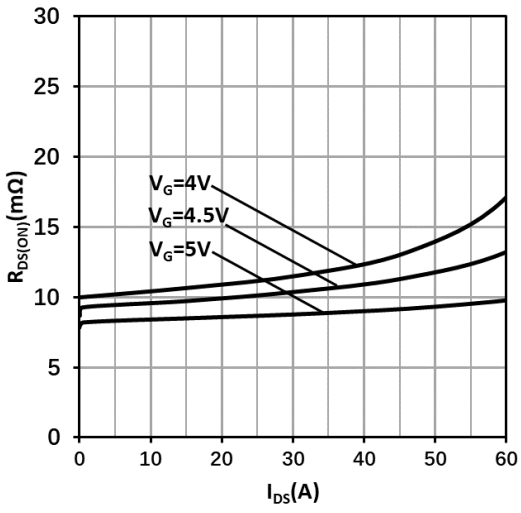



Fig. 4 Typ. Drain On-State Resistance ($T_J$ = 125 ˚C)

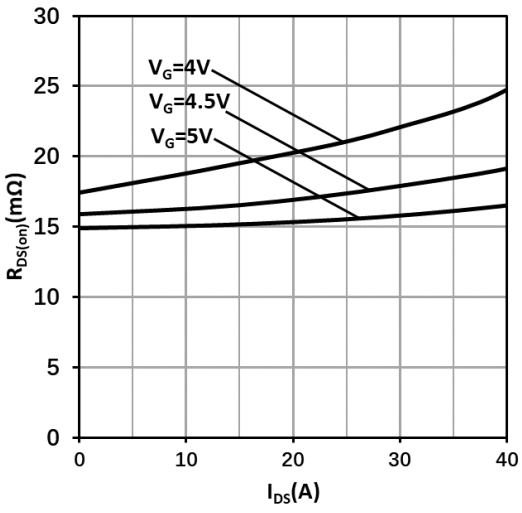


Fig. 5 Normalized On-State Resistance vs. Temp.

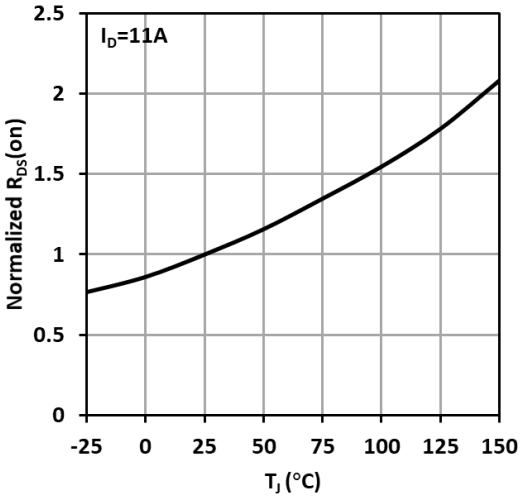



Fig. 6 Typ. Transfer Characteristics

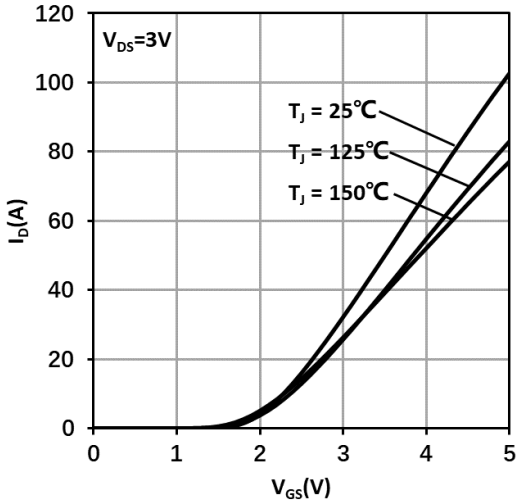



Fig. 7 Typ. Reverse Drain-Source Characteristics ($V_{GS} \leq 0, T_J = 25\ ^\circ C$)

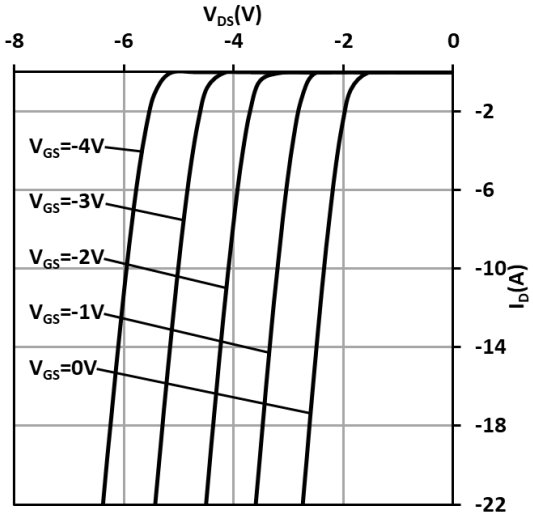



Fig. 8 Typ. Reverse Drain-Source Characteristics ($V_{GS} \geq 0, T_J = 25\ ^\circ C$)

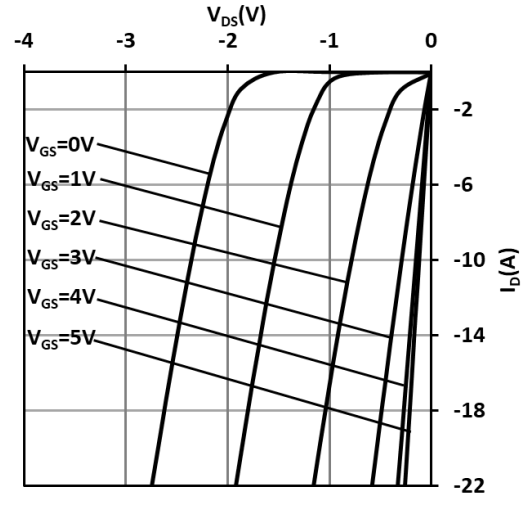


Fig. 9 Typ. Reverse Drain-Source Characteristics ($V_{GS} \leq 0$, $T_J$ = 125 ˚C)

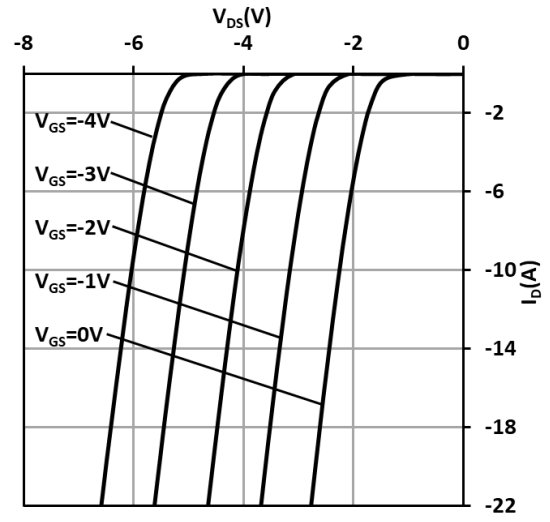



Fig. 10 Typ. Reverse Drain-Source Characteristics ($V_{GS} \geq 0$, $T_J$ = 125 ˚C)

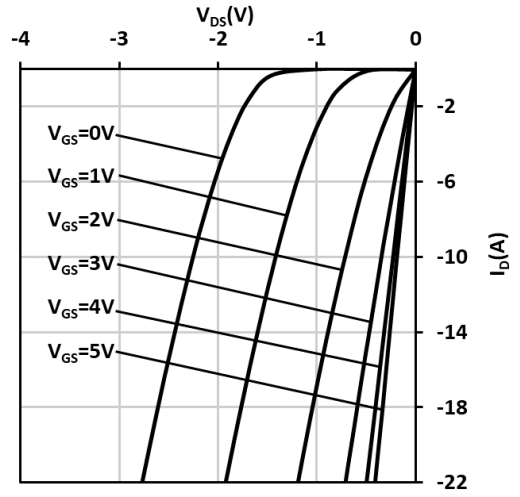



Fig. 11 Typ. Capacitances Characteristics

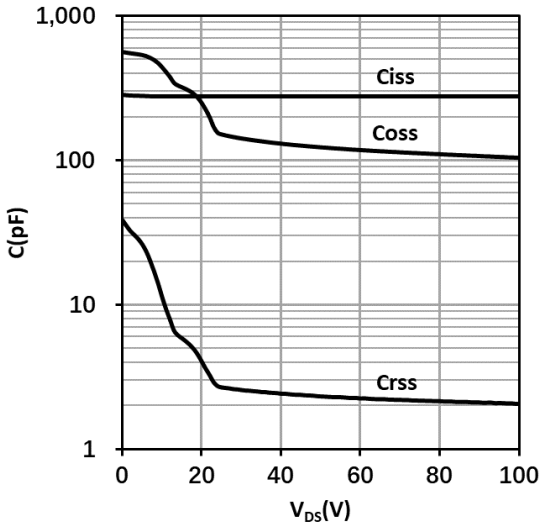



Fig. 12 Typ. Gate Charge

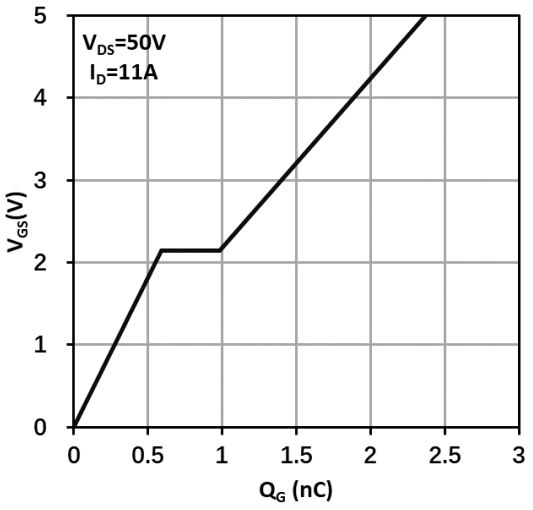


Fig. 13 Normalized Threshold Voltage vs. Temp.

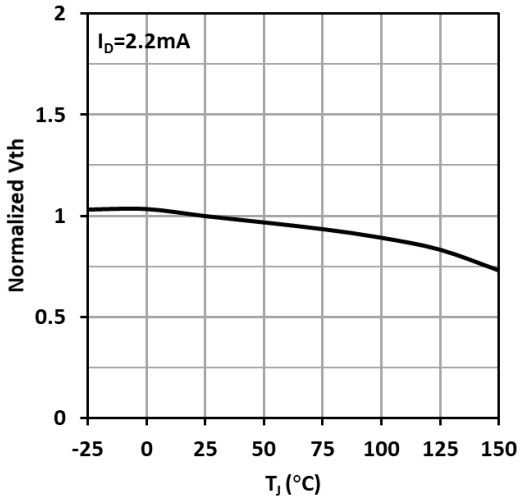



Fig. 14 Typ. Output Charge

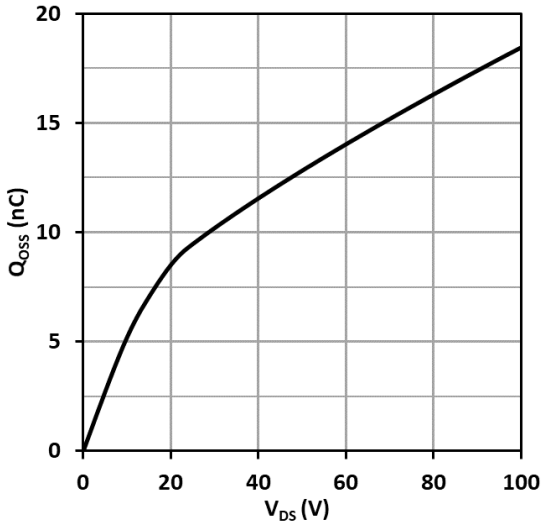



Fig. 15 Typ. Output Capacitance Stored Energy

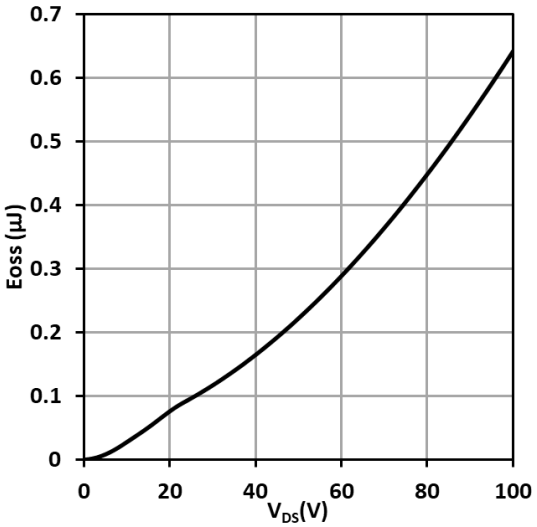



Fig. 16 Power Dissipation $P_{tot} = f(T_C)$, $R_{\theta JC}$ = 1.9˚C/W

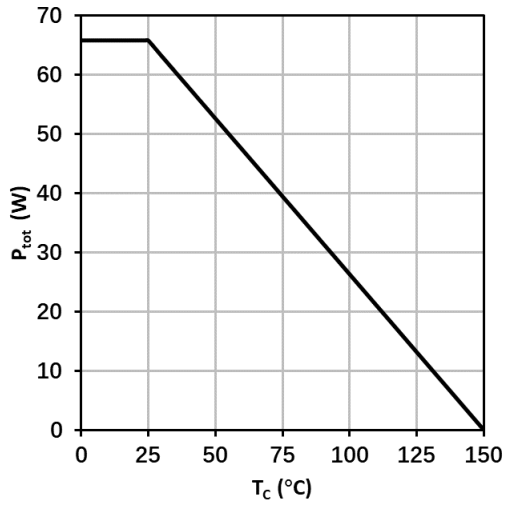


Fig. 17 Power Dissipation Ptot = f($T_A$), $R_{\theta JA}$ =65.88 ˚C/W

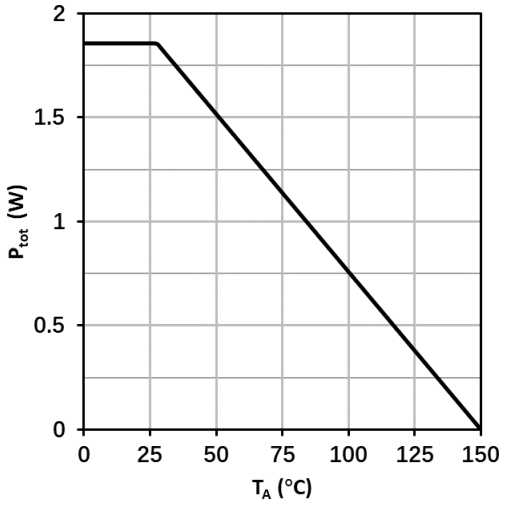



Fig. 18 Typ. Gate-to-Source Leakage Characteristics
$I_G$ = f($V_{GS}$); Drain Open

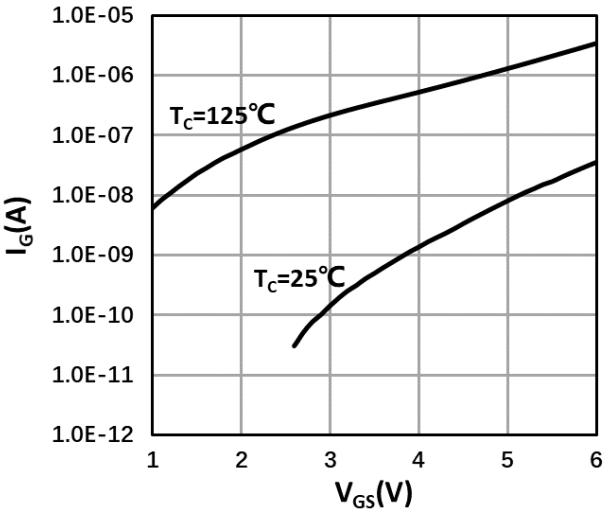



Fig. 19 Typ. Drain-Source Leakage Characteristics
$I_{DSS}$ = f($V_{DS}$); $V_{GS}$ = 0 V

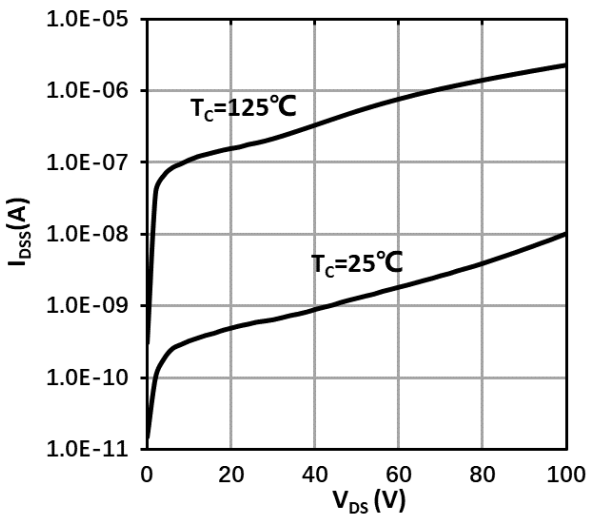



Fig. 20 Safe Operating Area
$I_D$ = f($V_{DS}$); $T_C$ = 25 ˚C; Single Pulse; Parameter: $t_p$

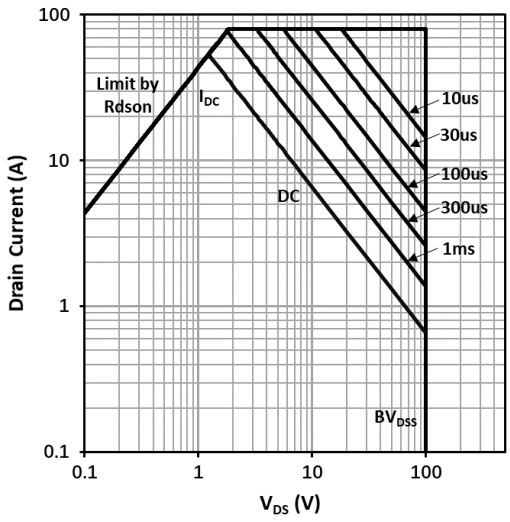


Fig. 21 Safe Operating Area
$I_D = f(V_{DS})$; $T_C$ = 125 ˚C; Single Pulse; Parameter: $t_p$

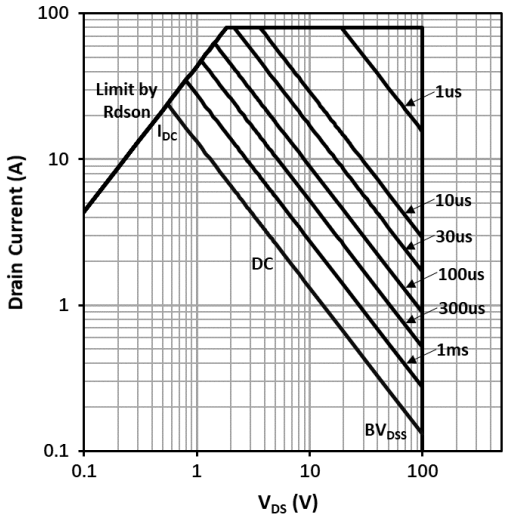
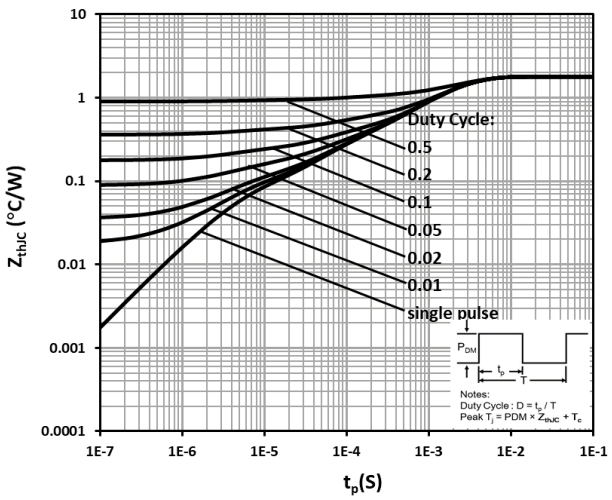
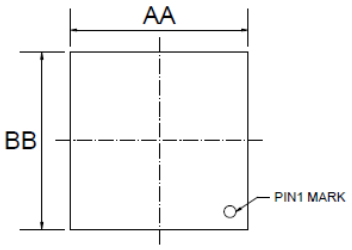



Fig. 22 Max. Transient Thermal Impedance
$Z_{thJC} = f(t_p)$; Parameter: $D=t_p/T$

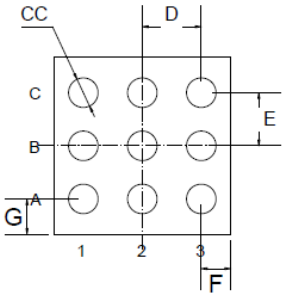


## 10. Package outlines

### Package Reference

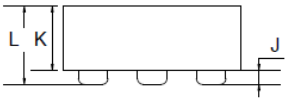



TOP VIEW




BOT VIEW

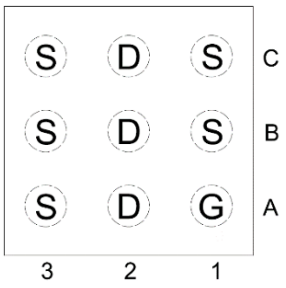
| SYMBOL | MILLIMETER | | | NOTE |
|---|---|---|---|---|
| | MIN | NOM | MAX | |
| AA | 1.475 | 1.500 | 1.525 | |
| BB | 1.475 | 1.500 | 1.525 | |
| CC | 0.230 | 0.250 | 0.270 | 9X |
| D | 0.500 BASIC | | | 6X |
| E | 0.450 BASIC | | | 6X |
| F | 0.250 REF | | | 6X |
| G | 0.300 REF | | | 6X |
| J | 0.083 | 0.103 | 0.123 | |
| K | 0.546 | 0.560 | 0.574 | |
| L | 0.626 | 0.663 | 0.700 | |




SIDE VIEW

NOTE:
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.05 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-221.
4) DRAWING IS NOT TO SCALE.
5) Bump Structure：65umCu+3umNi+35umSnAg
6) A1 is Gate;
A3/B1/B3/C1/C3 is Source;
A2/B2/C2 is Drain.

### Pin Configuration




TOP VIEW

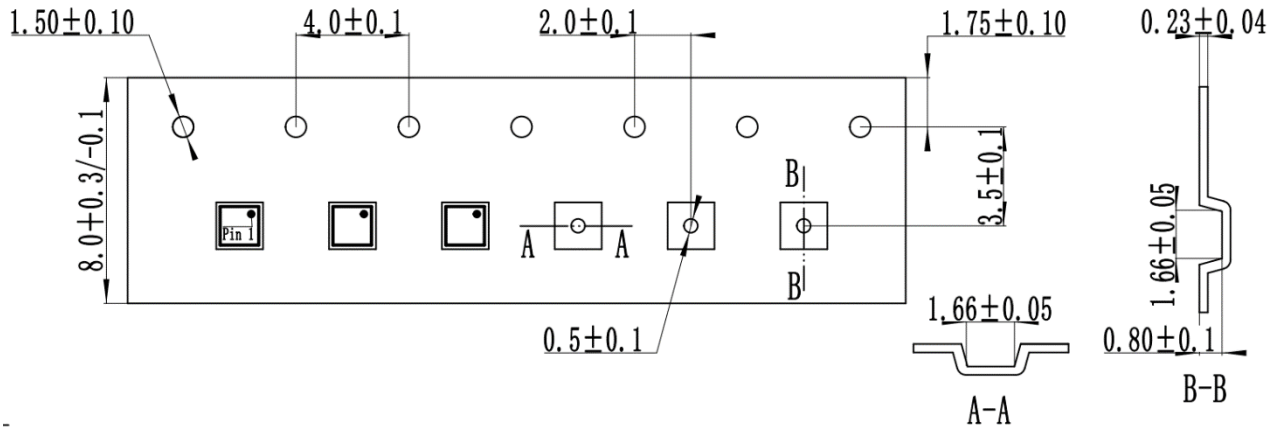
### Marking Reference



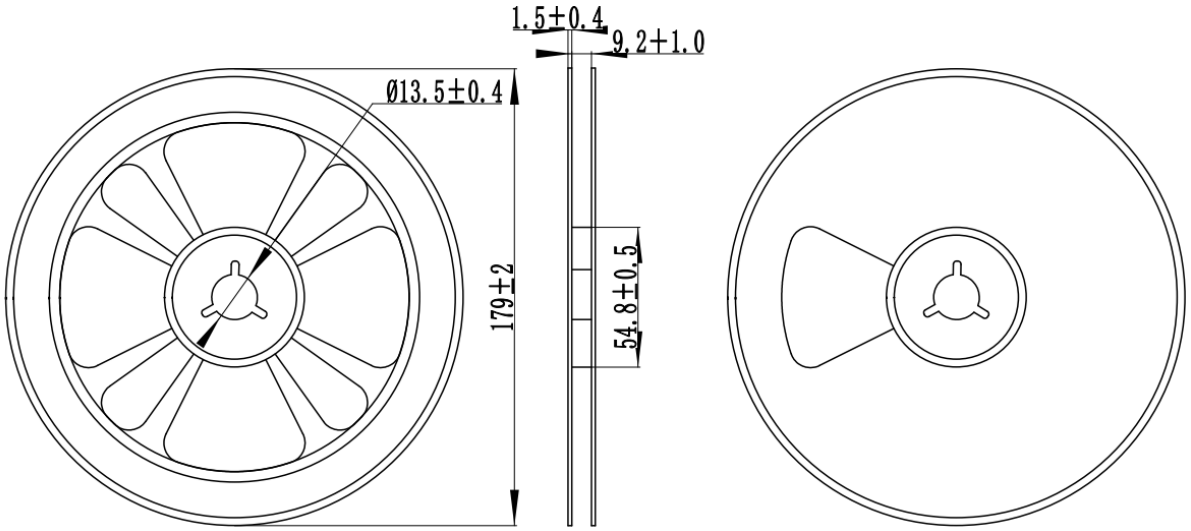

TOP VIEW

| Column | Description | Example |
|---|---|---|
| Col 1 | Company name | INN |
| Col 2 | Product code | XXX |
| Col 3 | Lot Code | XXXXXX |
| Col 4 | Date code | YYWW |
| Col 5 | Wafer ID | XX |
| Col 6 | Location ID | XXXYYY |

## 11. Reel Information

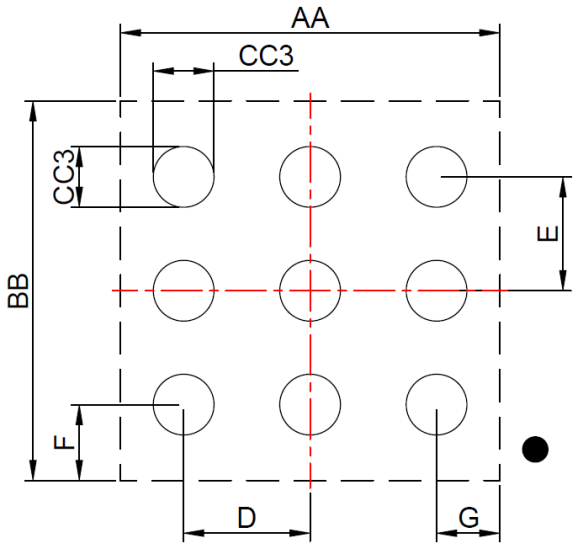



Notes:
(1)The cumulative error of any 10 sprocket holes shall not exceed ± 0.20mm;
(2)The material thickness shall be measured based on the edge of the carrier tape;
(3)The unspecified tolerance is ± 0.1mm, and R<0.3mm is not specified;
(4)The unmarked demolding slope is 5 ° ;
(5)Surface Resistivity: 1*10 e 5 Ω/Δ ~ 1*11 e11



## 12. Land Pattern

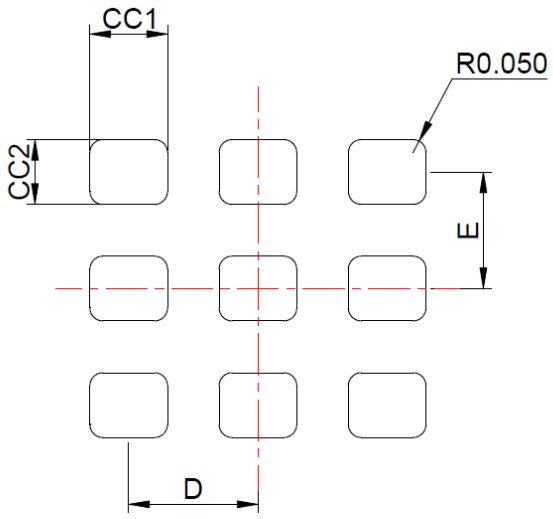
### Recommended Land Pattern




TOP VIEW

| SYMBOL | MILLIMETER | NOTE |
|---|---|---|
| AA | 1.50 | |
| BB | 1.50 | |
| CC3 | 0.24 | 9X |
| D | 0.50 | 6X |
| E | 0.45 | 6X |
| F | 0.30 | 6X |
| G | 0.25 | 6X |

### Recommended Stencil Drawing




TOP VIEW

| SYMBOL | MILLIMETER | NOTE |
|---|---|---|
| CC1 | 0.30 | 9X |
| CC2 | 0.25 | 9X |
| D | 0.50 | 6X |
| E | 0.45 | 6X |

## 13. Revision History

**Major changes since the last revision**

| Revision | Date | Description of changes |
|---|---|---|
| 1.0 | 2026-05-07 | Version 1.0 Setup |

## Important Notice

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