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Product Specification

XBLW TLV349x

Ultra-Low Power 310nA, 1.7V, RRI, CMOS Input Comparators

WEB | www.xinboleic.com



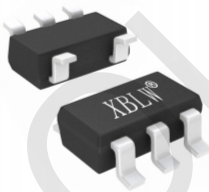
Descriptions

The TLV3491/3492/3494 devices are single-, dual-, and quad- channel comparators with push-pull output that are ideal for power-sensitive, low-voltage applications. Featuring a nano-power (typical 310 nA), fast 12 µs propagation delay, and a wide range of supply voltages from 1.7 V to 5.5 V with rail-to-rail common -mode voltage range makes the TLV3491/3492/3494 an ideal choice for a wide variety of portable electronics applications, such as handsets, tablets, notebooks and portable devices that have extremely power constraints and tight board space.

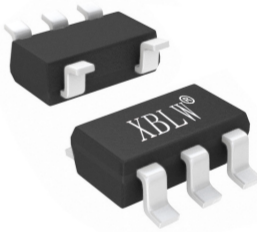
The output of the TLV3491/3492/3494 pulls to within 0.1 V of either supply rail without external pull-up circuitry, making these devices ideal for interface with both CMOS and TTL logics. All input and output pins can tolerate a continuous short-circuit fault condition to either rail. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

Features

- Nanopower Operating Current (310 nA) Preserves Battery Power
- Propagation Delay: 12 µs (100 mV Overdrive)
- Rail-to-Rail Input
- Push-Pull Output Current Drive: 30 mA Typically at 5V Supply
- Internal Hysteresis for Clean Switching
- Internal RF/EMI Filter
- Single 1.7 V to 5.5 V Supply Voltage Range
  – Can be Powered From the Same 1.8V/2.5V/3.3V/5V System Rails
- Operating Temperature Range: -40 °C to +85 °C



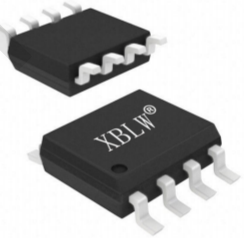
SC70-5



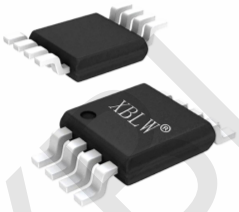
SOT23–5

Applications

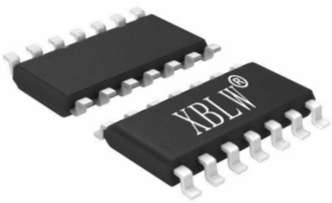
- Handsets, Tablets and Notebooks
- Wearables and Consumer Accessories
- Portable Medical Instruments
- Alarms and Monitoring Circuits
- Level Detectors
- IR Receivers
- Multi-vibrators



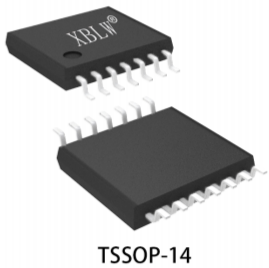
SOP-8



MSOP-8



SOP–14



TSSOP-14

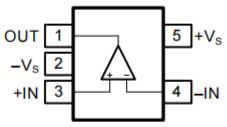
Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW TLV3491AIDCKR	SC70-5	VBNI	Tape	3000Pcs/Reel
XBLW TLV3491AIDBVR	SOT23-5	VBNI	Tape	3000Pcs/Reel
XBLW TLV3492AIDR	SOP-8	TLV3492	Tape	4000Pcs/Reel
XBLW TLV3492AIDGKR	MSOP-8	V3492	Tape	3000Pcs/Reel
XBLW TLV3494AIDR	SOP-14	TLV3494	Tape	2500Pcs/Reel
XBLW TLV3494AIPWR	TSSOP-14	TLV3494	Tape	3000Pcs/Reel

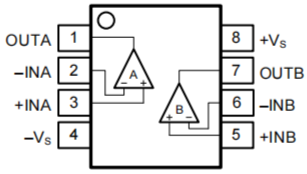
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Pin Configurations (Top View)

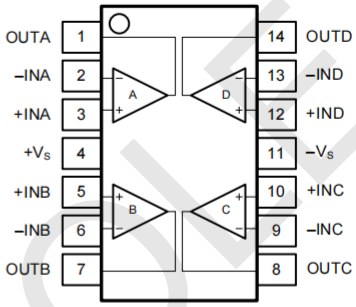
TLV3491
SOT23-5/ SC70-5



TLV3492
SOP-8/ MSOP-8



TLV3494
SOP-14/ TSSOP-14



Pin Description

Symbol	Description
–IN	Negative input. The voltage range is from (V_{S-} – 0.1V) to (V_{S+} + 0.1V).
+IN	Positive input. This pin has the same voltage range as –IN.
$+V_S$	Positive power supply. The voltage is from 1.7V to 5.5V. Split supplies are possible as long as the voltage between V_{S+} and V_{S-} is from 1.7V to 5.5V.
$–V_S$	Negative power supply. It is normally tied to ground. It can also be tied to a voltage other than ground as long as the voltage between V_{S+} and V_{S-} is from 1.7V to 5.5V.
OUT	Comparator output.

ESD Rating

Parameter	Item	Value	Unit
Electrostatic Discharge Voltage	Human body model (HBM), per MIL-STD-883J / Method 3015.9	±5000	V
	Charged device model (CDM), per ESDA/JEDEC JS-002-2014	±2000	
	Machine model (MM), per JESD22-A115C	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Absolute Maximum Ratings（TA=25℃)

Parameter	Absolute Maximum Rating
Supply Voltage, V_{S+} to V_{S-}	8.0 V
Signal Input Terminals: Voltage, Current	V_{S-} – 0.3 V to V_{S+} + 0.3 V, ±10 mA
Output Short-Circuit	Continuous
Storage Temperature Range, T_{stg}	–65 °C to +150 °C
Junction Temperature, T_J	150 °C
Lead Temperature Range (Soldering 10 sec)	260 °C

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter	MIN	MAX	UNIT
Supply voltage,VS	1.7	5.5	V
Specified temperature	–40	85	°C

Electrical Characteristics

V_S= 5. 0V, T_A= +25°C, unless otherwise noted.
Boldface limits apply over the specified temperature range, TA = -40 to +85 °C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_{CM} = 0		±0.5	±3.5	mV
		T_A = -40 to +85 °C			±4.0	
V_{OS}TC	Offset voltage drift	T_A = -40 to +85 °C		±1		µV/°C
PSRR	Power supply rejection ratio	V_S = 1.7 to 5.5 V, V_{CM} < (V_{S+} -1V)	65	85		dB
		TA = -40 to +85°C	60			
V_{HYST}	Input hysteresis	V_{CM} = 0		5		mV
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = VS /2		5		pA
		T_A = +85 °C		150		
I_{OS}	Input offset current	V_{CM} = V_S /2		10		pA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		V_{S-}–0.1		V_{S+}+0.1	V
CMRR	Common-mode rejection ratio	V_{CM} =-0.1 to 5.1 V	62	84		dB
		V_{CM} = 0 to 4.8 V, T_A =-40 to+85 °C	56			
		V_S= 1.8 V, V_{CM} =-0.1 to 1.9 V	60	82		
		V_{CM}=0 to 1.6 V, TA =-40 to+85 °C	55			
INPUT IMPEDANCE						
R_{IN}	Input resistance		100			GΩ
C_{IN}	Input capacitance	Differential		2.0		pF
		Common mode		3.5		
OUTPUT						
V_{OH}	High output voltage swing	I_{SOURCE} = 1 mA	V_{S+}–90	V_{S+}–73		mV
		T_A = -40 to +85 °C	V_{S+}–120			

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Electrical Characteristics (continued)

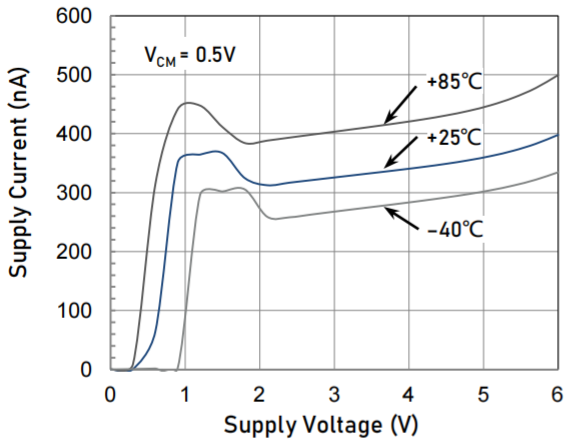
V_S= 5. 0V, T_A= +25°C, unless otherwise noted.
Boldface limits apply over the specified temperature range, TA = -40 to +85 °C.

V_{OL}	Low output voltage swing	I_{SINK} = 1 mA		V_S – +48	V_S – +60	mV
		T_A = -40 to +85 °C			V_S – +80	
I_{SC}	Output short-circuit current	Source current, OUT to V_S /2	30	36		mA
		Sink current, OUT to V_S /2		–27	–22	
POWER SUPPLY						
V_S	Operating supply voltage	T_A =-40 to +85 °C	1.7		5.5	V
I_Q	Quiescent current (per comparator)	V_S = 1.8 V, V_{CM} = 0.3V		310		nA
		V_S = 1.8 V, V_{CM} = 1.5V		380		
		V_S = 5.0 V, V_{CM} = 0.3V		355		
		V_S = 5.0 V, V_{CM} = 4.7V		440	670	
SWITCHING CHARACTERISTICS						
t_{PD+}	Propagation delay time, Low to high	Input overdrive = 10 mV, C_L = 15 pF		16		µs
		Input overdrive = 100 mV, C_L = 15 pF		12		
t_{PD-}	Propagation delay time, High to low	Input overdrive = 10 mV, C_L = 15 pF		17		µs
		Input overdrive = 100 mV, C_L = 15 pF		13		
t_R	Rise time	Input overdrive = 10 mV, C_L = 15 pF		230		ns
		Input overdrive = 100 mV, C_L = 15 pF		190		
t_F	Fall time	Input overdrive = 10 mV, C_L = 15 pF		300		ns
		Input overdrive = 100 mV, C_L = 15 pF		220		
THERMAL CHARACTERISTICS						
T_A	Operating temperature range		-40		+85	°C
θ_{JA}	Package Thermal Resistance	SC70-5		333		°C/W
		SOT23-5		190		
		MSOP-8		216		
		SOP-8		125		
		TSSOP-14		112		
		SOP-14		115		

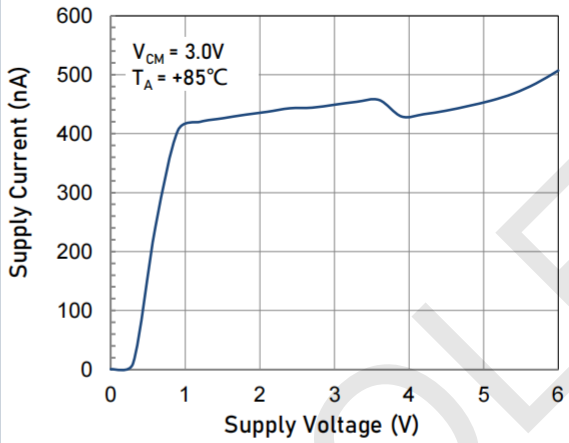
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Typical Performance Characteristics

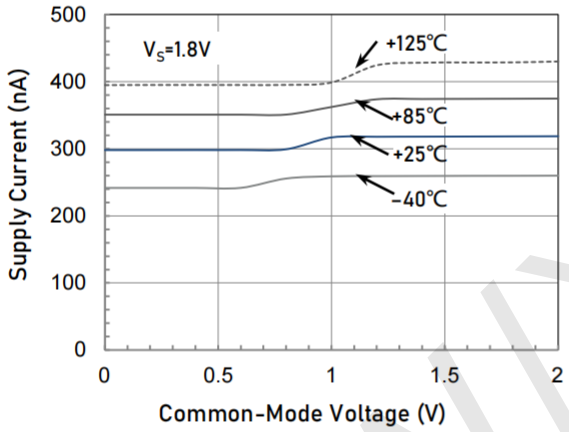
At T_A=+25℃, V_S=5. 0V, V_{CM}=V_S/2, R_L=10kΩ, and C_L=15pF, unless otherwise noted.



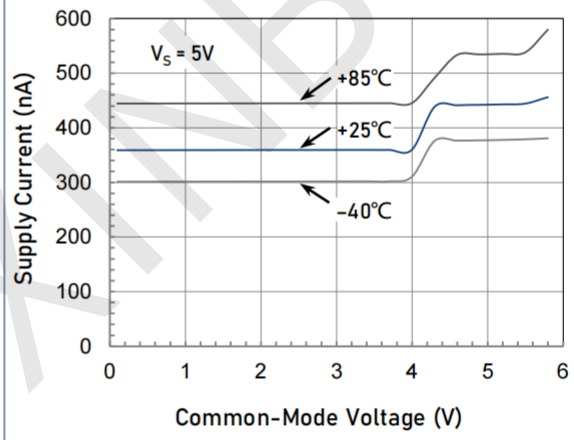
Supply Current vs. Supply Voltage



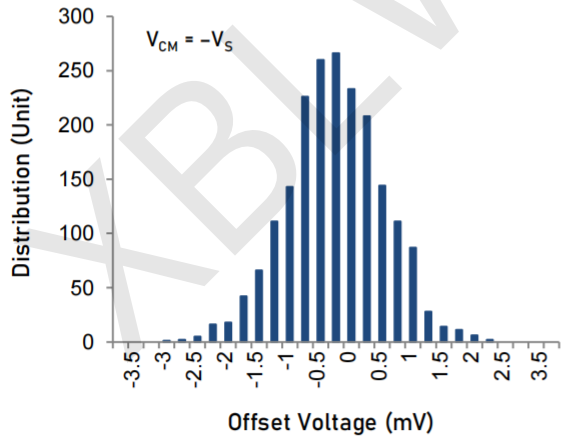
Supply Current vs. Supply Voltage



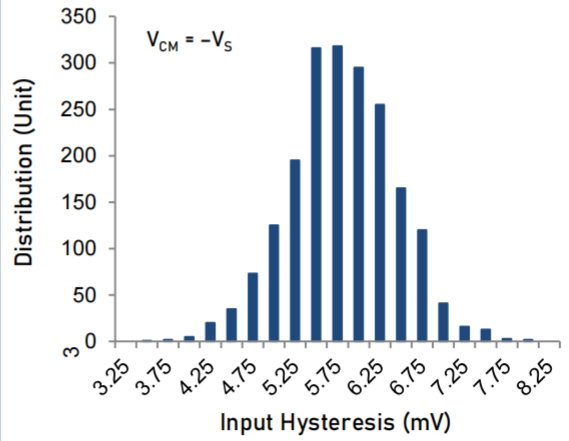
Supply Current vs. Common-Mode Input (V_S = 1.8V)



Supply Current vs. Common-Mode Input (V_S = 5.0V)



Offset Voltage Production Distribution

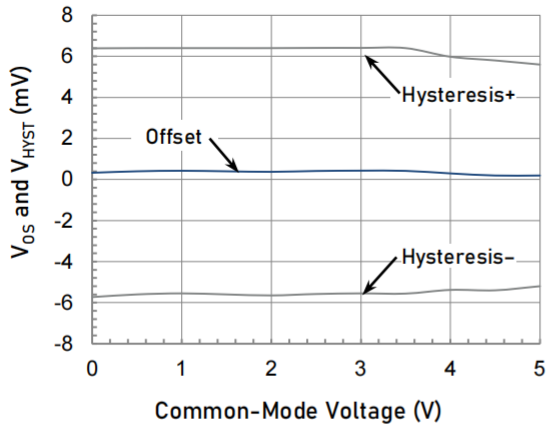


Hysteresis Production Distribution

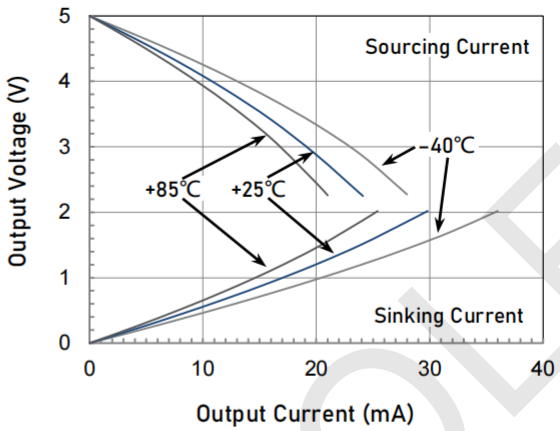
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Typical Performance Characteristics

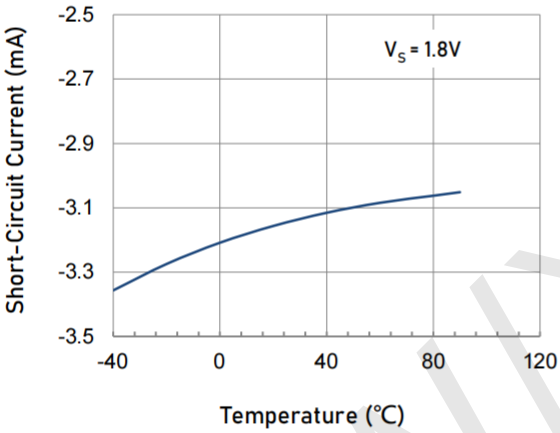
At T_A=+25℃, V_S=5. 0V, V_{CM}=V_S /2, R_L=10kΩ, and C_L=15pF, unless otherwise noted.



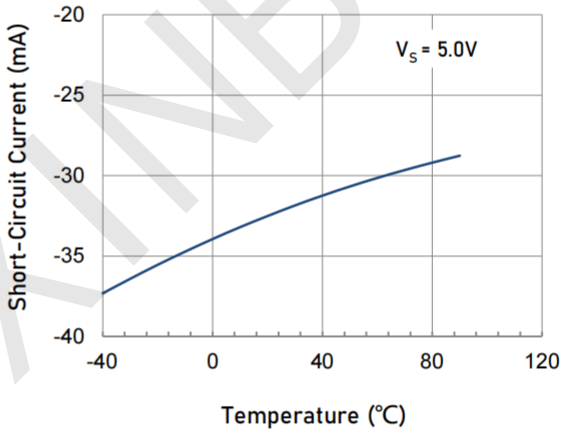
V_{OS} and V_{HYST} vs. Common-Mode Input



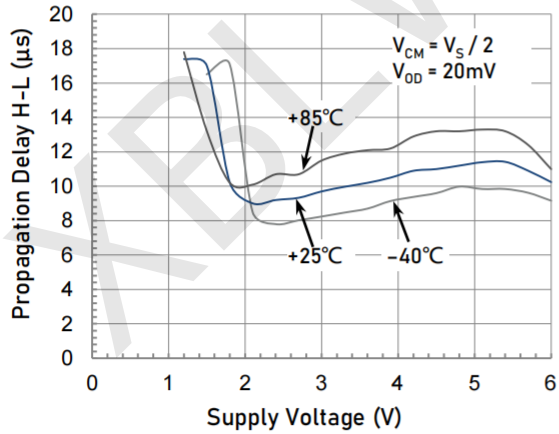
Output Voltage vs. Output Current



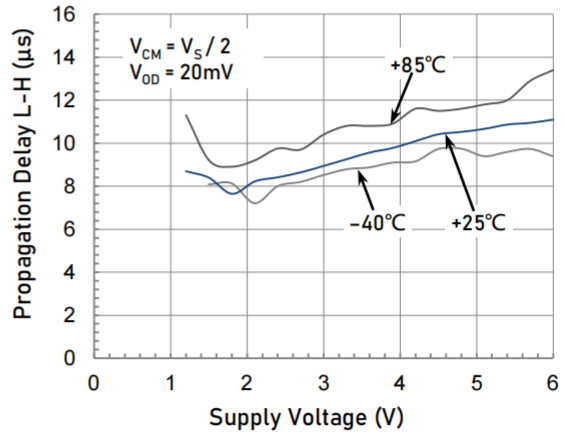
Short-Circuit Current vs. Temperature (V_S = 1.8V)



Short-Circuit Current vs. Temperature (V_S = 5.0V)



Propagation Delay H-L (t_{PD-}) vs. Supply Voltage

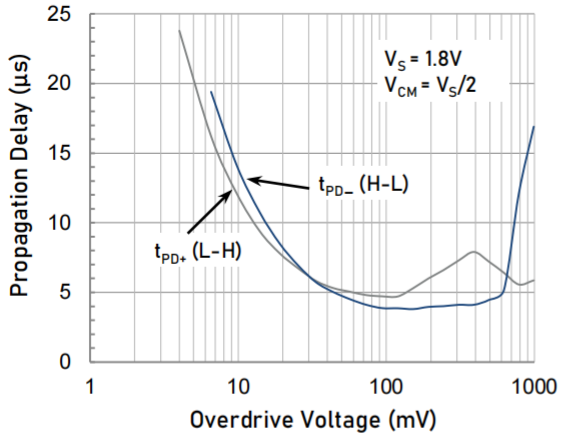


Propagation Delay L-H (t_{PD+}) vs. Supply Voltage

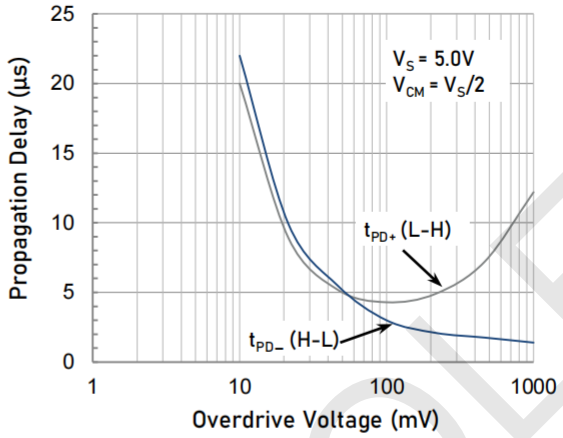
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Typical Performance Characteristics

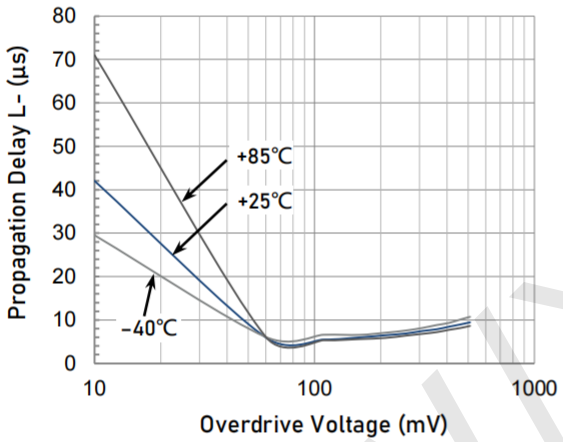
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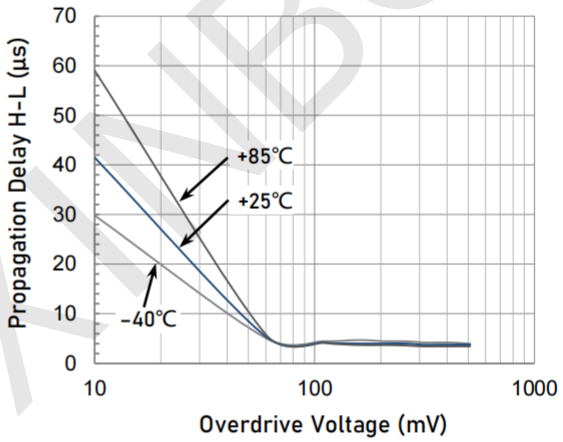
Propagation Delay vs. Input Overdrive (V_S = 1.8V)



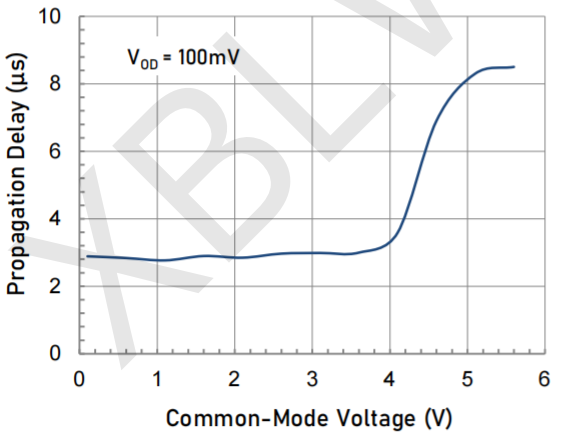
Propagation Delay vs. Input Overdrive (V_S = 5.0V)



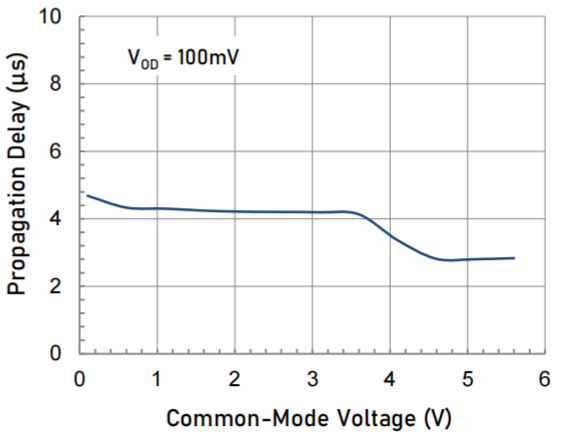
Propagation Delay H-L (t_{PD-}) vs. Input Overdrive



Propagation Delay L-H (t_{PD+}) vs. Input Overdrive



Propagation Delay H-L (t_{PD-}) vs. Input Common-Mode Voltage

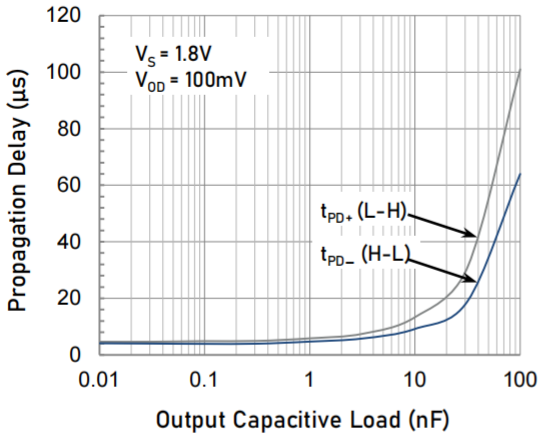


Propagation Delay L-H (t_{PD+}) vs. Input Common-Mode Voltage

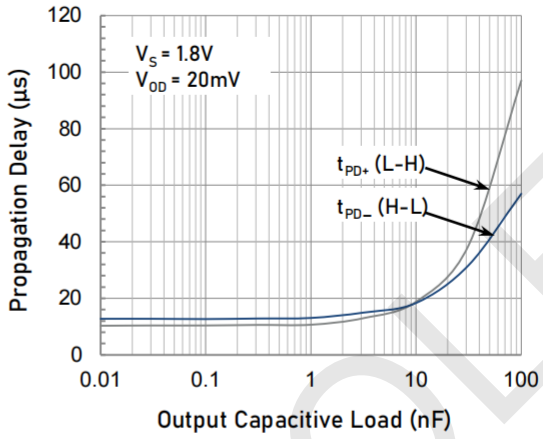
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Typical Performance Characteristics

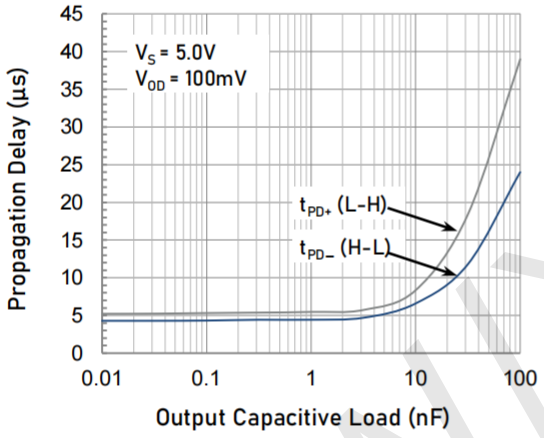
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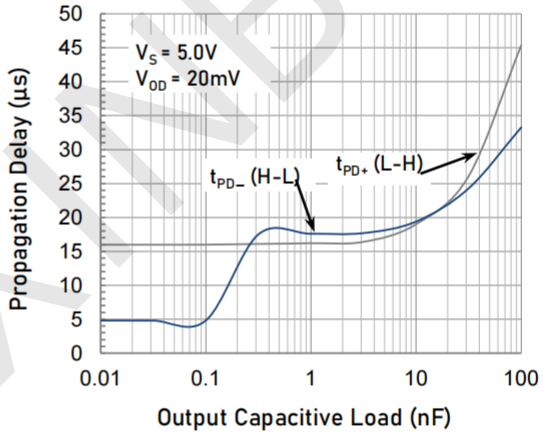
Propagation Delay vs. Capacitive Load (V_S = 1.8V)



Propagation Delay vs. Capacitive Load (V_S = 1.8V)



Propagation Delay vs. Capacitive Load (V_S = 5.0V)



Propagation Delay vs. Capacitive Load (V_S = 5.0V)

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Application Notes

OPERATING VOLTAGE

The TLV3491/3492/3494 family of nano-power comparators is fully specified and ensured for operation from 1.7V to 5.5V (±0.85V to ±2.75V). In addition, and many specifications apply over the industrial temperature range of –40°C to +85°C . Parameters that vary significantly with operating voltages or temperature are illustrated in the Typical Characteristics graphs.

NOTE: Supply voltages (V_{S+} to $V_{S–}$) higher than +10V can permanently damage the device.

INPUT VOLTAGE

The input common-mode voltage range of the TLV3491/3492/3494 comparators extends 100- mV beyond the supply rails. This performance is achieved with a complementary input stage: an N- channel input differential pair in parallel with a P- channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically V_{S+}–1.4V to the positive supply, whereas the P- channel pair is active for inputs from 100mV below the negative supply to approximately V_{S+}–1.4V. There is a small transition region, typically V_{S+}–1.2V to VS+ – 1V, in which both pairs are on. This 200mV transition region can vary up to 200mV with process variation. Thus, the transition region (both stages on) can range from V_{S+}–1.4V to V_{S+}–1.2V on the low end, up to V_{S+}–1V to V_{S+}–0.8V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

INPUT VOLTAGE

The TLV3491/3492/3494 comparator family uses CMOS transistors at the inputs which prevent phase inversion when the input pins exceed the supply voltages.

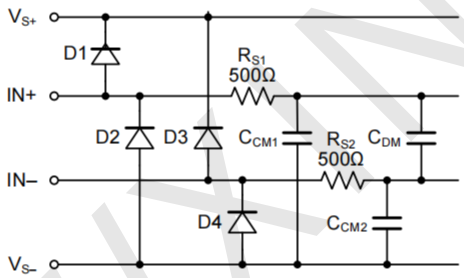


Figure 1. Input EMI Filter and Clamp Circuit

Figure 1 shows the input EMI filter and clamp circuit. The TLV3491/3492/3494 comparators have internal ESD protection diodes (D1, D2, D3, and D4) that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 300mV beyond the rails to be applied at the input of either terminal without causing permanent damage. See the table of Absolute Maximum Ratings for more information.

EMI REJECTION RATIO

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an amplifier must accurately amplify the input signals. However, all comparator pins — the non-inverting input, inverting input, positive supply, negative supply, and output pins — are susceptible to EMI signals. These high frequency signals are coupled into an comparator by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, comparators can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

The TLV3491/3492/3494 comparators have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$EMIRR = 20 \log (V_{IN_PEAK} / \Delta V_{OS})$

INTERNAL HYSTERESIS

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input. To counter the parasitic effects and noise, the devices have an internal hysteresis of 5 mV.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage. The difference between the trip points is the hysteresis. The average of the trip points

is the offset voltage. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. To increase hysteresis and noise margin even more, add positive feedback with two resistors as a voltage divider from the output to the non- inverting input. Figure 2 illustrates the case where IN– is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

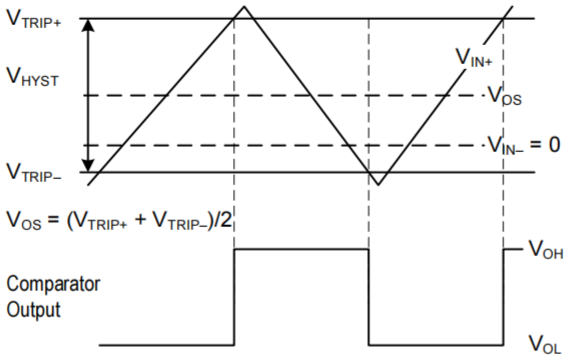


Figure 2. Input and Output Waveform, Non-inverting Input Varied

MAXIMIZING PERFORMANCE THROUGH PROPER LAYOUT

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the TLV3491/3492/3494 devices, care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the comparator inputs further reduces leakage currents. Figure 3 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

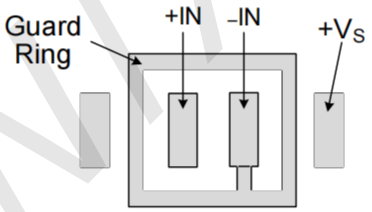


Figure 3. Use a guard ring around sensitive pins

Other potential sources of offset error are thermoelectric voltages on the circuit board. This voltage, also alled Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to- board trace and solder-to-component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

INPUT-TO-OUTPUT COUPLING

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

IR RECEIVER AFE AND WAKE- UP CIRCUIT

Infrared (IR) communication is inherently immune to RF interference as long as there is a line-of-sight path between the transmitter and the receiver. It is also one of the lowest cost communication schemes. This makes it a good choice for implementing wireless communications in applications such as utility metering. These smart utility meters are hermetically sealed and use a combination of batteries and solar cells to power

the system. Maintenance in the field can be costly, so minimizing system power consumption to extend battery life is desired.

A common system topology to extend battery life is to use a power efficient IR receiver analog front end (AFE) that is always on and wakes up the host only when there is a valid IR signal detected as shown in Figure 1. Power efficient comparators such as the TLV349x can be used in the IR receiver AFE to increase battery life.

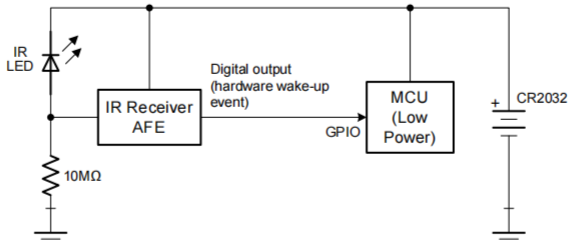


Figure 4. Coin Cell Battery Powered IR Receiver

The TLV349x device is responsible for two major tasks:

1. IR signal conditioning,
2. Host system wake-up.

The benefits of TLV349x for this application include the following:

1. Nano quiescent supply current (310 nA),
2. Low input bias current (5 pA) which allows a greater load resistor value.

The TLV349x device is constantly powered to always be ready to receive IR signals and wake up the host microcontroller (MCU) when data is received. The short working distance (approx 5 cm) is suitable for a virtual-contact operation where the IR transmitter and receiver are closely placed with an optional mechanical alignment guide.

Figure 1 shows the IR receiver system block diagram. The host MCU is normally in the shutdown mode (during which the quiescent current is less than 1 µA) except when data is being transferred.

Figure 2 shows the detailed circuit design. The circuit establishes a threshold through R_2 and C_1 which automatically adapts to the ambient light level. To further reduce BOM cost, this example uses an IR LED as the IR receiver. The IR LED is reverse-biased to function as a photodiode (but at a reduced sensitivity).

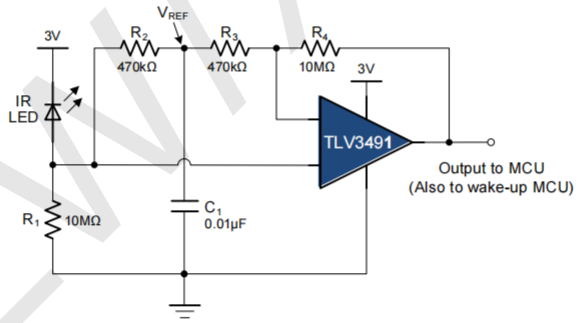


Figure 5. IR Receiver AFE Using TLV3491 (Push- Pull Output)

The low input bias current allows a greater load resistor value (R_1) without sacrificing linearity, which in turn helps reduce the always-on supply current.

The load resistor R_1 converts the IR light induced current into a voltage fed into the inverting input of the comparator. R_2 and C_1 establish a reference voltage V_{REF} which tracks the mean amplitude of the IR signal. The non-inverting input is connected to V_{REF} through R3. And finally R_3 and R_4 are used to introduce additional hysteresis to keep the output free of spurious toggles.

To achieve years of operation running on a single coin cell battery, the host MCU must be put in the shutdown power state. The MCU wakes up when data is received. After the data transmission is complete, the MCU reverts to the shutdown state and the overall supply current drops back to the micro amps level.

PARAMETER	
Aggregated always-on Current	2 µA
Peak Current (Wireless Radio + IR LED)	30 mA
Active Duration /Frequency	30 sec/30 days
CR 2032 Coin Cell Battery Capacity	240 mAh
CR 2032 Lifespan (minimum)	5 years
Lead Temperature Range (Soldering 10sec)	260 °C

Table 1 shows a power budget based on the following assumptions:

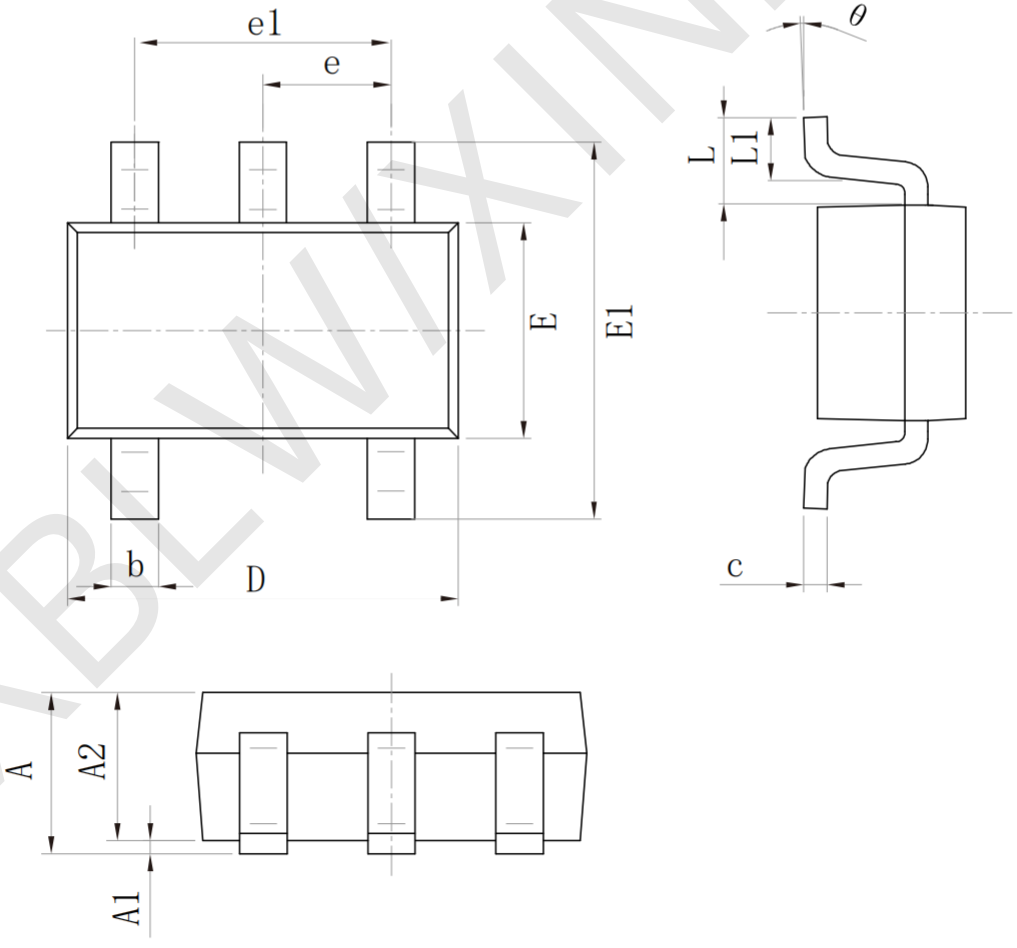
1. The aggregated always-on quiescent current is estimated as 2 µA, which includes the TLV3491 quiescent current, divider network current, and the MCU and supporting devices current in the shutdown state.
2. Peak current during active data transmission and RF radio operation is estimated as 30 mA.
3. Each active session last for 30 seconds or less for every 30 days or longer.
4. The coin cell is based on an Energizer CR2032, which is specified at 240 mAh and includes a 1% annual self-discharge rate.

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Package Information

• SC70-5

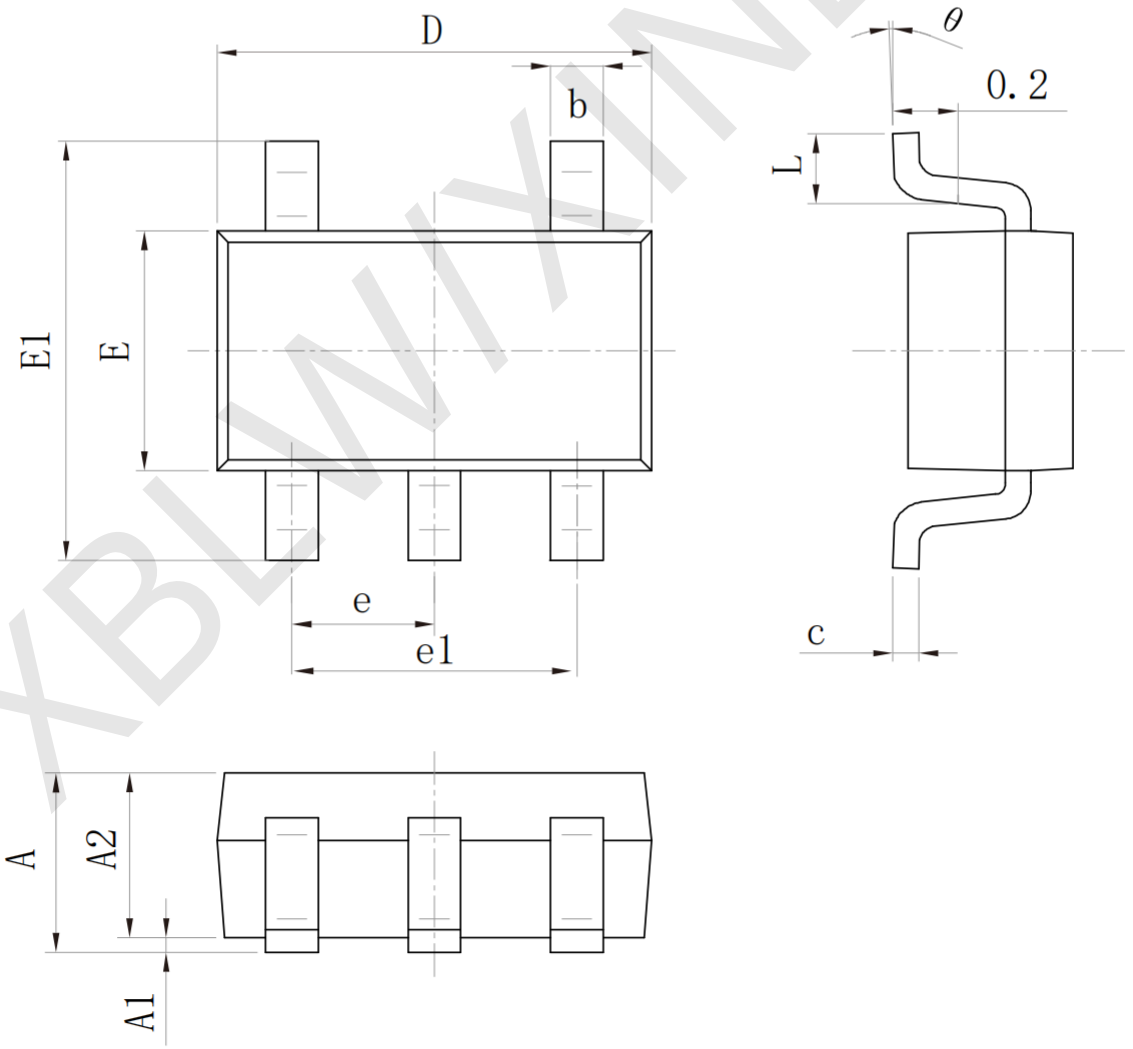
Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	0.800	1.100	A	0.035	0.043
A1	0.000	0.100	A1	0.000	0.004
A2	0.800	0.900	A2	0.035	0.039
b	0.150	0.350	b	0.006	0.014
C	0.080	0.150	C	0.003	0.006
D	1.850	2.150	D	0.079	0.087
E	1.100	1.400	E	0.045	0.053
E1	1.950	2.200	E1	0.085	0.096
e	0.85(typ)		e	0.026(typ)	
e1	1.200	1.400	e1	0.047	0.055
L	0.42(ref)		L	0.021(ref)	
L1	0.260	0.460	L1	0.010	0.018
θ	0°	8°	θ	0°	8°



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• SOT23-5

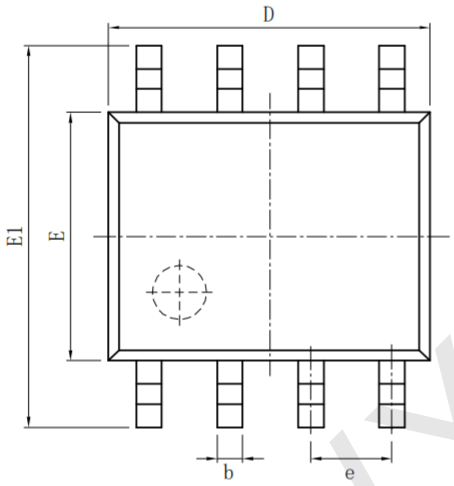
SIZE / SYMBOL	Dimensions In Millimeters		SIZE / SYMBOL	Dimensions In Inches	
	MIN(mm)	MAX(mm)		MIN(in)	MAX(in)
A	1.050	1.250	A	0.041	0.049
A1	0.000	0.100	A1	0.000	0.004
A2	1.050	1.150	A2	0.041	0.045
b	0.300	0.500	b	0.012	0.020
c	0.100	0.200	c	0.004	0.008
D	2.820	3.020	D	0.111	0.119
E	1.500	1.700	E	0.059	0.067
E1	2.650	2.950	E1	0.104	0.116
e	0.95(BSC)		e	0.037(BSC)	
e1	1.800	2.000	e1	0.071	0.079
L	0.300	0.600	L	0.012	0.024
θ	0°	8°	θ	0°	8°

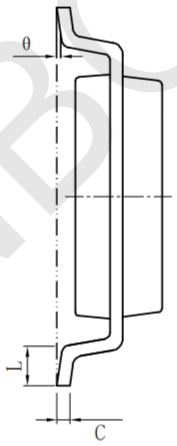


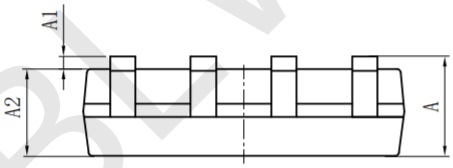
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- SOP-8

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	1.350	1.750	A	0.053	0.069
A1	0.100	0.250	A1	0.004	0.010
A2	1.350	1.550	A2	0.053	0.061
b	0.330	0.510	b	0.013	0.020
c	0.170	0.250	c	0.006	0.010
D	4.700	5.100	D	0.185	0.200
E	3.800	4.000	E	0.150	0.157
E1	5.800	6.200	E1	0.228	0.224
e	1.270(BSC)		e	0.050(BSC)	
L	0.400	1.270	L	0.016	0.050
θ	0°	8°	θ	0°	8°



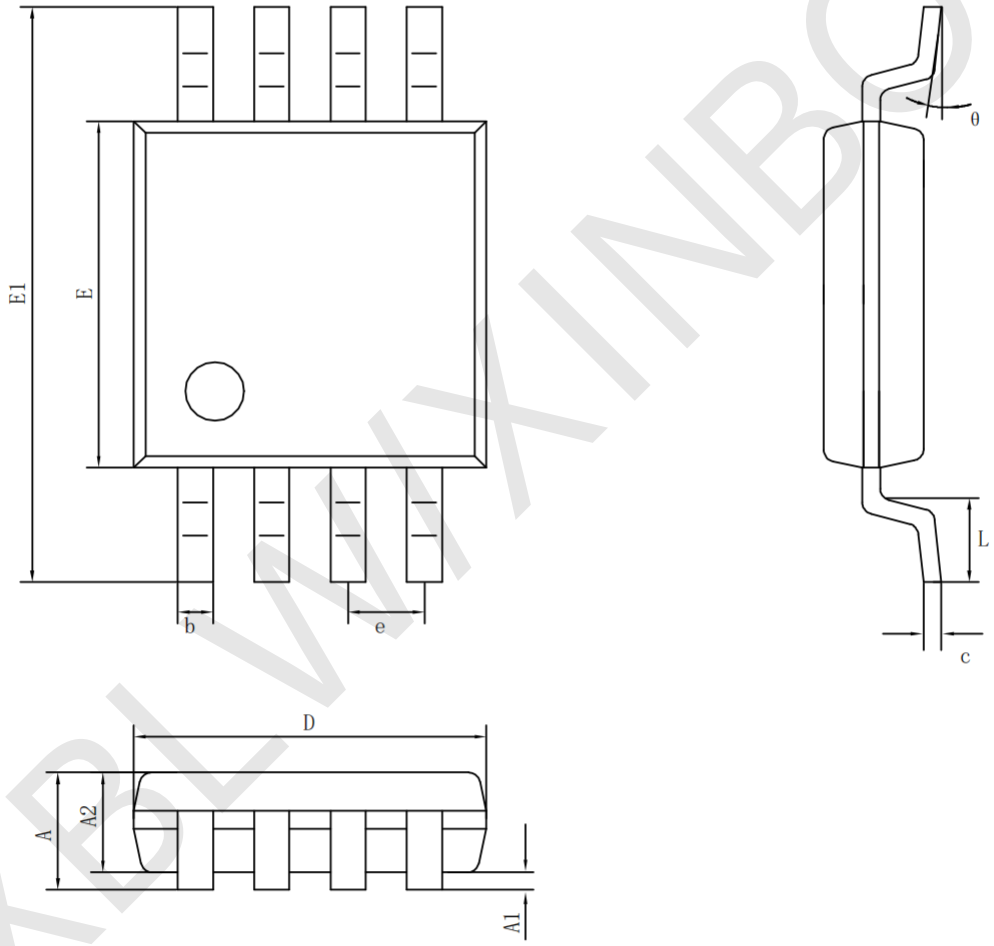




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· MSOP-8

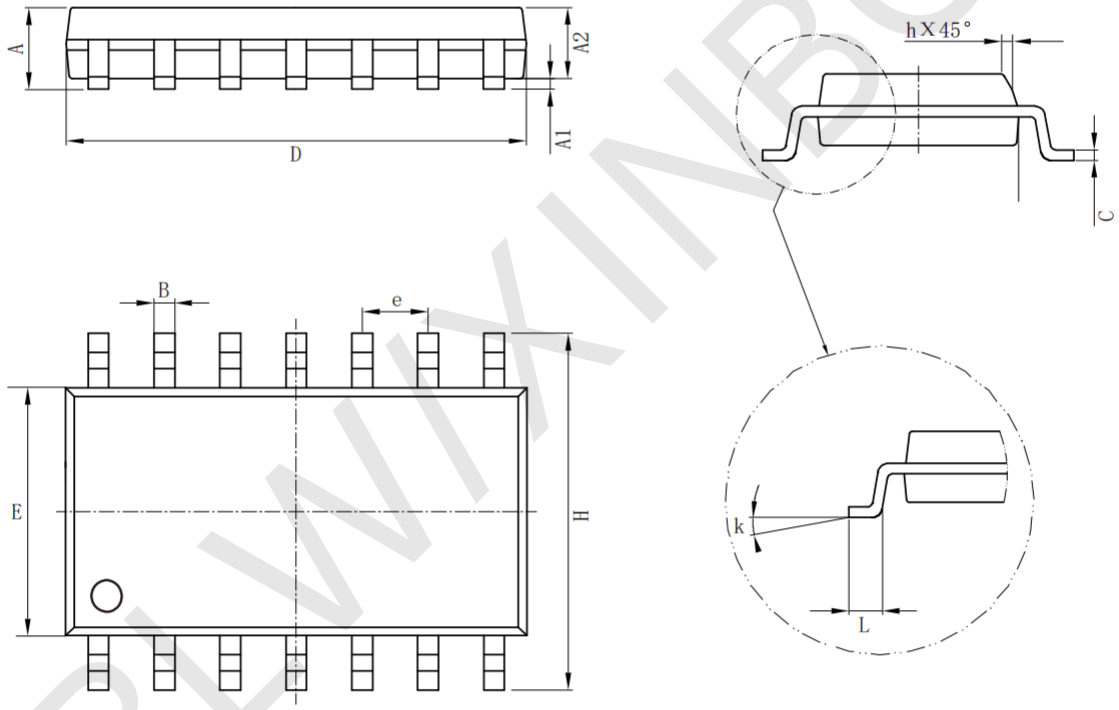
Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	0.820	1.100	A	0.320	0.043
A1	0.020	0.150	A1	0.001	0.006
A2	0.750	0.950	A2	0.030	0.037
b	0.250	0.380	b	0.010	0.015
c	0.090	0.230	c	0.004	0.009
D	2.900	3.100	D	0.114	0.122
e	0.65（BSC）		e	0.026(BSC)	
E	2.900	3.100	E	0.114	0.122
E1	4.750	5.050	E1	0.187	0.199
L	0.400	0.800	L	0.016	0.031
θ	0°	6°	θ	0°	6°



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· SOP-14

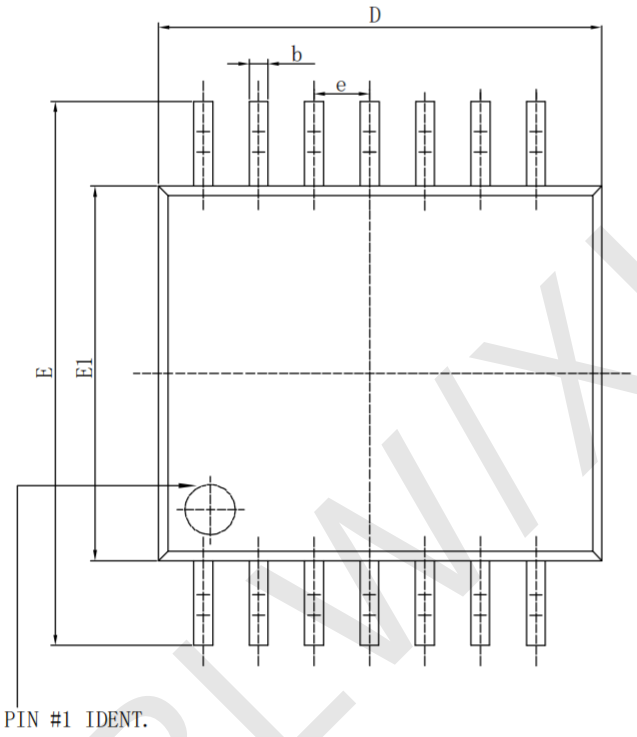
Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A	1.350	1.750	A	0.050	0.068
A1	0.100	0.250	A1	0.004	0.009
A2	1.100	1.650	A2	0.040	0.060
B	0.330	0.510	B	0.010	0.020
C	0.190	0.250	C	0.007	0.009
D	8.550	8.750	D	0.330	0.340
E	3.800	4.000	E	0.150	0.150
e	1.27		e	0.05	
H	5.800	6.200	H	0.220	0.240
h	0.250	0.500	h	0.009	0.020
L	0.400	1.270	L	0.015	0.050
k	8° (max)		k	8° (max)	

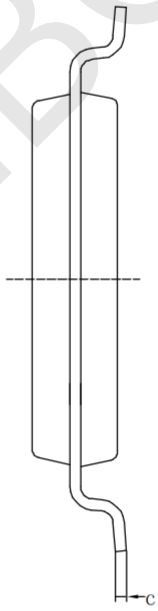


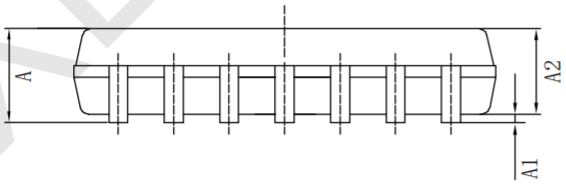
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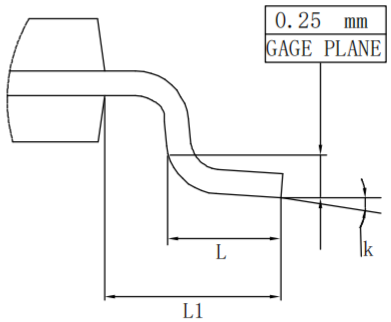
· TSSOP-14

Size / Symbol	Dimensions In Millimeters		Size / Symbol	Dimensions In Inches	
	Min(mm)	Max(mm)		Min(in)	Max(in)
A		1.200	A		0.047
A1	0.050	0.150	A1	0.002	0.006
A2	0.800	1.050	A2	0.031	0.041
b	0.190	0.300	b	0.007	0.012
c	0.090	0.200	c	0.004	0.0089
D	4.900	5.100	D	0.193	0.201
E	6.200	6.600	E	0.244	0.260
E1	4.300	4.500	E1	0.169	0.176
e	0.65		e	0.0256	
L	0.450	0.750	L	0.018	0.030
L1	1.00		L1	0.039	
k	0°	8°	k	0°	8°









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