DS1302

DATASHEET

Specification Revision History:

Version	Date	Description
V1.0	2020/01	New
V1.1	2021/05	Modify Ordering Information
V1.2	2023/02	Modify Ordering Information
V1.3	2025/05	Add application precautions and overall typesetting.

DESCRIPTION

The DS1302 Trickle Charge Timekeeping Chip contains a real time clock/calendar and 31 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The real time clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24–hour or 12–hour format with an AM/PM indicator.

Interfacing the DS1302 with a microprocessor is simplified by using synchronous serial communication. Only three wires are required to communicate with the clock/RAM: (1) CE (Reset), (2) I/O (Data line), and (3) SCLK (Serial clock). Data can be transferred to and from the clock/RAM 1 byte at a time or in a burst of up to 31 bytes. The DS1302 is designed to operate on very low power and retain data and clock information on less than 1microwatt.

In addition to the basic timekeeping functions, the DS1302 has the additional features of dual power pins for primary and back–up power supplies, programmable trickle charger for VCC1, and seven additional bytes of scratchpad memory.

FEATURES

※ Real time clock counts seconds, minutes hours, date of the month, month, day of the week, and year with leap year compensation valid up to 2100

※ 31×8 RAM for scratchpad data storage

※ Serial I/O for minimum pin count

※ 2.0–5.5V full operation

※ Uses less than 300nA at 2.0V

※ Single–byte or multiple–byte (burst mode) data transfer for read or write of clock or RAM data

※ Simple 3–wire interface

※ TTL–compatible (V_{CC} = 5V)

※ Optional temperature range –20°C to +85°C

※ PACKAGE: SOP8

APPLICATIONS

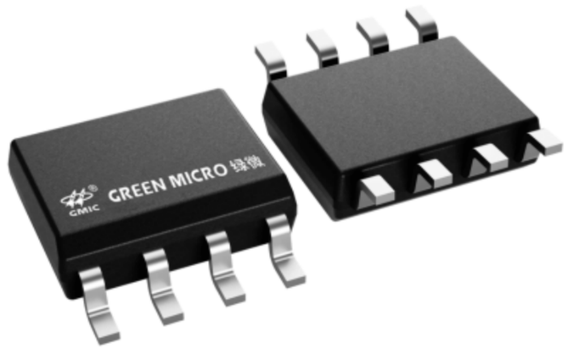
※ Telephone

※ Fax

※ Portable instrument

※ Instruments and meters

THE APPEARANCE OF THE PRODUCT

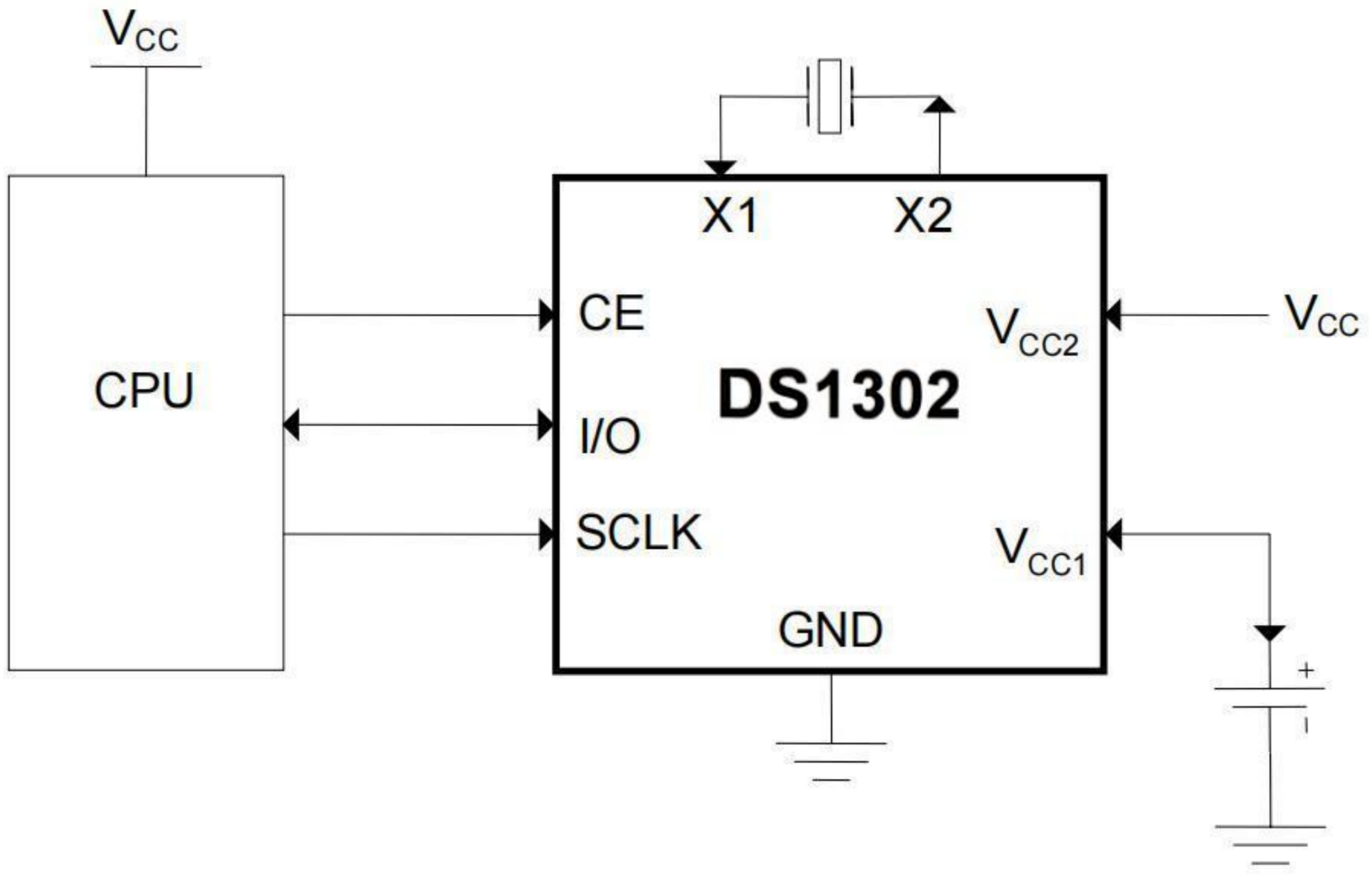


SOP-8

ORDERING INFORMATION

Product Model	Package Type	Packing	Packing Qty
DS1302ZN	SOP-8	REEL	2500PCS/REEL

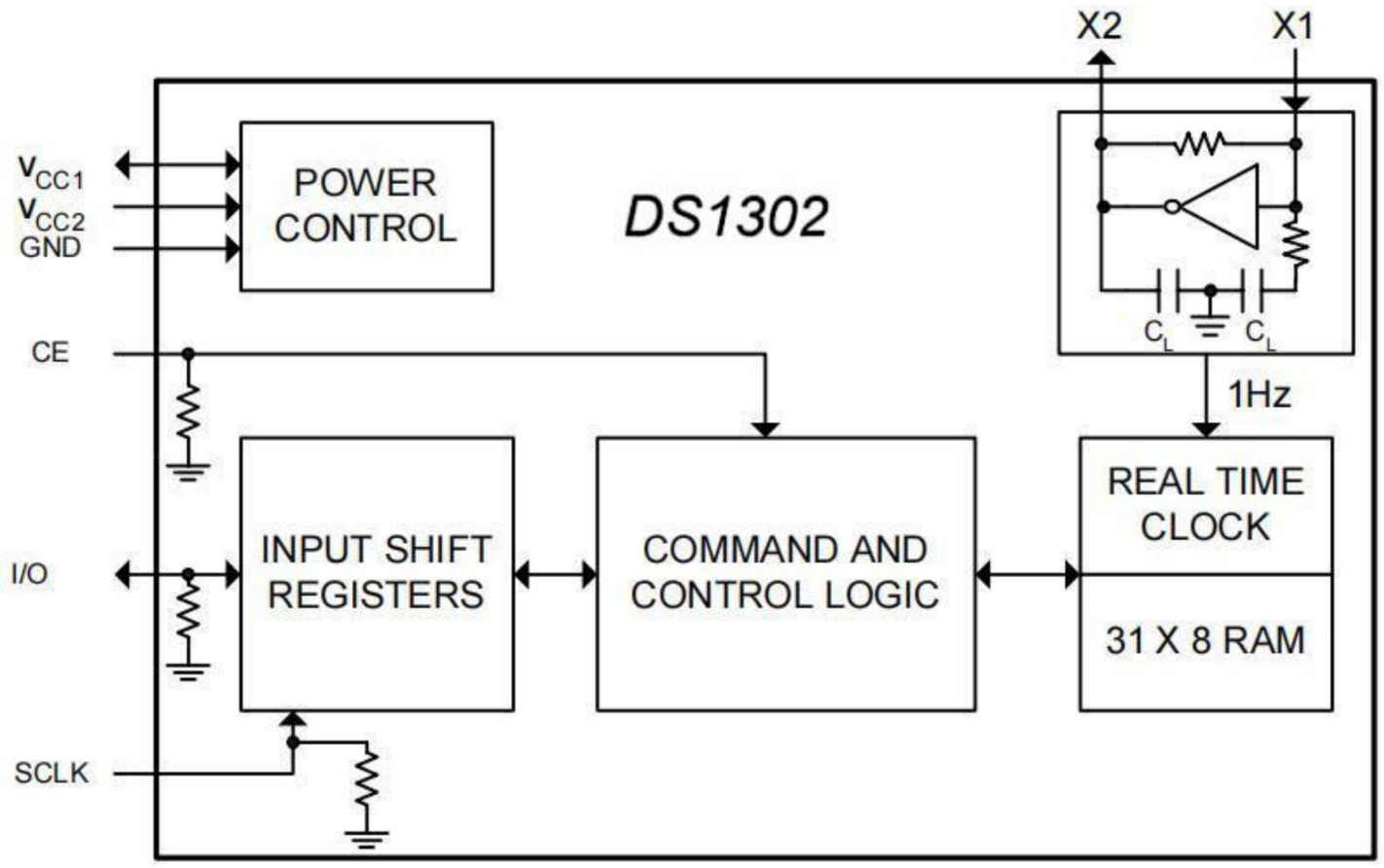
TYPICAL OPERATING CIRCUIT



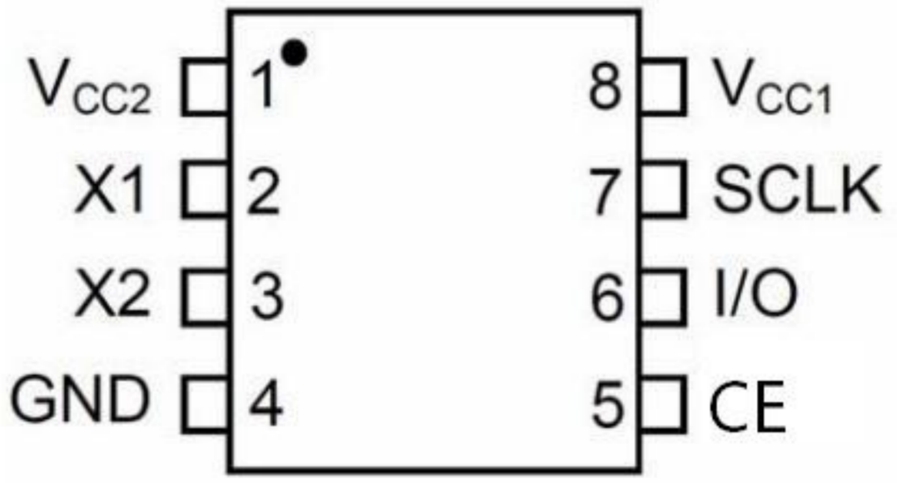
OPERATION

Figure 1 shows the main elements of the serial timekeeper: shift register, control logic, oscillator, real-time clock, and RAM.

Figure 1.Block Diagram



PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	V_{CC2}	P	Primary Power-Supply Pin in Dual Supply Configuration. V_{CC1} is connected to a backup source to maintain the time and date in the absence of primary power. The DS1302 operates from the larger of V_{CC1} or V_{CC2} . When V_{CC2} is greater than V_{CC1} + 0.2V, V_{CC2} powers the DS1302. When V_{CC2} is less than V_{CC1}, V_{CC1} powers the DS1302..
2	X1	I	Connections for Standard 32.768kHz Quartz Crystal. The internal oscillator is designed for operation with a crystal having a specified load capacitance of 6pF. The DS1302 can also be driven by an external 32.768kHz oscillator. In this configuration, the X1 pin is connected to the external oscillator signal and the X2 pin is floated.
3	X2	O	
4	GND	P	Ground

5	CE	I	Input. CE signal must be asserted high during a read or a write. This pin has an internal 40kΩ (typ) pulldown resistor to ground. Note: Previous data sheet Revisions referred to CE as RST. The functionality of the pin has not changed.
6	I/O	I/O	Input/Push-Pull Output. The I/O pin is the bidirectional data pin for the 3-wire interface. This pin has an internal 40kΩ (typ) pulldown resistor to ground.
7	SCLK	I	Input. SCLK is used to synchronize data movement on the serial interface. This pin has an internal 40kΩ (typ) pulldown resistor to ground.
8	V_{CC1}	P	Low-Power Operation in Single Supply and Battery-Operated Systems and Low-Power Battery Backup. In systems using the trickle charger, the rechargeable energy source is connected to this pin.

COMMAND BYTE

The command byte is shown in Figure 2. Each data transfer is initiated by a command byte. The MSB (Bit 7) must be a logic 1. If it is 0, writes to the DS1302 will be disabled. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits 1 through 5 specify the designated registers to be input or output, and the LSB (bit 0) specifies a write operation (input) if logic 0 or read operation (output) if logic 1. The command byte is always input starting with the LSB (bit 0).

Figure 2.ADDRESS/COMMAND BYTE

7	6	5	4	3	2	1	0
1	RAM / $\overline{CK}$	A4	A3	A2	A1	A0	RD / $\overline{W}$

CE AND CLOCK CONTROL

All data transfers are initiated by driving the CE input high. The CE input serves two functions. First, CE turns on the control logic which allows access to the shift register for the address/command sequence. Second, the CE signal provides a method of terminating either single byte or multiple byte data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. If the CE input is low all data transfer terminates and the I/O pin goes to a high impedance state. Data transfer is illustrated in Figure 3. At power–up, CE must be a logic 0 until VCC>2.0 volts. Also SCLK must be at a logic 0 when CE is driven to a logic 1 state.

DATA INPUT

Following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored should they inadvertently occur. Data is input starting with bit 0.

DATA OUTPUT

Following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles re-transmit the data bytes should they inadvertently occur so long as RST remains high. This operation permits continuous burst mode read capability. Also, the I/O pin is tri–stated upon each rising edge of SCLK. Data is output starting with bit 0.

BURST MODE

Burst mode may be specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (address/command bits 1 through 5 = logic 1). As before, bit 6 specifies clock or RAM and bit 0 specifies read or write. There is no data storage capacity at locations 9 through 31 in the Clock/Calendar Registers or location 31 in the RAM registers. Reads or writes in burst mode start with bit 0 of address 0.

When writing to the clock registers in the burst mode, the first eight registers must be written in order for the data to be transferred. However, when writing to RAM in burst mode it is not necessary to write all 31 bytes for the data to transfer. Each byte that is written to will be transferred to RAM regardless of whether all 31 bytes are written or not.

CLOCK/CALENDAR

The clock/calendar is contained in seven write/read registers as shown in Figure 4. Data contained in the clock/ calendar registers is in binary coded decimal format (BCD).

CLOCK HALT FLAG

Bit 7 of the seconds register is defined as the clock halt flag. When this bit is set to logic 1, the clock oscillator is stopped and the DS1302 is placed into a low–power standby mode with a current drain of less than 100nA. When this bit is written to logic 0, the clock will start. The initial power on state is not defined.

AM-PM/12-24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

WRITE PROTECT BIT

Bit 7 of the control register is the write-protect bit. The first seven bits (bits 0-6) are forced to 0 and will always read a 0 when read. Before any write operation to the clock or RAM, bit 7 must be 0. When high, the write protect bit prevents a write operation to any other register. The initial power on state is not defined. Therefore the WP bit should be cleared before attempting to write to the device.

TRICKLE CHARGE REGISTER

This register controls the trickle charge characteristics of the DS1302. The simplified schematic of Figure 5 shows the basic components of the trickle charger. The trickle charge select (TCS) bits (bits 4-7) control the selection of the trickle charger. In order to prevent accidental enabling, only a pattern of 1010 will enable the trickle charger. All other patterns will disable the trickle charger. The DS1302 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2-3) select whether one diode or two diodes are connected between V_{CC2} and V_{CC1}. If DS is 01, one diode is selected or if DS is 10, two diodes are selected. If DS is 00 or 11, the trickle charger is disabled independently of TCS. The RS bits (bits 0- 1) select the resistor that is connected between VCC2 and VCC1 . The resistor selected by the resistor select (RS) bits is as follows:

RS Bits	Resistor	Typical Value
00	None	None
01	R1	2 kΩ
10	R2	4 kΩ
11	R3	8 kΩ

If RS is 00, the trickle charger is disabled independently of TCS.

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 5 volt is applied to VCC2 and a super cap is connected to VCC1 . Also assume that the trickle charger has been enabled with one diode and resistor R1 between VCC2 and VCC1 . The maximum current Imax would therefore be calculated as follows:

$$I_{max} = (5.0V - \text{diode drop}) / R1 \approx (5.0V - 0.7V) / 2\,k\Omega \approx 2.2mA$$

Obviously, as the super cap charges, the voltage drop between VCC2 and VCC1 will decrease and therefore the charge current will decrease.

CLOCK/CALENDAR BURST MODE

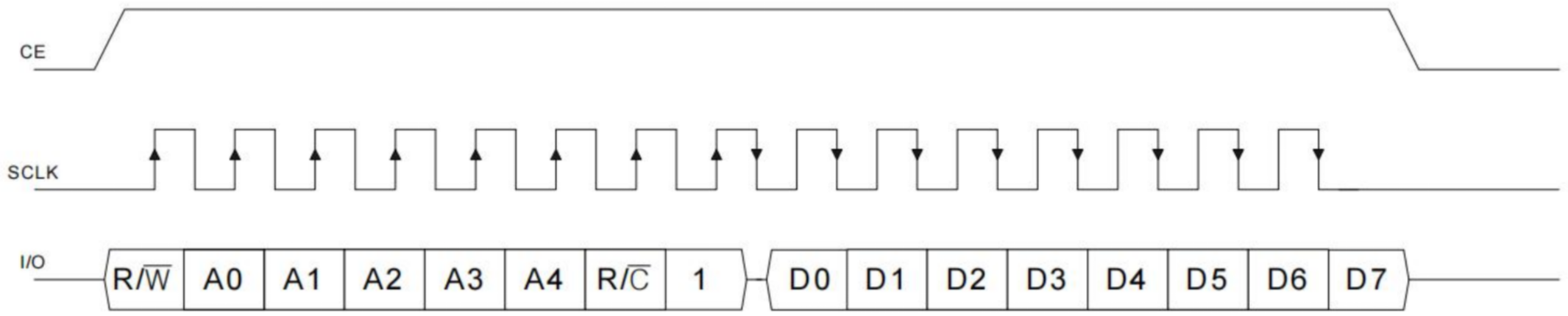
The clock/calendar command byte specifies burst mode operation. In this mode the first eight clock/calendar registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

The clock/calendar command byte specifies burst mode operation. In this mode the first eight clock/calendar registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

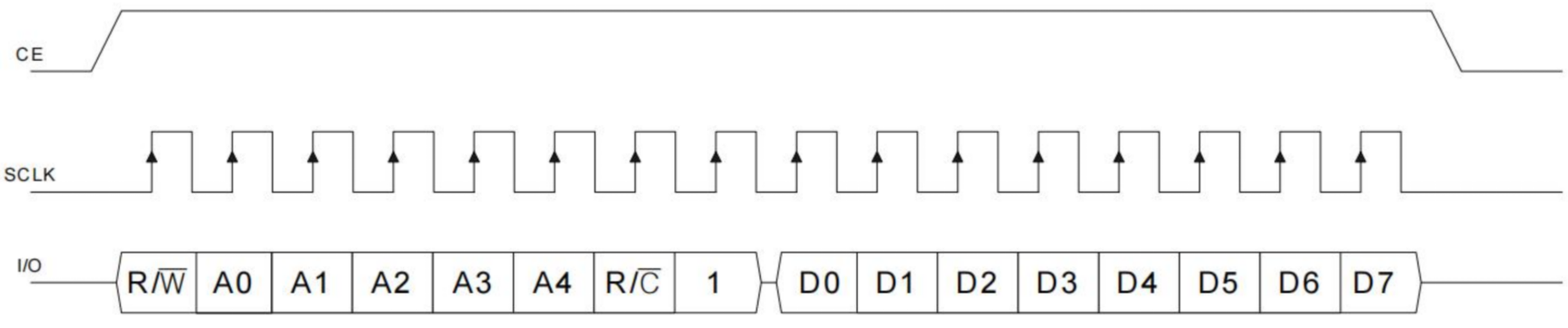
At the beginning of a clock burst read, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

Figure 3. DATA TRANSFER SUMMARY

SINGLE-BYTE READ



SINGLE-BYTE WRITE



NOTE: IN BURST MODE, CE IS KEPT HIGH AND ADDITIONAL SCLK CYCLES ARE SENT UNTIL THE END OF THE BURST.

RAM

The static RAM is 31 x 8 bytes addressed consecutively in the RAM address space.

RAM BURST MODE

The RAM command byte specifies burst mode operation. In this mode, the 31 RAM registers can be consecutively read or written (see Figure 4) starting with bit 0 of address 0.

REGISTER SUMMARY

A register data format summary is shown in Figure 4.

CRYSTAL SELECTION

A 32.768 kHz crystal can be directly connected to the DS1302 via X1 and X2. The crystal selected for use should have a specified load capacitance (CL) of 6pF.

Figure 4.REGISTER ADDRESS/DEFINITION

REGISTER ADDRESS

A. CLOCK

	7	6	5	4	3	2	1	0
SEC	1	0	0	0	0	0	0	RD/$\overline{W}$
MIN	1	0	0	0	0	0	1	RD/$\overline{W}$
HR	1	0	0	0	0	1	0	RD/$\overline{W}$
DATE	1	0	0	0	0	1	1	RD/$\overline{W}$
MONTH	1	0	0	0	1	0	0	RD/$\overline{W}$
DAY	1	0	0	0	1	0	1	RD/$\overline{W}$
YEAR	1	0	0	0	1	1	0	RD/$\overline{W}$
CONTROL	1	0	0	0	1	1	1	RD/$\overline{W}$
TRICKLE CHARGER	1	0	0	1	0	0	0	RD/$\overline{W}$
CLOCK BURST	1	0	1	1	1	1	1	RD/$\overline{W}$

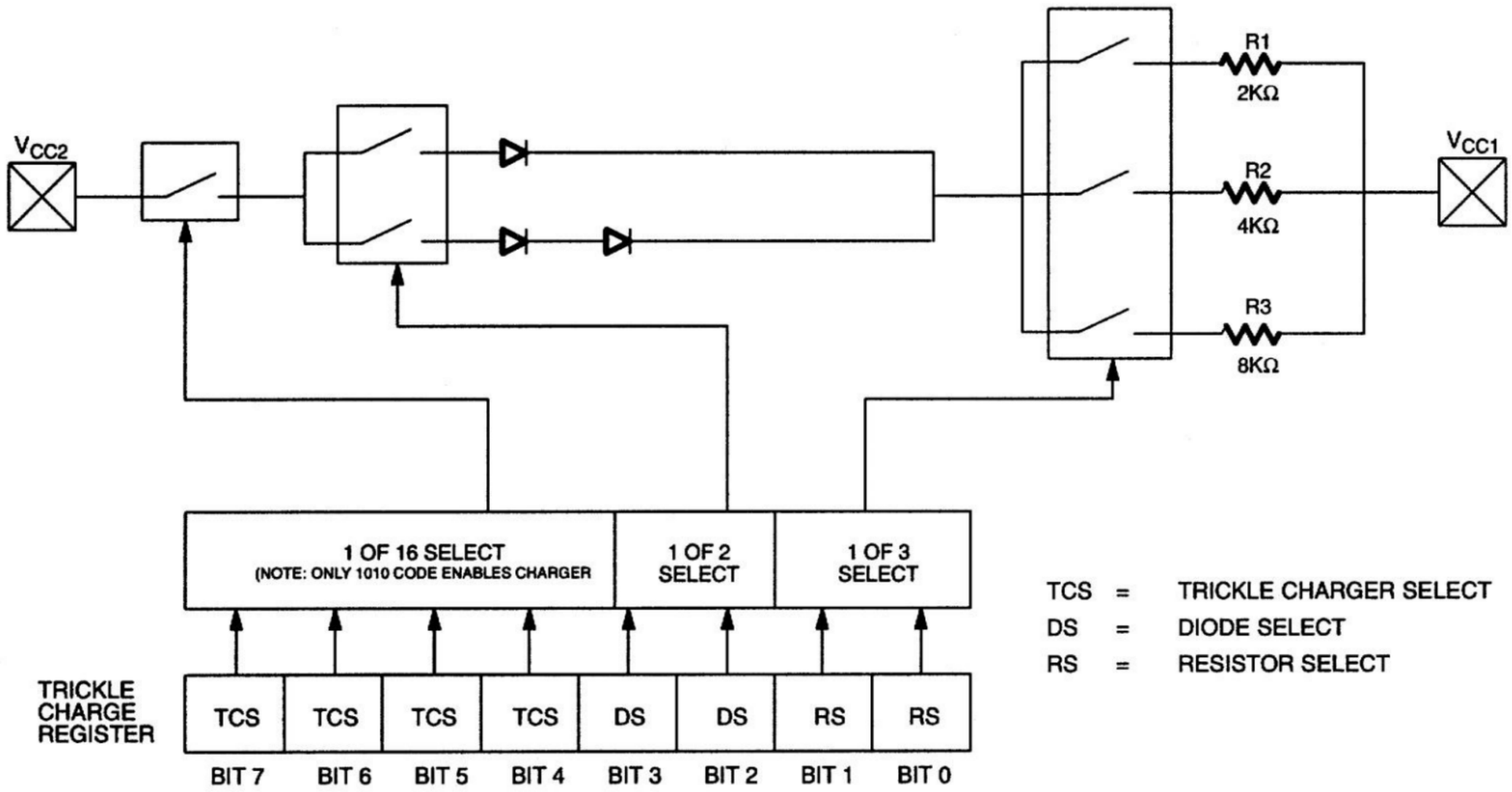
B. RAM

RAM 0	1	1	0	0	0	0	0	RD/$\overline{W}$
⋮								
RAM 30	1	1	1	1	1	1	0	RD/$\overline{W}$
RAM BURST	1	1	1	1	1	1	1	RD/$\overline{W}$

REGISTER DEFINITION

00–59	CH	10 SEC		SEC				
00–59	0	10 MIN		MIN				
01–12 00–23	12/24	0	10 A/P	HR	HR			
01–28/29 01–30 01–31	0	0	10 DATE		DATE			
01–12	0	0	0	10 M	MONTH			
01–07	0	0	0	0	0	DAY		
00–99	10 YEAR				YEAR			
	WP	0	0	0	0	0	0	0
	TCS	TCS	TCS	TCS	DS	DS	RS	RS
RAM DATA 0								
⋮								
RAM DATA 30								

Figure 5.DS1302 PROGRAMMABLE TRICKLE CHARGER



ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	MAX	UNIT
Voltage on Any Pin Relative to Ground	-0.5	7	V
Operating Temperature Range	-20	+85	°C
Storage Temperature Range	-55	+125	°C
Soldering Temperature(10 seconds)	-	260	°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL		NOTES	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC1},V_{CC2}		1, 11	2.0	-	5.5	V
Logic 1 Input	V_{IH}		1	2.0	-	V_{CC}+0.3	V
Logic 1 Input	V_{IL}	V_{CC}=2V	1	-0.3	-	+0.3	V
		V_{CC}=5V	1	-0.3	-	+0.8	V

DC ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{CC} = 2.0 to 5.5V, TA = -20°C to +85°C.)

PARAMETER	SYMBOL		NOTES	MIN	TYP	MAX	UNIT
Input Leakage	I_{LI}		6			500	uA
I/O Leakage	I_{LO}		6			500	uA
Logic 1 Output	V_{OH}	V_{CC}=2V	2	1.6			V
		V_{CC}=5V		2.4			
Logic 0 Output	V_{OL}	V_{CC}=2V	3			0.4	V
		V_{CC}=5V				0.4	
Active Supply Current	I_{CC1A}	V_{CC1}=2V	5, 12			0.4	mA
		V_{CC1}=5V				1.2	
Timekeeping Current	I_{CC1T}	V_{CC1}=2V	4, 12			0.3	uA
		VCC1=5V				1	
Standby Current	I_{CC1S}	V_{CC1}=2V	10, 12, 14			100	nA
		V_{CC1}=5V				100	
		IND				200	
Active Supply Current	I_{CC2A}	V_{CC2}=2V	5, 13			0.425	mA
		V_{CC2}=5V				1.28	
Timekeeping Current	I_{CC2T}	V_{CC2}=2V	4, 13			25.3	uA
		V_{CC2}=5V				81	
Standby Current	I_{CC2S}	V_{CC2}=2V	10, 13			25	uA
		V_{CC2}=5V				80	
Trickle Charge Resistors	R1				2		KΩ
	R2				4		
	R3				8		
Trickle Charge Diode Voltage Drop	V_{TD}				0.7		V

AC ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, VCC = 2.0 to 5.5V, TA = -20°C to +85°C.)

PARAMETER	SYMBOL		NOTES	MIN	TYP	MAX	UNIT
Data to CLK Setup	t_{DC}	V_{CC}=2V	7	200			ns
		V_{CC}=5V		50			
CLK to Data Hold	t_{CDH}	V_{CC}=2V	7	280			ns
		V_{CC}=5V		70			
CLK to Data Delay	t_{CDD}	V_{CC}=2V	7, 8, 9			800	ns
		V_{CC}=5V				200	
CLK Low Time	t_{CL}	V_{CC}=2V	7	1000			ns
		V_{CC}=5V		250			
CLK High Time	t_{CH}	V_{CC}=2V	7	1000			ns
		V_{CC}=5V		250			
CLK Frequency	t_{CLK}	V_{CC}=2V	7			0.5	MHz
		V_{CC}=5V		DC		2.0	
CLK Rise and Fall	$t_{R, tF}$	V_{CC}=2V				2000	ns
		V_{CC}=5V				500	
CE to CLK Setup	t_{CC}	V_{CC}=2V	7	4			ns
		V_{CC}=5V		1			
CLK to CE Hold	t_{CCH}	V_{CC}=2V	7	240			ns
		V_{CC}=5V		60			
CE Inactive Time	t_{CWH}	V_{CC}=2V	7	4			ns
		V_{CC}=5V		1			
CE to I/O High Impedance	t_{CDZ}	V_{CC}=2V	7			280	ns
		V_{CC}=5V				70	
SCLK to I/O High Impedance	t_{CCZ}	V_{CC}=2V	7			280	ns
		V_{CC}=5V				70	

Figure 6.TIMING DIAGRAM: READ DATA TRANSFER

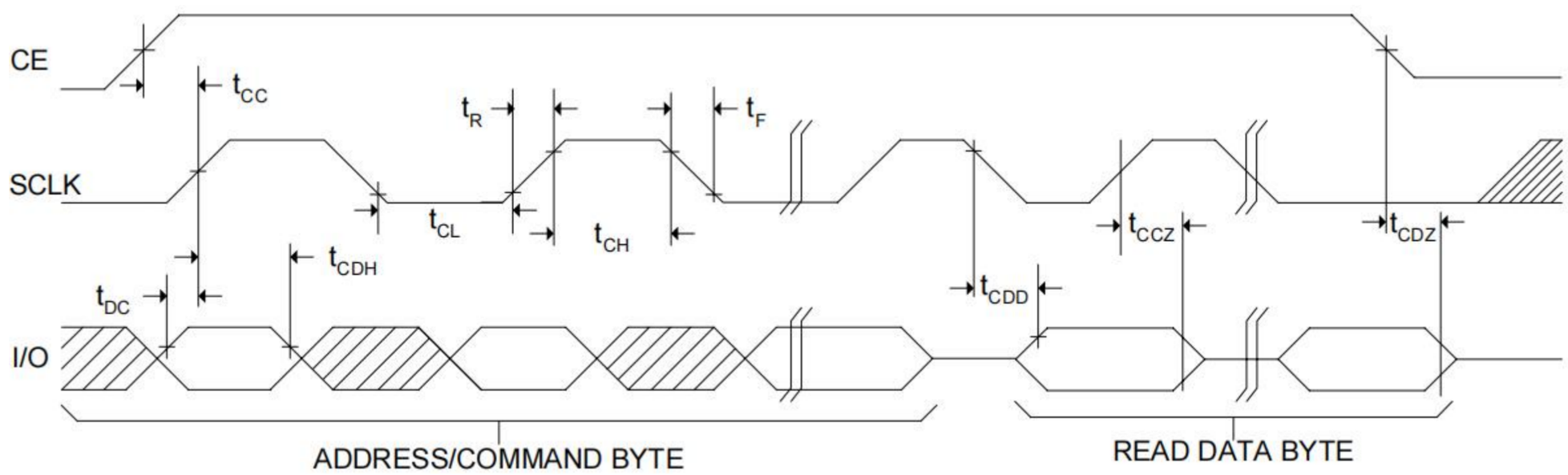
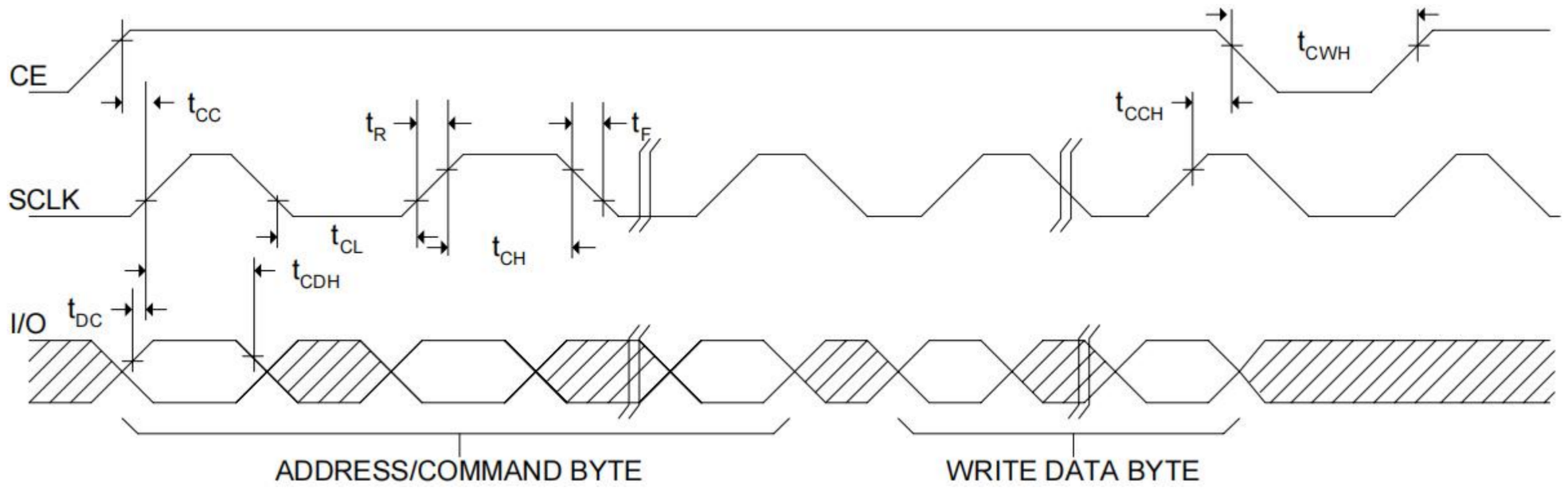


Figure 7.TIMING DIAGRAM: WRITE DATA TRANSFER

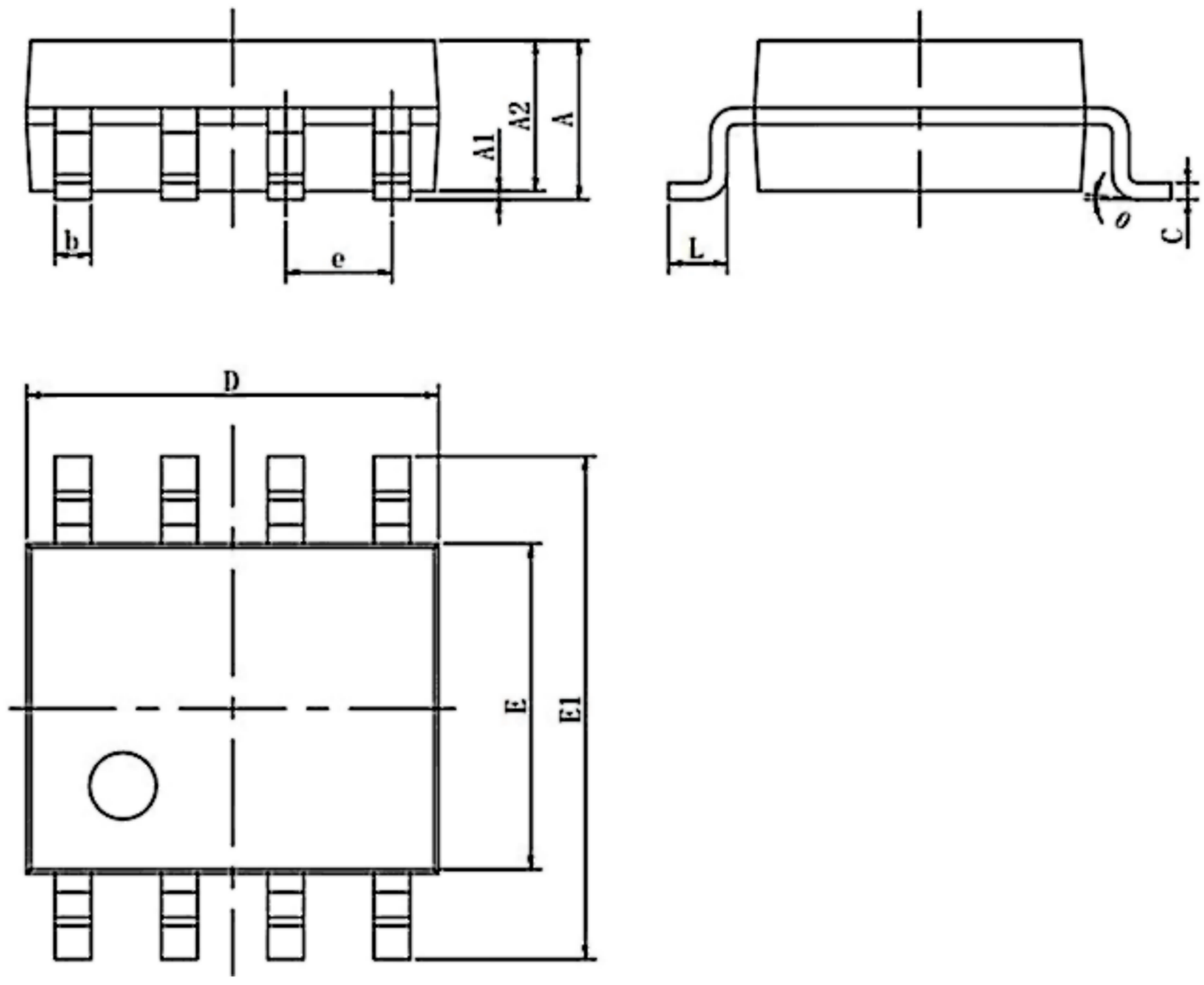


NOTES:

1. All voltages are referenced to ground.
2. Logic one voltages are specified at a source current of 1mA at V_{CC}=5V and 0.4mA at V_{CC}=2.0V, V_{OH}=V_{CC} for capacitive loads.
3. Logic zero voltages are specified at a sink current of 4mA at V_{CC}=5V and 1.5mA at V_{CC}=2.0V, V_{OL}=GND for apacitive loads.
4. I_{CC1T} and I_{CC2T} are specified with I/O open, CE set to a logic “0”, and clock halt flag=0 (oscillator enabled).
5. I_{CC1A} and I_{CC2A} are specified with the I/O pin open, CE high, SCLK=2MHz at V_{CC}=5V; SCLK=500kHz, V_{CC}=2.0V and clock halt flag=0 (oscillator enabled).
6. CE, SCLK, and I/O all have 40 kΩ pull–down resistors to ground.
7. Measured at V_{IH}=2.0V or V_{IL}=0.8V and 10ns maximum rise and fall time.
8. Measured at V_{OH}=2.4V or V_{OL}=0.4V.
9. Load capacitance = 50pF.
10. I_{CC1S} and I_{CC2S} are specified with CE, I/O, and SCLK open. The clock halt flag must be set to logic one (oscillator disabled).
11. V_{CC}=V_{CC2}, when V_{CC2}>V_{CC1}+0.2V; V_{CC}=V_{CC1}, when V_{CC1}>V_{CC2}.
12. V_{CC2}=0V.
13. V_{CC1}=0V.
14. Typical values are at 25°C.

OUTLINE DIMENSIONS

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.800	0.053	0.071
A1	0.050	0.250	0.004	0.010
A2	1.250	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.170	0.250	0.006	0.010
D	4.780	5.000	0.185	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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