RAA221497

90A Smart Power Stage (SPS) Module with Integrated High Accuracy Current and Temperature Monitors

The RAA221497 is a 90A Smart Power Stage (SPS) that is compatible with Renesas Digital Multiphase (DMP) controllers. The SPS provides best-in-class current sense accuracy over line, load, and temperature. When combined with a Renesas DMP, these devices enable precision system-level power management and best-in-class transient response for load line based regulators. Additionally, these devices simplify design by eliminating typical DCR sensing networks and associated thermal compensation components. The thermally enhanced 4x6 standard package enables high density designs.The exposed heat slug package version reduces topside thermal impedance.

The RAA221497 features the Renesas tri-state PWM input that works together with Renesas Digital Multiphase controllers to provide a robust solution in the event of abnormal operating conditions. The SPS also improves system performance and reliability with integrated fault protection, including overcurrent (OCH and OCL), Negative Overcurrent (NOCP), Over-Temperature (OTP), BOOT UVLO, Brownout Detection (BD), and V_{CC} Undervoltage Lockout (UVLO).

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Features

- V_{IN} input range: +3.0V to +16V
- Supports 90A DC current
- 3.3V compatible tri-state PWM input
- ±3% accuracy continuous signal for current monitor
- 8mV/°C temperature monitor, TOUT
- Comprehensive fault protection for high system reliability
  - Negative Overcurrent Protection (NOCP)
  - Over-temperature and overcurrent protections
  - Auto Boot Capacitor Refresh and BOOT UVLO
  - V_{CC} (UVLO) and Brownout Detect
- Enable input and fault reporting outputs
- IOUT fault voltage levels
- Low power mode operation
- Up to 1.25MHz switching frequency
- ROHS compliant with Exemption 7a, 4x6 QFN package
  - Standard and Top exposed pad

Applications

- High frequency and high efficiency VRM and VRD
- Core, graphic, and memory VRs for µPs
- High density VR for server, networking, and cloud computing
- POL DC/DC converters and video gaming consoles

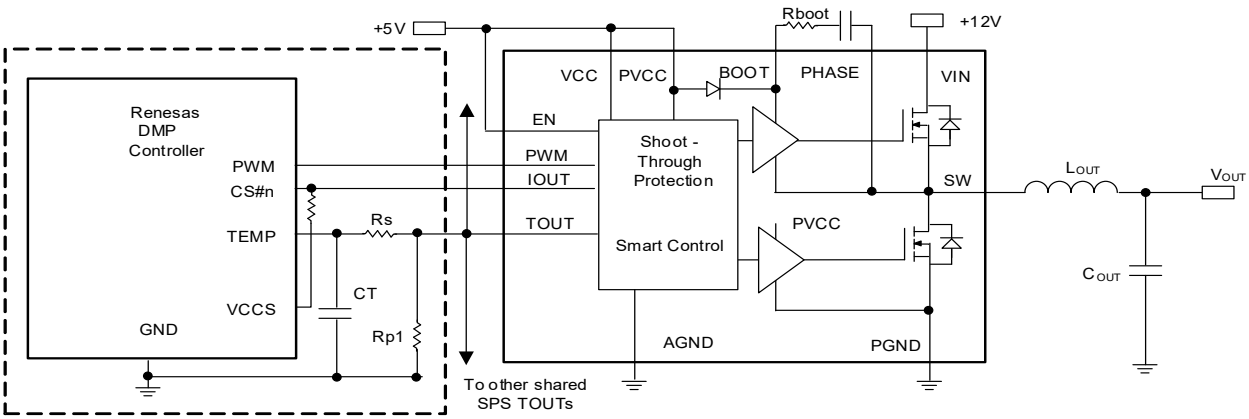


Figure 1. Simplified Application Block Diagram - See Table 1 for Rboot value

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1. Overview

1.1 Typical Application Circuit

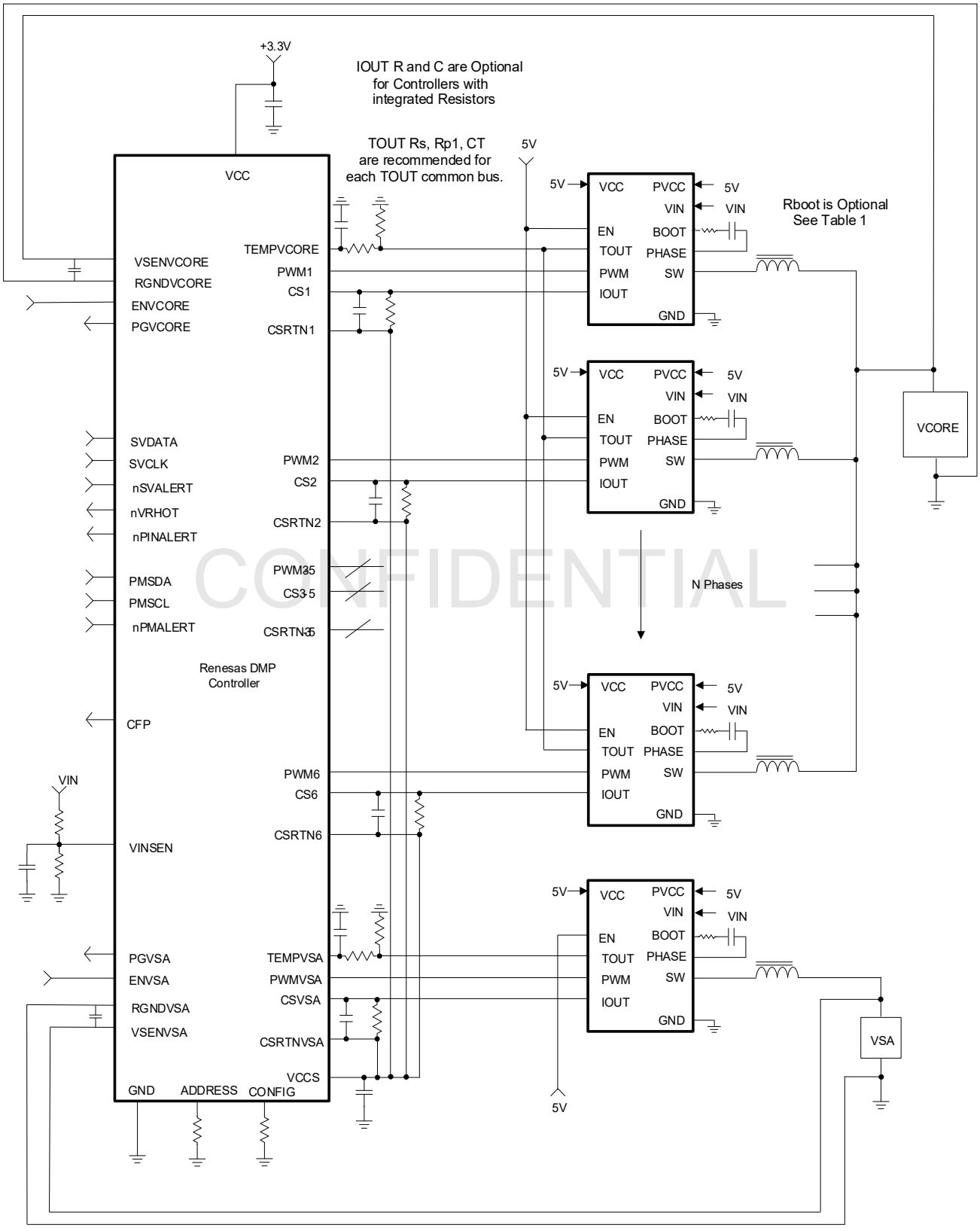


Figure 2. Typical Application Circuit - See Table 1 for Rboot value

1.2 Block Diagram

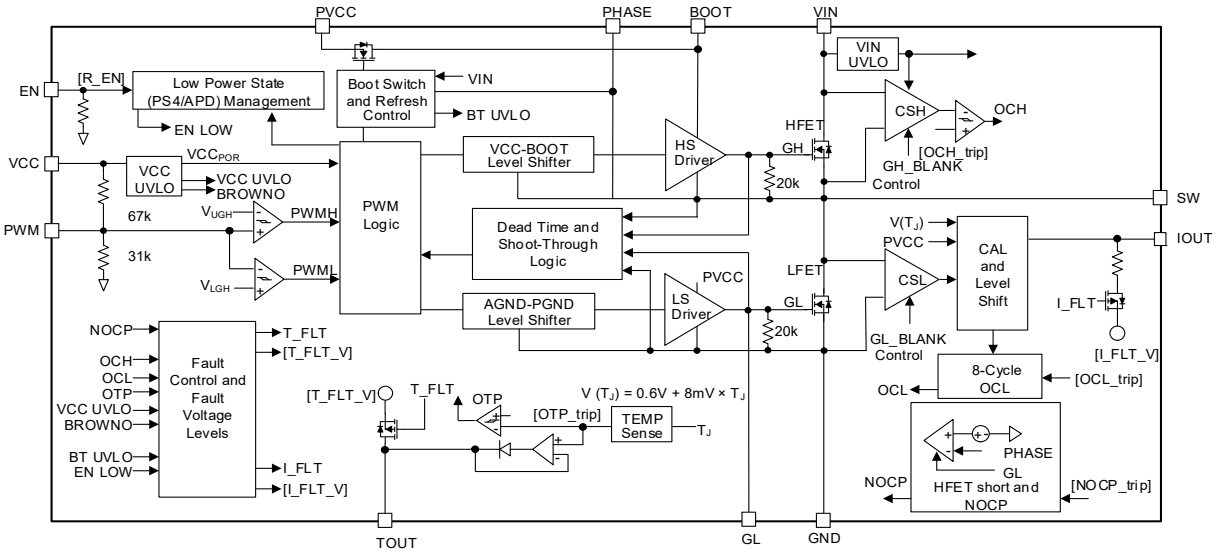
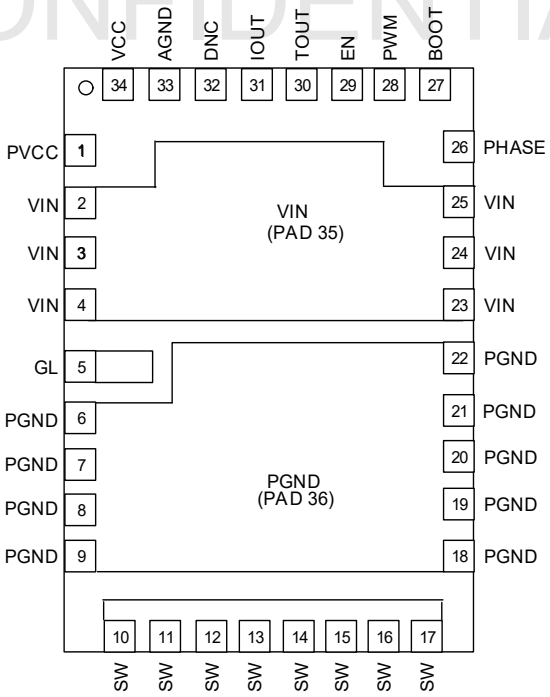


Figure 3. Functional Block Diagram

2. Pin Information

2.1 Pin Assignments

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Top View

2.2 Pin Descriptions

Pin #	Pin Name	Description
1	PVCC	+5V gate drive bias supply. Place a high quality ceramic capacitor (~1µF/X7R) in close proximity from this pin to AGND, on the same board layer. Connect PVCC to VCC. A combined VCC/PVCC capacitor provides the best layout and lowers component count (when the pins are adjacent or close). See Figure 14.
2, 3, 4, 23, 24, 25, PAD 35	VIN	Input of Power Stage (to drain of HFET); also used for VIN POR (for OCH) and auto boot refresh. Place at least two ceramic capacitors (10µF or higher, X5R or X7R) in close proximity across VIN and GND. Place 0603 or 0402 1µF/X5R high frequency decoupling capacitor on the same side of SPS, as shown in Figure 14. See the PCB layout shown in Figure 15 and Figure 16. For optimal performance, place as many vias as possible in the bottom side VIN paddle and extended VIN copper. VIN POR is only monitored for OCH, so the controller should separately monitor VIN for the system.
5	GL	Low-side gate driver output pin. Use is optional for monitoring and debugging.
6, 7, 8, 9, 18, 19, 20, 21, 22, PAD 36	PGND	All PGND pins are internally connected. Figure 14 illustrates how GND paddles should be connected to the system GND plane with as many vias as possible to maximize thermal and electrical performance.
10, 11, 12, 13, 14, 15, 16, 17	SW	Switching junction node between the HFET source and LFET drain. Connect directly to the output inductor.
26	PHASE	Return of boot capacitor. Internally connected to SW node so no external routing is required for SW connection.
27	BOOT	Floating bootstrap supply pin for the upper gate drive. Place a high quality ceramic capacitor (0.1µF/X7R) in close proximity across the BOOT and PHASE pins. A resistor in series with the boot capacitor might be recommended, based on the input voltage range in Table 1.
28	PWM	3.3V compatible PWM input of gate driver.
29	EN	Enable input. Enable low enters ultra low power mode after time-out, and Enable high exits low power mode with latency. Use a weak pull down to GND to keep pin from floating above its turn-on threshold at standby mode. When not used, tie to the VCC pin (do not float).
30	TOUT	Temperature and all-FAULT reporting output. For multiphase, the TOUT pins can be connected together as a common bus; the highest voltage (representing the highest temperature) is sent to the PWM controller. TOUT is pulled high when a fault is detected (see Table 3). When V_{CC} UVLO and Enable Low, this pin is pulled to GND. Renesas recommends using a network (capacitor to GND, a series Rs, and a parallel Rp) on each common or single TOUT bus. Locate all three components near its controller TEMP input pin, and its local GND. See Thermal Monitoring (TOUT) and Figure 13.
31	IOUT	A current sourced output is terminated into an external source/sink regulator from the controller (VCCS: typical 1.2V). The IOUT current signal is scaled to a proportional voltage with a 1kΩ resistor. Connect the IOUT output to the appropriate current sense input of the controller. No more than 47pF capacitance is recommended directly connected across the 1kΩ resistor. The IOUT pin also shows different voltage levels for the various faults; see Table 3.
32	DNC	Do Not Connect
33	AGND	Signal ground. Connect to system ground plane and PGND PAD 36. See Figure 14.
34	VCC	+5V logic bias supply. Place a high quality ceramic capacitor (~1µF/X7R) in close proximity from this pin to AGND, on the same board layer. Connect VCC to PVCC. A combined VCC/PVCC capacitor provides the best layout and lowers component count (when the pins are adjacent or close). See Figure 14.
Exposed Top Metal	(SW)	Electrically connected to SW internally. Use non-conductive epoxy to attach to heatsink.

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3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter (T_A = 25°C)	Minimum	Maximum	Unit
Continuous Current[1]	-	90	A
Supply Voltage (V_{CC}, PVCC)	-0.3	+6	V
Input Supply Voltage (V_{VIN-PH})	-0.3	+28	V
VIN-PHASE Voltage (V_{VIN-PH}) for 5ns	-10	+32	V
PHASE, SW Voltage (V_{PH-GND}, V_{SW-GND})	-0.3	+28	V
PHASE, SW Voltage (V_{PH-GND}, V_{SW-GND}) for 5ns	-10	+32	V
PHASE, SW Voltage (V_{PH-GND}, V_{SW-GND}) for 2ns	-15	+32	V
BOOT Voltage ($V_{BOOT-GND}$)	-0.3	+36	V
Other I/O Pin Voltage	-0.3	V_{CC}+0.3	V
Maximum Junction Temperature (Plastic Package)	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2017)	-	2	kV
Charged Device Model (Tested per JS-002-2018)	-	750	V
Latch-Up (Tested per JESD-78E; Class 2, Level A)	-	200	mA

1. Limited to power dissipation, thermal management solution, junction temperature, and over-temperature trip point for continuous operation; lower power dissipation and better cooling design allow higher continuous current.

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3.2 Recommended Operating Conditions

Caution: The device is not guaranteed to have full capability outside of its Recommended Operating Range.

Parameter	Minimum	Maximum	Unit
Operating Junction Temperature Range	-40	+125	°C
Supply Voltage, V_{CC}, PVCC	4.75	5.25	V
Input Supply Voltage, V_{IN}	3	16	V

3.3 Thermal Information

Package Description	Thermal Resistance[1] (Typical, °C/W)			
	Airflow (LFM)	θ_{JA}	ψ_{JB}[2]	$\theta_{JC\text{-}top}$[3]
34 Ld 4x6 QFN L34.4x6	0	12.7	1.4	4.5
	400	10.0	1.5	N/A
34 Ld 4x6 QFN w/ exposed pad L34.4x6E[4]	0	12.5	1.3	1.8
	400	10.0	1.4	N/A

1. These thermal resistances vary with PCB layout, thermal design, and operating conditions. Maximum high-side MOSFET junction temperature is used. A Renesas Demo Board is assumed. See TB379 for general thermal metric information.
2. For ψ_{JB}, PCB temperature is measured at the hottest point on the PCB within 0.2mm of the SPS package. ψ_{JB} can increase slightly with airflow since more heat is transferred to the package top with airflow than without airflow. However, the device equivalent thermal resistance decreases with a reduced junction temperature.
3. For the $\theta_{JC\text{-}top}$, case temperature is measured at the hottest point on the top of the package. It assumes a thermal impedance of 5mW/mK mounting pad and an aluminum heatsink held at 60°C. Therefore, $\theta_{JC\text{-}top}$ is Not Applicable (N/A) with airflow, as the airflow cannot alter the temperature of the constant temperature heatsink.
4. Exposed Top Metal is electrically connected to SW internally. Use non-conductive epoxy to attach to heatsink.

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3.4 Electrical Specifications

Recommended operating conditions, unless otherwise noted. **Boldface limits apply across the operating temperature range, T_J = -40°C to +125°C.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
V_{CC} Supply Current						
Shutdown Bias Current	I_{VCC}	EN = 0V	-	2.2	-	mA
Logic Operational Current	I_{VCC}	EN = 5V	-	5.3	-	mA
Gate Drive Standby Current	I_{PVCC}	PWM = Open, EN = 5V	-	32	-	µA
Gate Drive Operational Current	I_{PVCC}	PWM = 300kHz, EN = 5V	-	13	-	mA
Power-On Reset						
V_{CC} Rising POR Threshold	-	-	-	4.125	**4.3**	V
V_{CC} Falling POR Threshold	-	-	**3.7**	3.875	-	V
V_{CC} POR Delay to Operation	-	V_{CC} = 5V	-	250	325	µs
V_{CC} Rising BD Threshold	-	-	-	4.3	-	V
V_{CC} Falling BD Threshold	-	-	-	4.0	-	V
V_{IN} Rising POR Threshold	-	-	-	2.4	-	V
V_{IN} Falling POR Threshold	-	-	-	2.1	-	V

Recommended operating conditions, unless otherwise noted. **Boldface limits apply across the operating temperature range, T_J = -40°C to +125°C. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Enable Pin						
Enable Rising Threshold	-	V_{CC} = 5V	-	1.7	**2**	V
Enable Falling Threshold	-	V_{CC} = 5V	**0.8**	1.2	-	V
Enable Pull-Down Resistor	R_{EN}	VCC > VCC POR	-	1	-	MΩ
Enable Pull-Down Resistor at VCC POR	R_{EN}	VCC < VCC POR	-	1.25	-	kΩ
GH and IOUT PS4 Exit Latency	$t_{PS4EXIT}$	V_{CC} = 5V	-	13	30	µs
3.3V PWM Input						
Pull-Up (Sink) Impedance	-	-	-	67	-	kΩ
Pull-Down (Source) Impedance	-	-	-	31	-	kΩ
Tri-State Lower Gate Falling Threshold	-	V_{CC} = 5V	-	1.11	-	V
Tri-State Lower Gate Rising Threshold	-	V_{CC} = 5V	-	0.87	-	V
Tri-State Upper Gate Rising Threshold	-	V_{CC} = 5V	-	2.13	-	V
Tri-State Upper Gate Falling Threshold	-	V_{CC} = 5V	-	1.95	-	V
Tri-State Shutdown Window	-	V_{CC} = 5V	**1.3**	-	**1.8**	V
Current Monitor						
IOUT Current Gain Accuracy (Renesas SPS Validation Board, V_{CC} = 5V, V_{IN} = 12V)	-	≥10A, T_J = 25°C to +100°C See Current Monitoring (IOUT) section.	-	±3	-	%
IOUT Terminator Voltage (VT) Range	VCCS	External reference voltage	0.8	1.2	2.0	V
HFET Overcurrent Trip (OCH)	OCH_{TRIP}	-	-	135	-	A
LFET Overcurrent Trip (OCL)	OCL_{TRIP}	-	-	125	-	A
LFET Reverse Overcurrent Trip (NOCP)	$NOCP_{TRIP}$	-	-	-85	-	A
Fault Reset PWM Tri-State Timeout	-	V_{CC} = 5V	-	200	-	µs
IOUT Voltage Level at Faults	-	NOCP	-	2.7	-	V
	-	OCH/OCL	-	2.0	-	V
	-	OTP	-	0.8	-	V
	-	BOOT UVLO, Brownout Detect	-	0.0	0.3	V
Temperature Monitor						
Over-Temperature Rising Threshold	OTP_{TRIP}	-	-	140	-	°C
Over-Temperature Falling Threshold	-	-	-	130	-	°C
TOUT Temperature Coefficient	-	T_J = -40°C to +125°C	-	8	-	mV/K
TOUT Voltage at +25°C Temperature	-	V (T_J) = 0.6V + (8mV*T_J)	-	0.80	-	V

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Recommended operating conditions, unless otherwise noted. **Boldface limits apply across the operating temperature range, T_J = -40°C to +125°C. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
TOUT High at Faults	-	All faults except V_{CC} UVLO and V_{IN} POR	2.5	2.7	2.85	V
TOUT Voltage at SLEEP/PS4 State	-	EN = 0V or VCC UVLO	-	-	0.3	V
Bootstrap Diode						
Forward Voltage Drop	-	5mA	-	90	-	mV
ON-Resistance	R_F	-	-	16	-	Ω

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

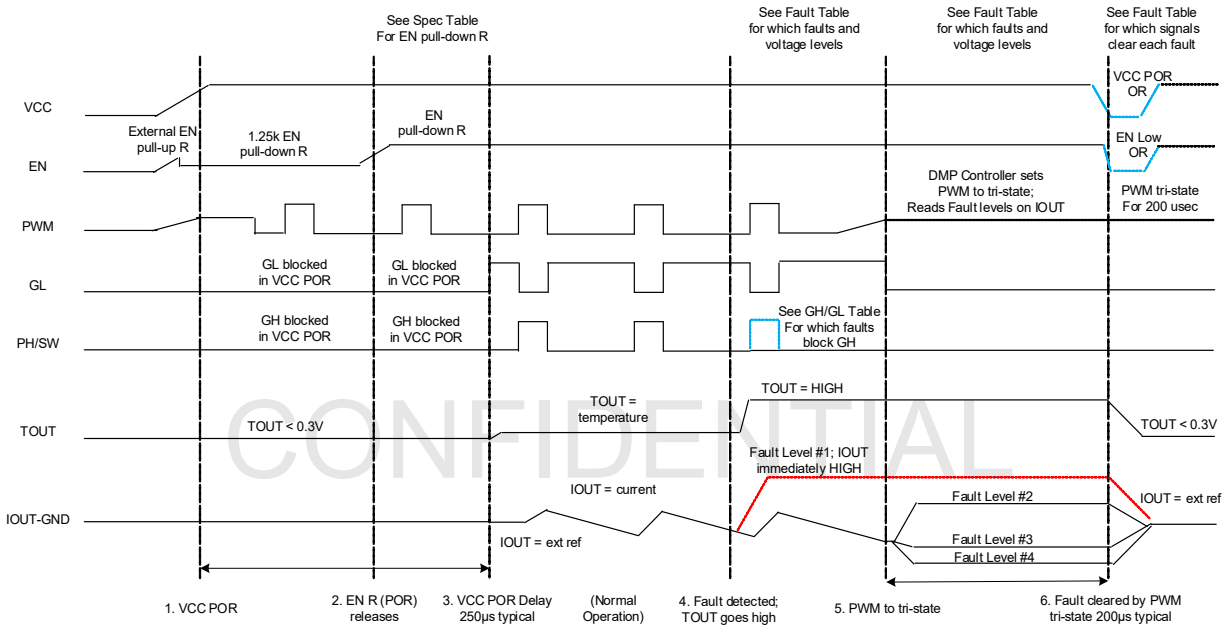


Figure 4. Timing

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4. Typical Performance Curves

V_{CC} = PVCC = 5V, V_{IN} = 12V, f_{SW} = 600kHz, L_{OUT} = (120nH, 0.12mΩ, FP10087R7-R120-R), T_A = +25°C, unless otherwise stated.

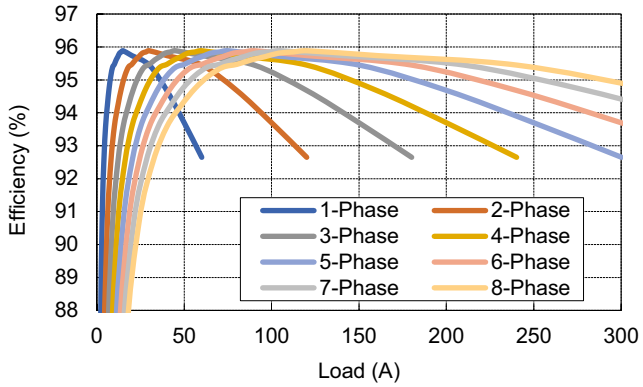


Figure 5. 1.8V Multiphase (APD off) Power Stage Efficiency, including Inductor and excluding 5V Losses (V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 600kHz, L_{OUT} = 120nH)

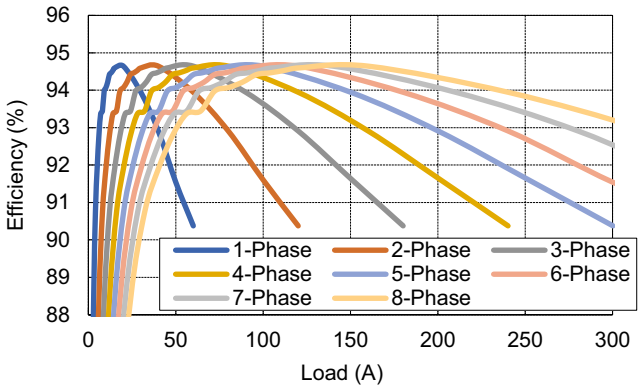


Figure 6. 1.2V Multiphase (APD off) Power Stage Efficiency, including Inductor and excluding 5V Losses (V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 600kHz, L_{OUT} = 120nH)

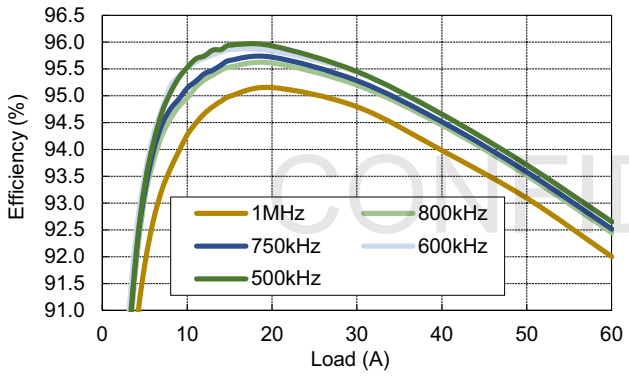


Figure 7. 1.8V 1-Phase Power Stage Efficiency including Inductor and excluding 5V Losses (V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = vary, L_{OUT} = 120nH)

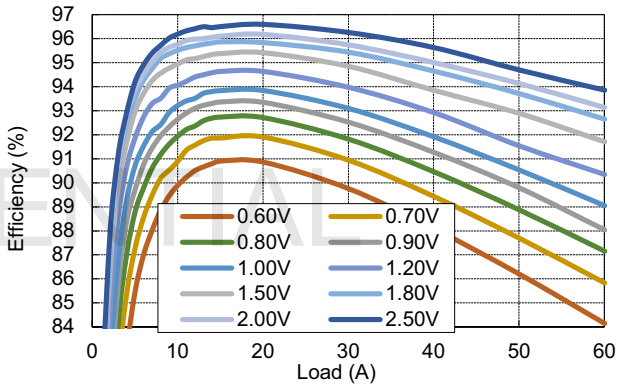


Figure 8. 600kHz 1-Phase Power Stage Efficiency, including Inductor and excluding 5V Losses (V_{IN} = 12V, V_{OUT} = vary, f_{SW} = 600kHz, L_{OUT} = 120nH)

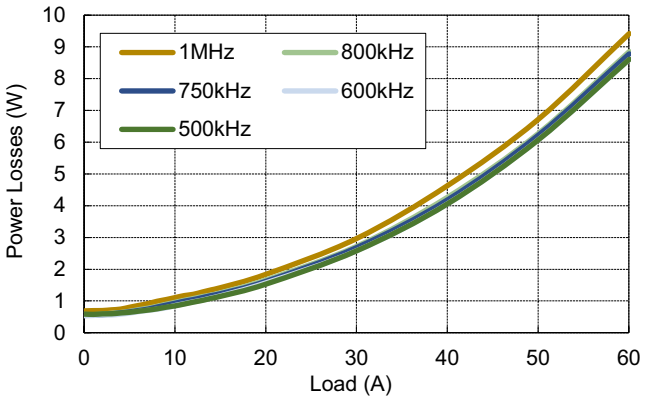


Figure 9. 1.8V 1-Phase SPS Power Losses including Inductor and excluding 5V Losses (V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = vary, L_{OUT} = 120nH)

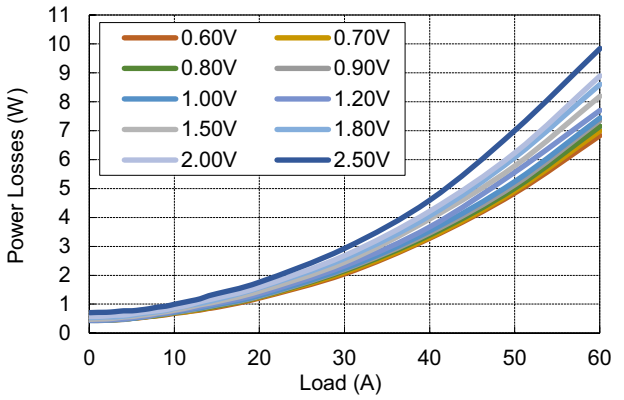


Figure 10. 600kHz 1-Phase SPS Power Losses, including Inductor and excluding 5V Losses (V_{IN} = 12V, V_{OUT} = vary, f_{SW} = 600kHz, L_{OUT} = 120nH)

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5. Operation

The RAA221497 is an optimized power stage solution for high density synchronous DC/DC power conversion. It includes high performance GH and GL drivers, an NFET controlled to function as a bootstrap diode, and a pair of MOSFETs optimized for high switching frequency buck voltage regulators. Figure 4 shows some basic functionality, sequencing, and timing. The figure is illustrative; not all actual system waveforms and the timing and voltage levels are not all to scale. It shows VCC powering up, some normal operation, fault reporting, and several ways to clear faults.

5.1 V_{CC} Power-On Reset (POR) and Brownout Detection (BD)

The V_{CC} voltage is monitored during initial start-up. When the rising V_{CC} voltage exceeds 4.125V (typical) for ~60µs, the 1.25kΩ pull-down resistor on the EN pin is released, and the 1MΩ pull-down resistor takes over.After 250µs (typical) total, normal operation of the driver is enabled, but only if the initial V_{CC} voltage is also above the rising Brownout trip level of 4.3V (typical). If not, normal operation waits until the brownout level is exceeded. Normal operation includes PWM signals are passed through to the gate drivers, the TOUT output is valid, and the IOUT becomes valid on the first GL signal.

When powering down, the V_{CC} voltage first drops below the falling brownout trip level of 4.0V (typical). The Brownout fault is declared; TOUT goes high, IOUT goes to 0V, and GH is gated off but GL continues to follow PWM. The fault clears ~200µs after PWM enters tri-state, or by EN low, or by V_{CC} POR. When V_{CC} drops below the falling V_{CC} POR threshold of 3.875V (typical), the Brownout fault is cleared, operation of the driver is disabled, including switching, TOUT and IOUT. See Table 3 for TOUT and IOUT fault response.

The PVCC voltage is not monitored for either, because it should be from the same supply as V_{CC}.

5.2 Tri-State PWM Input

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The RAA221497 supports a 3.3V PWM tri-level input and is compatible with Renesas digital multiphase controllers as well as other control ICs that use 3.3V PWM logic. If the pin is pulled into and remains in the tri-state window for a set hold-off time, the driver forces both MOSFETs to their off states. When the PWM signal moves outside the shutdown window, the driver immediately resumes driving the MOSFETs according to the PWM commands.This feature is used by Renesas PWM controllers as a method of forcing both MOSFETs off. If the PWM input is left floating, the pin is pulled into the tri-state window internally and therefore forces both MOSFETs to a safe off state.

5.3 Bootstrap Function, Auto Boot Refresh and BOOT UVLO

The RAA221497 features an internal NFET that is controlled to function as a bootstrap diode. Place a high quality ceramic capacitor in close proximity across the BOOT and PHASE pins. The bootstrap capacitor should be 0.1µF (0402~0603 and X5R~X7R) for normal buck switching applications. A resistor in series with the boot capacitor may be recommended, based on the input voltage range in Table 1.

The SPS can refresh the boot capacitor to maintain > 4V V_{BOOT_PHASE} so that it has sufficient $V_{BOOT-PHASE}$ to turn on the high-side FET when it resumes operation.The VIN voltage is required to be ~3V higher than $V_{BOOT-GND}$ for proper operation. Alternatively, the Renesas DMP controller can enable its own boot refresh to maintain sufficient V_{BOOT_PHASE} for all VIN inputs.

There is also a BOOT UVLO circuit that monitors the BOOT voltage. If it falls below its trip point (3.8V typical) for four consecutive PWM cycles, a BOOT UVLO fault is declared and TOUT goes high. See Table 3 for TOUT and IOUT fault response. GH is gated off and GL still follows PWM and turns off upon PWM tri-state sent by the controller. The fault is cleared either 200µs after PWM goes tri-state, or EN low, or V_{CC} POR.

Table 1. R_{BOOT} Resistor Recommendation

V_{IN} DC Range (V)	R_{BOOT} (Ω)
<13.5	0
13.5-15	1
15-16	2

5.4 Low Power States

The RAA221497 supports a low power state that reduces bias current to the minimum level. It enters the Low Power mode when the EN pin is pulled low. The device exits Low Power mode when the EN pin is pulled high and requires 13µs (typically) to resume normal operation. A 1.25kΩ resistor pulls down the EN pin, when VCC drops below its POR, while 1MΩ is always there when VCC is above its POR.

The low power state does NOT reset faults latched before entry. If low power mode is not desired, tie the EN pin to the VCC pin.

5.5 Current Monitoring (IOUT)

The LFET current is monitored and a signal proportional to that current is output on the IOUT pin. An external sink/source voltage source VCCS (typical 1.2V) and a scaling resistor (1kΩ recommended, determined by the controller ADC range) converts the current to a proportional voltage signal. Typically, the SPS gain in the PowerNavigator starts with 4.75mV/A and then goes through IOUT offset and gain calibration to improve IOUT overall accuracy. Contact local Renesas support for IOUT tuning process.

Figure 11 depicts the low-side current sense concept. The IOUT is holding the average current during PWM high and the GL blanking time of ~ 350ns. The IOUT pin output approximates the actual I_L waveform. On start-up after VCC POR, the IOUT outputs zero current (IOUT = VCCS) until the switching begins and the current can be properly measured.

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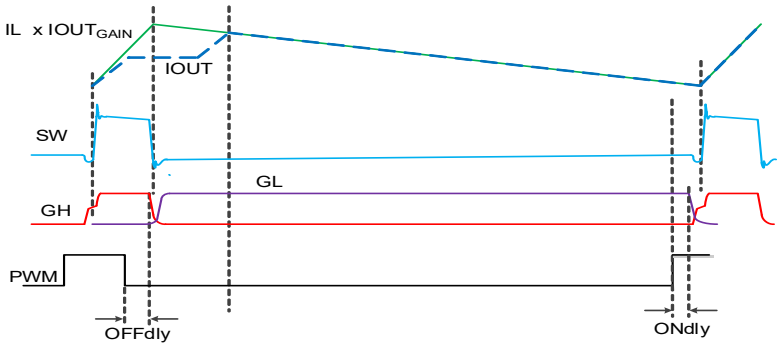


Figure 11. Current Sample Diagram

5.6 Thermal Monitoring (TOUT)

The RAA221497 monitors its internal temperature and provides a signal proportional to that temperature on the TOUT pin. TOUT has a voltage of 600mV at 0°C and reflects temperature at 8mV/°C. The TOUT output is valid 250µs after V_{CC} POR.

Figure 12 shows a simplified functional representation of thermal monitoring. The top section includes the sensor and the output buffer. The bottom section includes the protection sensing that pulls the output high. The TOUT/FLT pin is configured internally so that a user can tie multiple pins together externally, and the resulting TOUT bus assumes the voltage of the highest contributor (representing the highest temperature).

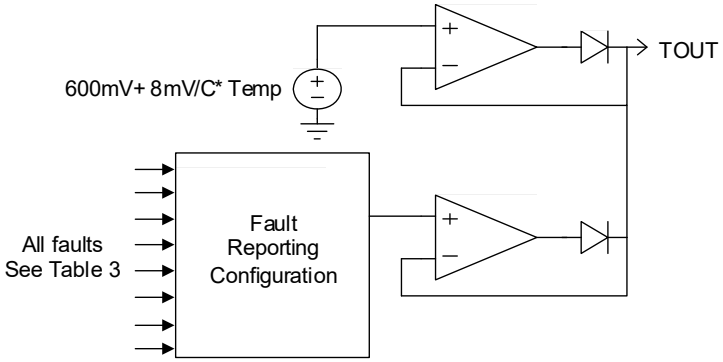


Figure 12. TOUT Fault Reporting Diagram

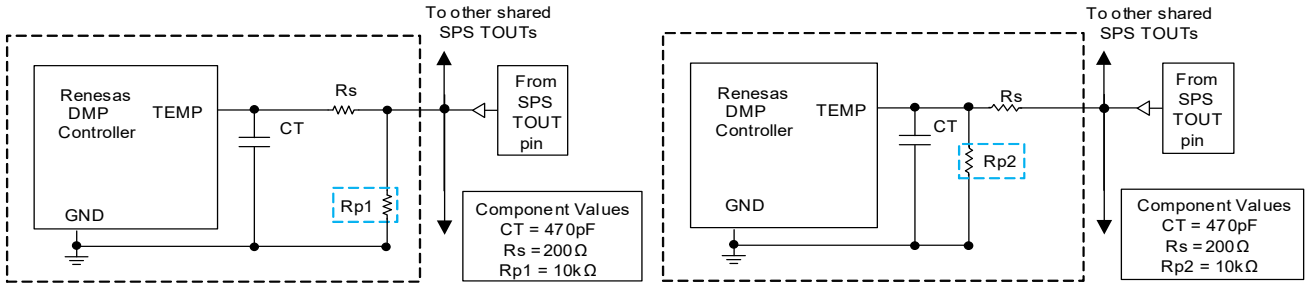


Figure 13. Recommended TOUT Network (Rp1 or Rp2 options)

If any faults are detected, the TOUT/FLT pin is pulled high. On V_{CC} UVLO and EN low, the TOUT/FLT pin is pulled low. See Table 3 for TOUT and IOUT fault response.

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Renesas recommends using a network (470pF capacitor to GND, a series 200Ω Rs, and a parallel 10kΩ Rp) on each common or single TOUT bus to the controller. Locate all components near its controller TEMP input pin and its local GND. Without this network, noise spikes on the SPS GND can potentially overcharge CT. Rs limits the charging of CT to minimize the effect. Rp provides a discharge path for the CT.

Figure 13 shows two options for the network. On the left, Rp1 is on the SPS side of Rs. On the right, Rp2 is on the CT side of Rs. This second option introduces a resistor-divider 2% error to the controller TOUT reading (such as 2°C lower at 25°C; 4°C lower near the SPS over-temperature trip point). As long as this offset is considered in the controller, this configuration can be used with the same results as Rp1.

To modify an existing layout, choose the option that is the easiest to implement based on the board layout, routing options, and the area available. For new layouts, either option is available. Renesas recommends matching existing board designs to be consistent, especially with respect to whether the controller needs to adjust for the offset. The Rp1 option is suggested for new designs to avoid the controller changes.

5.7 Thermal Protection (Over-Temperature; OTP)

If the internal temperature exceeds the over-temperature trip point (+140°C typical), the TOUT/FLT pin is pulled high, and GH is gated off. No other action is taken on chip. The TOUT/FLT pin remains in the fault mode until the junction temperature drops below +130°C (typical), and either 200µs after PWM goes tri-state, or EN low. V_{CC} POR also clears the fault; The TOUT/FLT pin resumes normal operation after the fault is cleared. See Table 3 for TOUT and IOUT fault response.

5.8 Shoot-Through Protection

Before V_{CC} POR, the undervoltage protection function is activated, and both GH and GL are held active low (HFET and LFET off). If the driver has no bias voltage applied (either V_{CC} or PVCC missing) and is unable to

actively hold the MOSFETs off, an integrated 20kΩ resistor from the upper MOSFET gate-to-source aids in keeping the HFET device in its off state. In addition, an integrated 20kΩ resistor from the lower MOSFET gate-to-source aids in keeping the LFET device in its off state. This can be especially critical in applications in which the input voltage rises before the RAA221497 V_{CC} and PVCC supplies.

After V_{CC} POR (see Power-On Reset in Electrical Specifications) and a 250µs delay, the state of EN and PWM control both high-side and low-side MOSFETs, as shown in Table 2.

During switching operation, the RAA221497 dead time control is optimized for high efficiency and ensures that simultaneous conduction of both FETs cannot occur.

Table 2. GH and GL Operation Truth Table

PWM	EN	Fault Event	HFET, LFET
Tri-State	x	x	Both off
0	0	No Fault	HFET off, LFET **ON**
		NOT NOCP	HFET off, LFET **ON**
		NOCP	HFET off, LFET off
1	0	x	Both off
0	1	No Fault	HFET off, LFET **ON**
		NOT NOCP	HFET off, LFET **ON**
		NOCP	HFET off, LFET off
1	1	No Fault	HFET **ON**, LEFT off
		OTP, OCL, OCH, NOCP, BOOT UVLO, BD	HFET off, LFET off

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5.9 Overcurrent Protection (OCH,OCL)

The RAA221497 HFET current is monitored while it is conducting (GH high; also requires V_{IN} above its POR trip point). If the current exceeds 135A (typical), an OCH fault is declared; GH is gated off (even if PWM is still high), effectively shortening the HFET pulse-width and limits peak current. The LFET current is also monitored; if LFET current exceeds 125A (typical), for 8 PWM clock cycles, GH is gated off, and an OCL fault is declared. Either OCH or OCL fault pulls TOUT high. The fault clears ~200µs after PWM enters tri-state or by EN low, or by V_{CC} POR. Then the TOUT flag is released, and the driver normally responds to the PWM inputs. See Table 3 for TOUT and IOUT fault response.

5.10 Negative Overcurrent Protection (NOCP)

The RAA221497 includes a negative overcurrent protection circuit (NOCP) to protect the low-side MOSFET. When an LFET reverse current greater than 85A is detected, the device ensures that GL is gated off for 900ns (typical), to block reverse current build-up, and to avoid high frequency toggling of GL. It also tolerates triggers on three consecutive GL pulses before issuing a fault on the TOUT/FLT going high.

See Table 3 for TOUT and IOUT fault response. The NOCP fault resets only by V_{CC} POR, NOT by EN low nor by PWM tri-state.

5.11 FAULT Reporting

Table 3 provides a description of the device fault reporting behavior. Any detection of over-temperature, overcurrent, BOOT UVLO, BROWNOUT DETECT (BD), or NOCP pulls the TOUT/FLT pin to a high (fault) level so that the PWM controller quickly recognizes it as out of the normal range.The Fault Level #'s in the first column are shown in Figure 4; this table shows the IOUT and TOUT/FLT voltage levels (or N/A) for each fault.

Table 3. Fault Reporting Summary

Fault Event Fault Levels	IOUT	TOUT/FLT	Fault cleared by	Response
OCH/OCL Fault Level #2	2.0V	HIGH (2.7V)	V_{CC} POR **OR** PWM tri-state >200µs **OR** EN low	Both OCH and OCL cause GH to be gated off, GL follows PWM, and TOUT is pulled high. (If system OVP occurs, the controller may send PWM low to turn on LFET).
NOCP Fault Level #1	2.7V	Latched HIGH (2.7V) after timeout	V_{CC} POR	The TOUT is not latched until NOCP is detected for three consecutive GL pulses, while it also continues to monitor HFET short during the NOCP event. It stops responding to PWM high until fault latch is cleared.
OTP Fault Level #3	0.8V	HIGH (2.7V)	V_{CC} POR **OR** [<130 °C **AND** (PWM tri-state >200µs **OR** EN low)]	GH is gated off and GL follows PWM while TOUT is pulled high, when the SPS temperature is above 140°C.The fault is released when the SPS temperature is below 130°C, AND (either after ~200µs after PWM enters tri-state, or by EN low). V_{CC} POR also clears the fault.
BOOT UVLO Fault Level #4	0.0V	HIGH (2.7V)	V_{CC} POR **OR** PWM tri-state >200µs **OR** EN low	If the BOOT voltage falls below its UVLO trip point, for 4 consecutive PWM cycles, TOUT is pulled high, and IOUT is pulled to 0V. GH is gated off and GL still follows PWM and turn off upon PWM tri-state sent by the controller. There is a delay after powering up (and EN going high).
BROWNOUT DETECT Fault Level #4	0.0V	HIGH (2.7V)	V_{CC} POR **OR** PWM tri-state >200µs **OR** EN low	GH is gated off and GL follows PWM; TOUT is pulled high.
V_{CC} UVLO	0µA	LOW	-	Switching stops, IOUT outputs zero current, and TOUT is pulled low while in UVLO. When above V_{CC} POR, after 250µs, GH and GL follow PWM; the TOUT/FLT pin is released; TOUT is valid; IOUT starts at zero current, and becomes valid when GL starts switching.
EN LOW	0µA	LOW	-	Low power mode (Sleep/PS4 State). IOUT outputs zero current.GH is gated off; GL follows PWM to respond any OVP event.

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6. PCB Layout Considerations

Proper PCB layout reduces noise coupling to other circuits, improves thermal performance, and maximizes efficiency. Assume the SPS and inductor are on the top PCB layer. ***Important***: The following guidelines are mandatory for an optimized layout and design to achieve full potentials of the device; any deviation from these should contact local support.

Table 4. Design and Layout Guidelines

AGND-PGND	Directly connected to the ground plane with the shortest distance via. The distance between AGND and PGND (pin 6 on this SPS) must be the shortest, and the open copper area should be minimized in the next layer below the IC (typically, layer 2). See Figure 15 (top layer) for the component placement of the VCC cap. Figure 16 (bottom layer) shows the many GND vias under the SPS. Figure 17 shows the layer 2 GND plane, with those same vias highlighted. The white arrows show the solid metal paths between them on this GND plane (The VIN vias break up part of the path between the arrows). The goal is to minimize the space between the AGND and PGND vias, and provide wide unbroken paths, as best as possible.
VCC/PVCC	The decoupling cap should be next to SPS, on the same top layer, NOT on the bottom layer. Tight loop and minimum trace inductance. Direct GND pad of cap via the ground plane. Combined VCC/PVCC cap into one capacitor provides the best layout and lower components count (when the pins are adjacent or close). Strong common bus if many phases are involved to avoid too much PCB drop; however, a single via is sufficient and can minimize cross-coupling. See Figure 15.
VIN-PGND	Place multiple 10µF or greater ceramic capacitors directly under the SPS between VIN and PGND, as indicated in Figure 14. Also, place 0603 or 0402 1µF/X5R high-frequency decoupling capacitors next to the SPS on the same top layer. See Figure 14 and Figure 15. This is the most critical decoupling and reduces parasitic inductance in the power-switching loop. This reduces overall electrical stress on the device and reduces coupling to other circuits. The best practice is to place the decoupling capacitors on the same PCB side as the device. These decoupling capacitors can be placed under the device for a design with tight space requirements. For example, on the bottom layer, as shown in Figure 16.
BOOT-PHASE	Boot capacitor (and series boot resistor, if recommended) next to SPS, on the same top layer. Tight loop and minimum trace inductance. See Figure 15.
IOUT	The IOUT network and its vias should not sit on the VIN plane; a keep-out area in all layers is recommended (see Figure 15). Avoid routing near switching noise and adjacent to the noise planes (such as VIN). No series resistor to the LDO of the controller. An external resistor from the LDO output to ground might be needed for a very high phase count to the sink current.
TOUT	TOUT output has a 300kΩ weak pull-down and is noise sensitive. Avoid routing near switching noise nodes and adjacent to the noise planes (such as VIN). Renesas recommends using a network (470pF capacitor to GND, a series 200Ω Rs, and a parallel 10kΩ Rp) on each common or single TOUT bus to the controller. Locate all components near its controller TEMP input pin and its local GND, see Figure 13.
EN	Avoid routing near switching noise nodes and adjacent to the noise planes (such as VIN).
SW	Keep on the top layer, avoid multiple layers, and avoid routing any traces below it.
PGND	Connect to the system GND plane with a large via array as close to the GND pins as design rules allow. This improves thermal and electrical performance. See Figure 15.
VIA	The PCB is a better thermal heatsink material than any top-side cooling material. The PCB should have enough vias to connect VIN and GND planes. Insufficient vias yields lower efficiency and very poor thermal performance.
SPACE	Ensure sufficient space between SPS devices to avoid thermal and current crowding, typically 0.350” or more.
Exposed Metal Pad	Electrically connected to SW internally. Use non-conductive epoxy to attach to heatsink.

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Figure 14 summarizes critical design components and layout considerations (as an illustration; it is not drawn to any PCB layout rules), while Figure 15 and Figure 16 show a multiphase PCB layout example (with 4x6 package; a layout for 4x5 package would be similar, with respect to the capacitors). Figure 17 shows the layer 2 (just under the top layer) GND plane, with the VCC cap GND and the SPS PGND vias highlighted and the solid metal paths between them (no traces or vias in the way). Figure 18 shows a contrast between a good layout (left) and a bad

layout (right). The good layout has a GND path around the VIN vias on both sides; the bad layout has no direct path across the rows of vias, creating local voltage drop differences between the AGND and PGND voltages for each SPS.

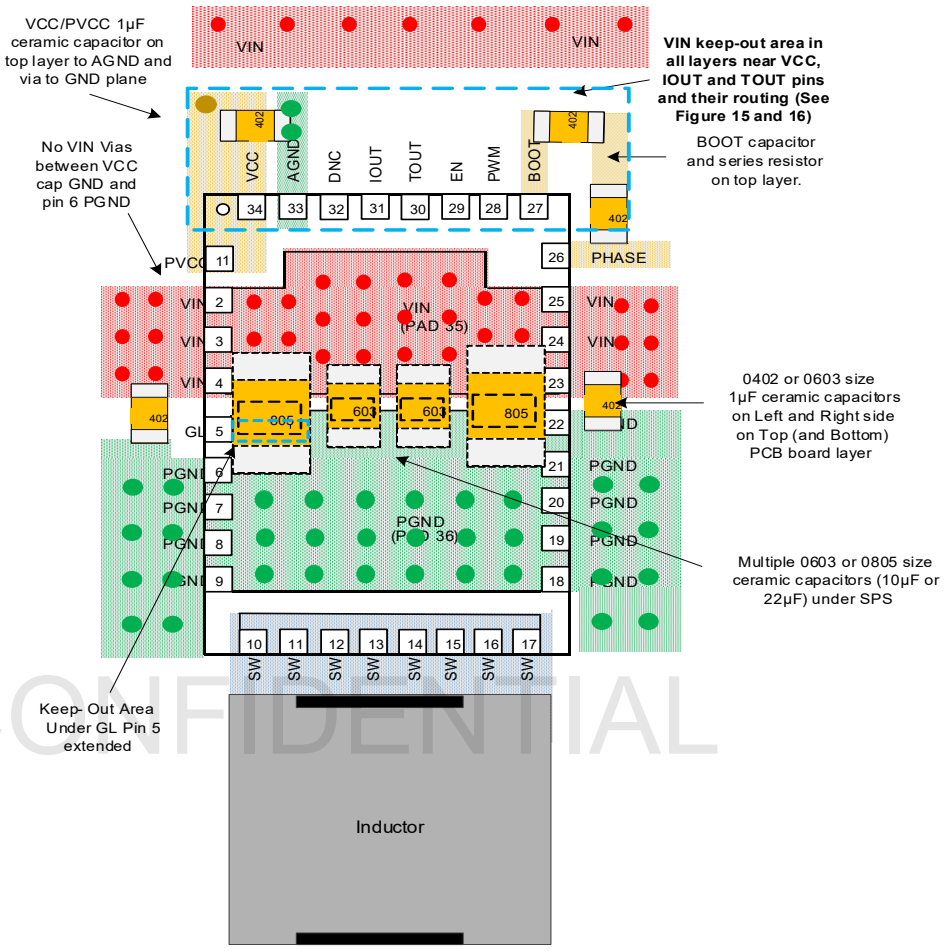


Figure 14. Single-Phase PCB Layout for Minimizing Current Loops

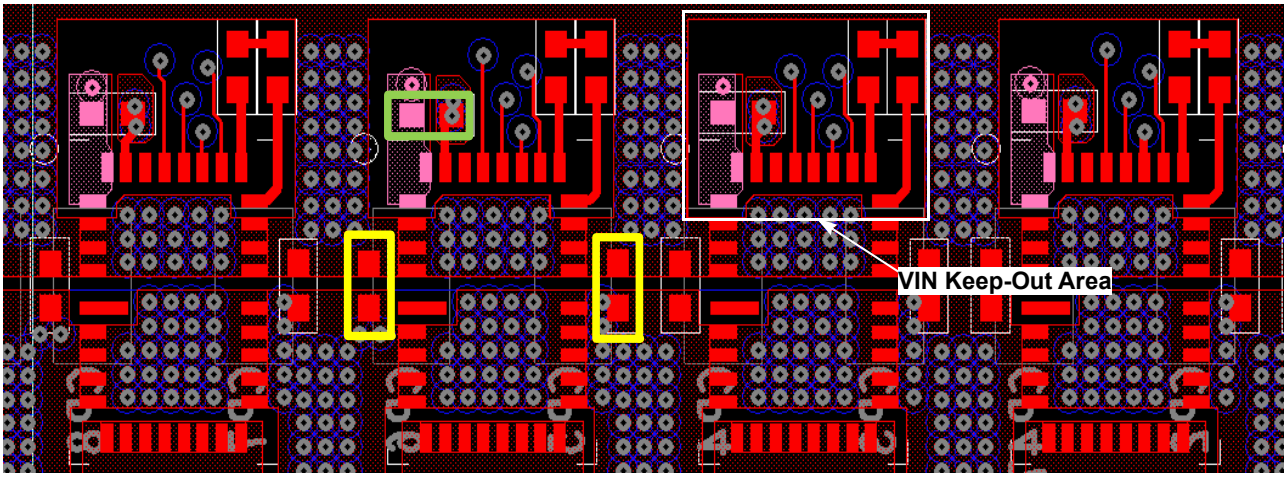


Figure 15. Multiphase PCB Layout Example (4x6 package); Top Layer; 2×1µF VIN Capacitors and a VCC Capacitor

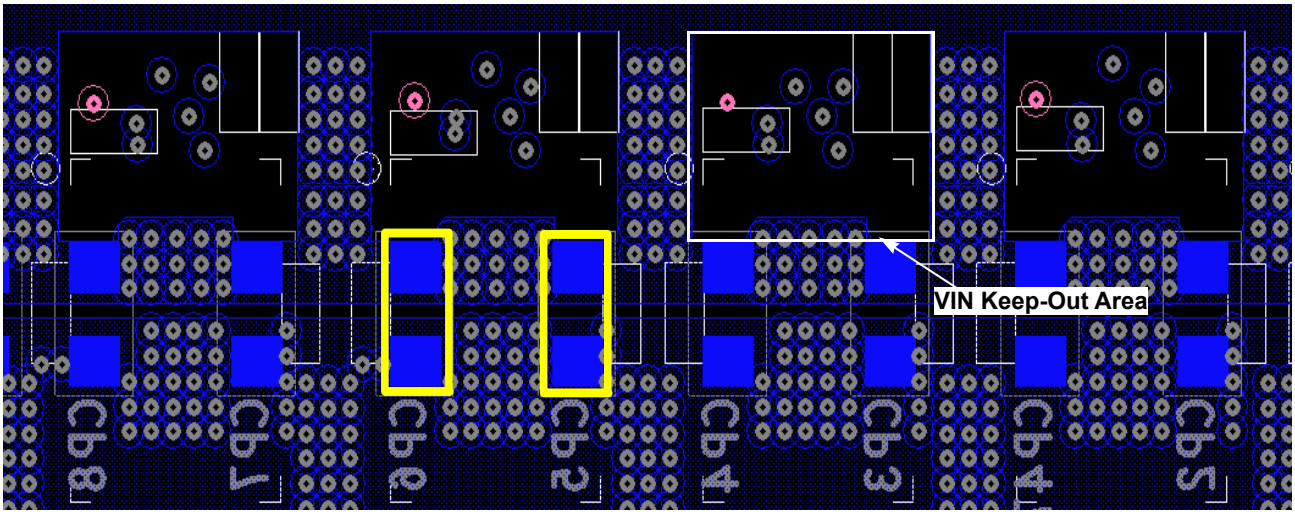


Figure 16. Multiphase PCB Layout Example (4x6 package); Bottom Layer; 2×10 or 22µF VIN Capacitors

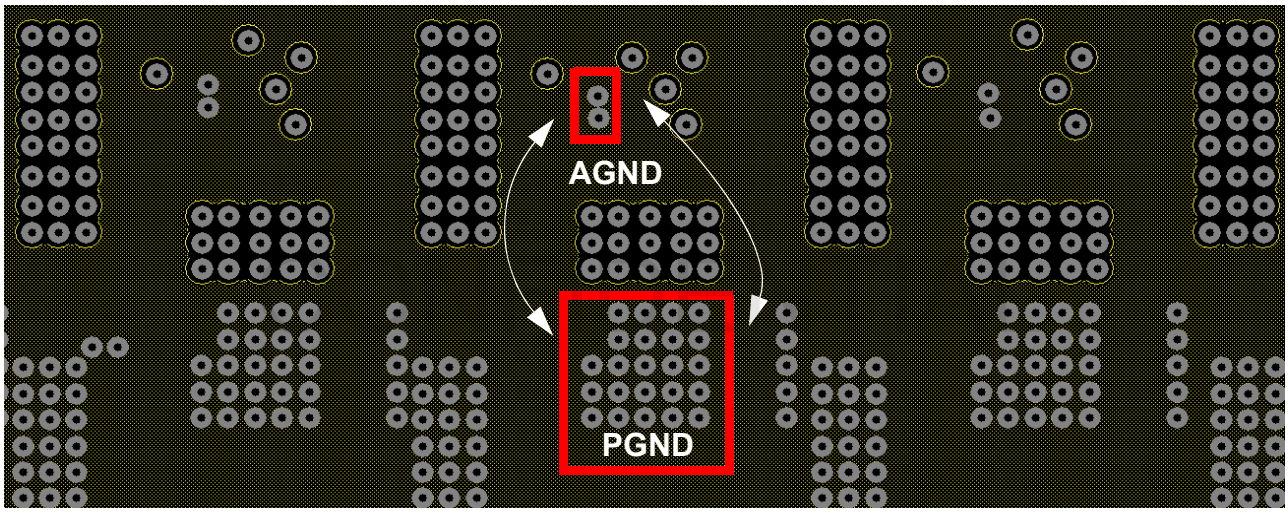
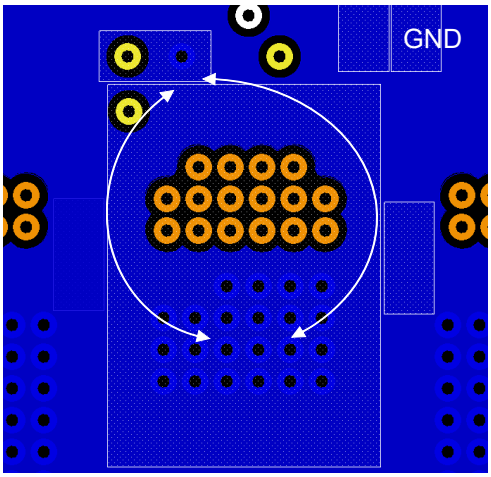
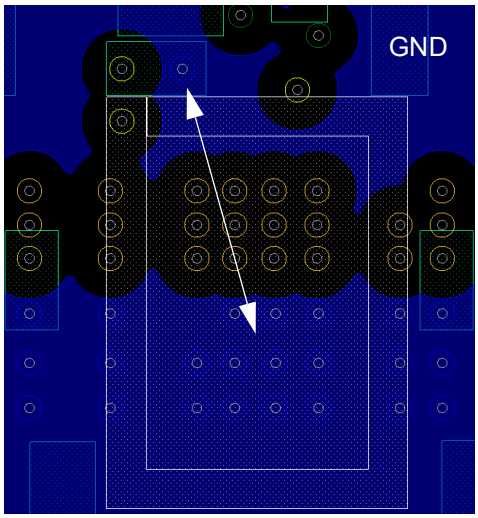


Figure 17. Multiphase PCB Layout Example (4x6 package); Next Layer Below SPS: GND Layer



Good Layout (Well Connected)



Bad Layout (Not Directly Connected)
DO NOT USE

Figure 18. GND Connection Good vs Bad Layout

7. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

8. Ordering Information

Part Number[1][2]	Part Marking	Current Rating	PWM Input	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #[4]	Carrier Type[5]	Junction Temp Range
RAA2214974GNP#HBA	R2214974 HBA	90A	3.3V	34Ld 4x6 QFN	L34.4x6	Reel, 3k	-40 to +125°C
RAA2214974GNP#HBK[6]	R2214974 HBK	90A	3.3V	34Ld 4x6 QFN (Exposed Top)	L34.4x6E	Reel, 3k	-40 to +125°C

1. This product is in compliance with EU Directive 2015/863/EU amending Annex II to EU Directive 2011/65/EU (RoHS) and contains Pb according to RoHS exemption 7a, lead in high melting temperature type solders. These plastic packaged products use 100% matte tin plate plus anneal (e3) termination finish, which is compatible with both SnPb and Pb-free soldering operations. RoHS compliant products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. The Moisture Sensitivity Level (MSL) rating is 3. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. The REF tolerance is ±0.10mm
5. See TB347 for details about reel specifications.
6. Exposed Top Metal is electrically connected to SW internally. Use non-conductive epoxy to attach to heatsink.

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Table 5. Key Differences Among Family of SPS Parts

Part #	Current Rating (A)	PWM (V)	IOUT Mode	FAULT#/EN	Low Power	Package Dwg. #	Pin-to-Pin Compatible
3.3V PWM Power Stage Family							
RAA221320	20	3.3	Voltage	FAULT#	No	L25.4x5	RAA221340
RAA221340	40	3.3	Voltage	FAULT#	No	L25.4x5	RAA221320
RAA221450	50	3.3	Current	EN	from EN	L30.4x5	N/A
RAA221490	90	3.3	Current	EN	from EN	L34.4x6	RAA221497
RAA2214974GNP#HBA	90	3.3	Current	EN	from EN	L34.4x6	RAA221490
RAA2214974GNP#HBK	90	3.3	Current	EN	from EN	L34.4x6E	RAA221490

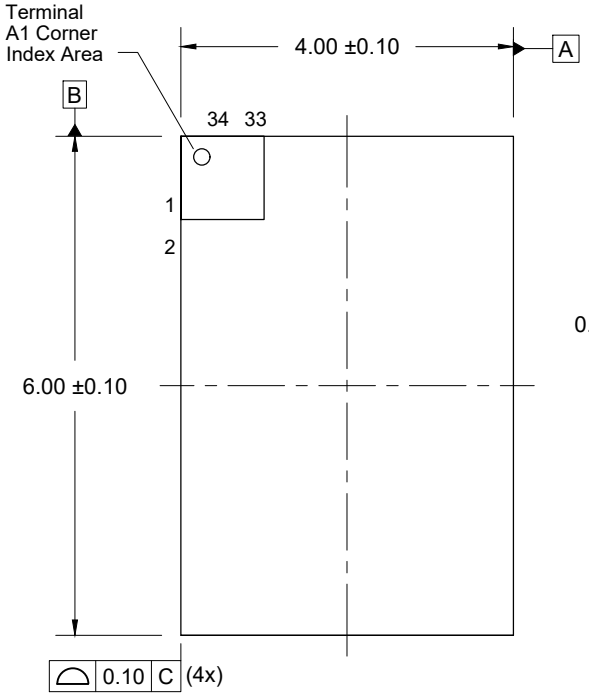
9. Revision History

Revision	Date	Description
1.01	Feb 10, 2025	Updated POD L34.4x6 to the latest version; changes are as follows: ▪ Additional dimensions added to the Bottom View. Cleaned up for clarity. ▪ Additional dimensions added to the Recommended Footprint. Updated POD L34.4x6E to the latest version; changes are as follows: ▪ Corrected the side-view graphic ▪ Added Detail B and corresponding Note 4. ▪ Additional dimensions were added to the Recommended Footprint Pattern per customer request. ▪ Corrected the drawing/dimensions for the exposed pad width (3.6mm to 3.5mm). ▪ Updated the Bottom View dimensions to match/align with the L34.4x6 POD.
1.00	Sep 26, 2024	Initial release.

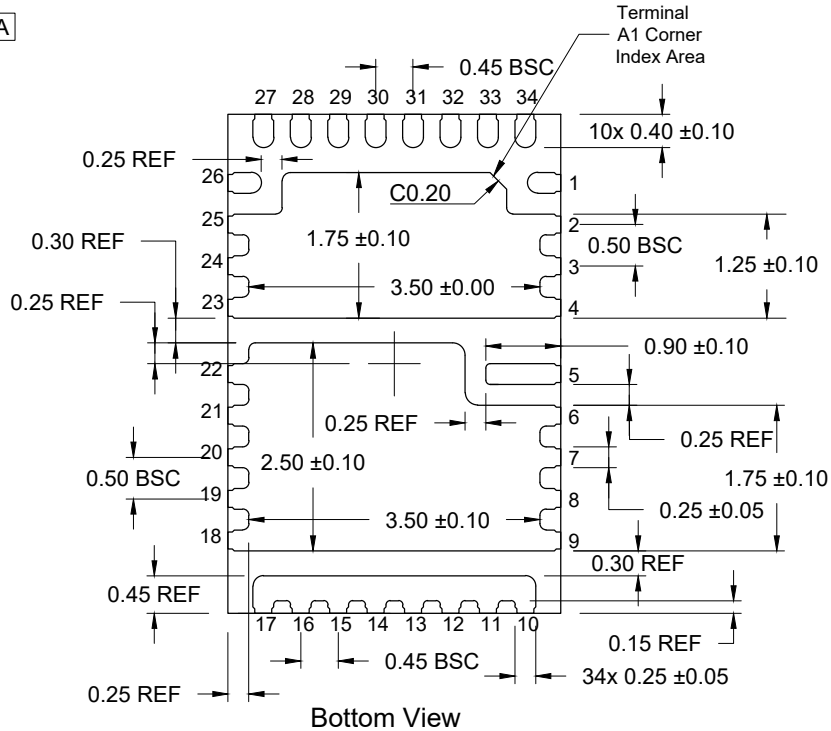
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Package Outline Drawing

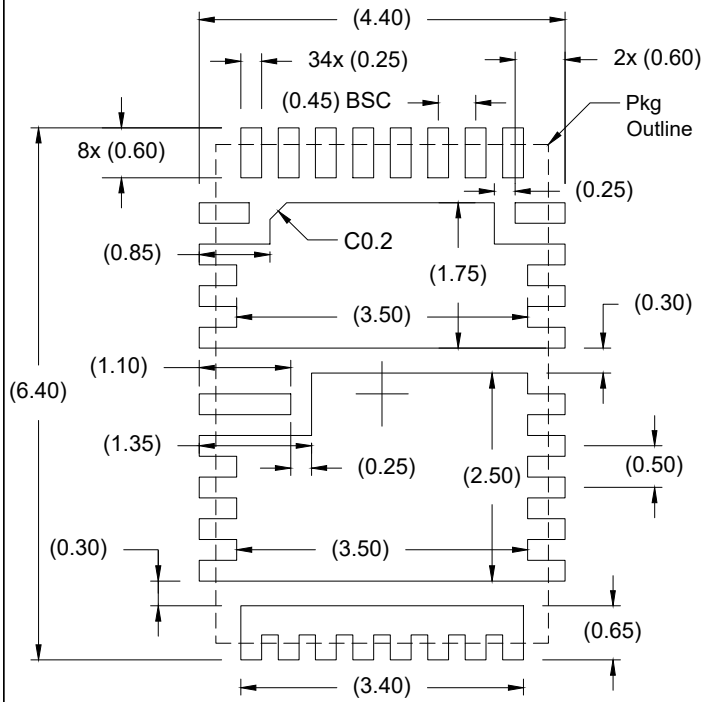
34 Lead Power Quad Flat No-Lead (PQFN) Plastic Package
POD Number: L34.4x6, Revision no: 05, Date Created: Jan 22, 2025



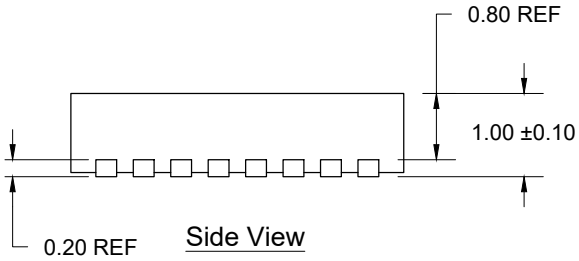
Top View



Bottom View



Recommended Land Pattern



Side View

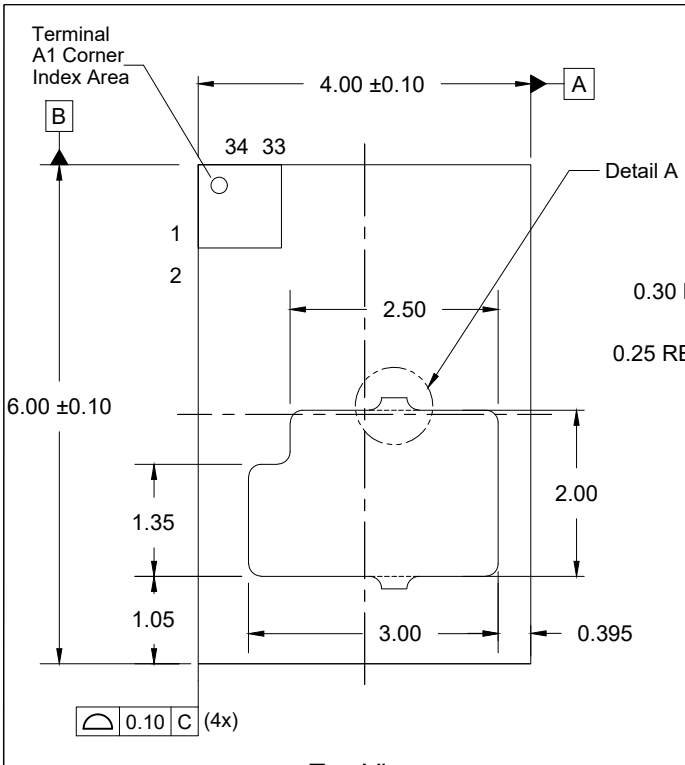
Notes:

1. Dimensioning and tolerancing conforms to ASME Y14.5M - 1994.
2. All dimensions are in millimeters, Dimensions in ( ) for reference only.

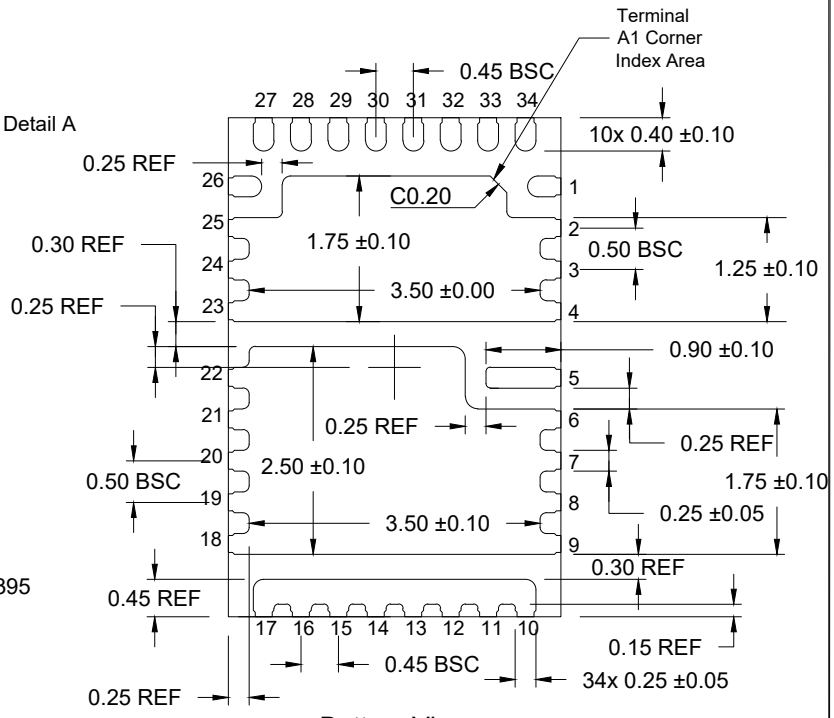
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Package Outline Drawing

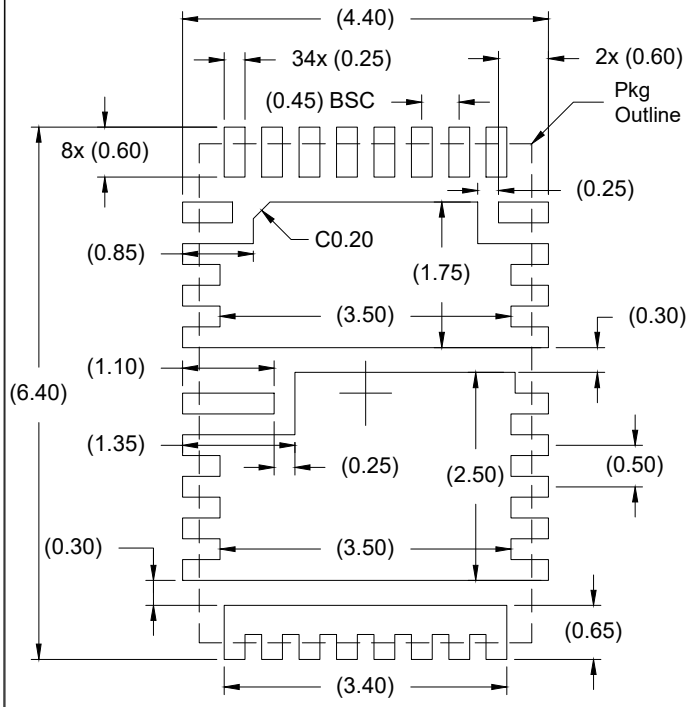
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POD Number: L34.4x6E, Revision No: 05, Date Created: Jan 22, 2025



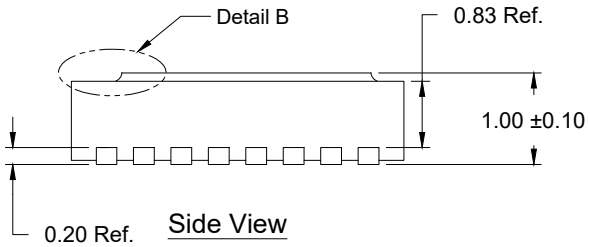
Top View



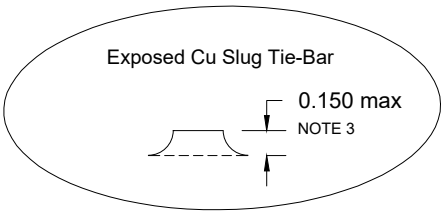
Bottom View



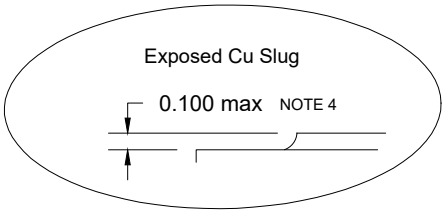
Recommended Land Pattern



Side View



Detail A
SCALE: 2X



Detail B
SCALE: 2X

Notes:

1. Dimensioning and tolerancing conforms to ASME Y14.5 - 1994.
2. All dimensions are in millimeters, Dimensions in ( ) for reference only.
3. Copper slug tie-bar exposure ranges from 0.00mm ~ 0.150mm due to manufacturing variability.
4. Copper slug extension over mold ranges from 0.00mm ~ 0.100mm due to manufacturing variability.

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