NOVOSENSE
纳芯微电子

NSUC1610

High performance micro-controller with Integrated driver for DC, Stepper, and BLDC Motor Controlling

Datasheet (EN) 0.5

Subject to change without notice

Product Overview

The NSUC1610 is an ARM MCU with integrated 4 half-bridge drivers to control low-power DC motors. It can drive DC brushed motors, brush-less motors, stepper motors, etc. And it is widely used in the automotive markets. The chip conforms to the AEC-Q100 standard, and its junction temperature can support up to 175°C. Also, it is integrated with over-voltage protection function, and the LIN port can support -40V~40V, BVDD pin can support -0.3~40V. The core of the chip is Cortex-M3 based on the ARM instruction set. The core adopts Harvard structure and uses independent data bus and address bus, which can improve the efficiency of getting address and data.

Key Features

- ARM Cortex-M3 32bit core
- 64KBytes Flash, 4KBytes SRAM, 512 Bytes EEPROM
- 32MHz high precision oscillator
- 35KHz Low power and low speed clock
- Operating voltage 5.5V~18V
- One 12-bit high precision ADC
- Two 8-bit current-limiting DAC
- Three rapid BEMF Comparators
- One SPI communication support 3 line / 4 line
- One UART peripheral
- LIN PHY module support LIN2.2 communication
- Three 16-bit input capture module
- Two 16-bit timer
- One window watchdog
- One digital watchdog
- Four output half bridge
- Four enhanced PWM output
- A high side drive controlled by software
- One 5V output ALDO
- One 1.8V output DLDO
- Two temperature sensors
- Four working modes: active, retention, idle and sleep mode
- Sleeping power consumption is less than 50 μA with all range of temperature
- AEC - Q100 Grade 0 reliability standard
- ROHS

Applications

- Automotive low power water pump
- Automotive water valve
- Automotive air conditioning pendulum
- DC brush-less motor control
- DC brush motor control
- Stepper motor control

Device Information

Part Number	*Package*	*Body Size*
NSUC1610-Q1QNR	QFN32	5mm × 5mm

Functional Block Diagrams

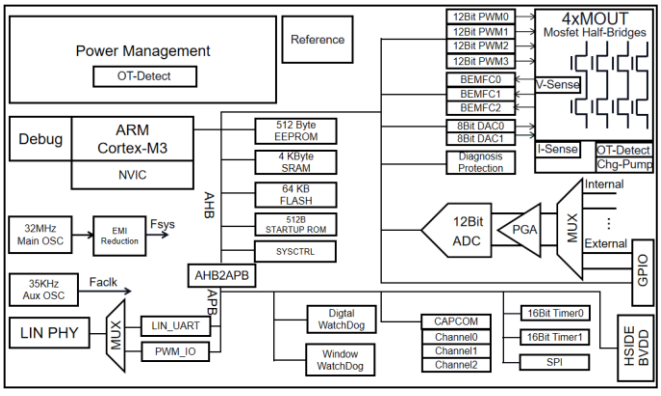


Figure 1. NSUC1610 Block Diagram

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1. Pin Configuration and Functions

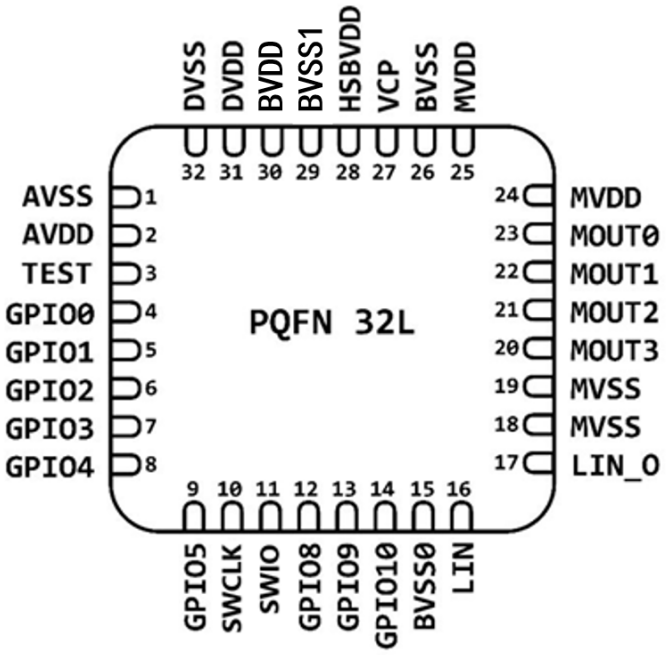


Figure 1.1 NSUC1610 Pin Out

Table 1.1 NSUC1610 Pin Configuration and Description

NSUC1610 PIN NO.	*SYMBOL*	*FUNCTION*
1	AVSS	5V analog power ground
2	AVDD	5V analog power output
3	TEST	Test pin
4	GPIO0	Generic I/O 0
5	GPIO1	Generic I/O 1
6	GPIO2	Generic I/O 2
7	GPIO3	Generic I/O 3
8	GPIO4	Generic I/O 4
9	GPIO5	Generic I/O 5
10	SWCLK	SWD debugging port SWLK
11	SWIO	SWD debugging port SWIO
12	GPIO8	Generic I/O 8
13	GPIO9	Generic I/O 9
14	GPIO10	Generic I/O 10

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15	BVSS0	Battery Ground 0
16	LIN	LIN bus input
17	LIN_O	LIN bus output
18	MVSS	Bridge Ground
19	MVSS	Bridge Ground
20	MOUT3	Bridge output 3
21	MOUT2	Bridge output 2
22	MOUT1	Bridge output 1
23	MOUT0	Bridge output 0
24	MVDD	Bridge power supply
25	MVDD	Bridge power supply
26	BVSS	Battery Ground
27	VCP	Charge pump pin
28	HSBVDD	High-side drive power output
29	BVSS1	Battery Ground 1
30	BVDD	Battery power input
31	DVDD	1.8V digital voltage output
32	DVSS	1.8V digital Ground
33	EPAD	Hot welding pad needs to be connected to GND

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2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit	Comments
BVDD voltage	Vsup	-0.3		40	V	
Bridge ground voltage	VMVSS	-0.3		+0.3	V	
LIN pin voltage	VLIN	-40		40	V	
GPIO pin voltage	VGPIO	-0.3		6.5	V	
MOUT pin voltage	VMOUT	-0.3		40	V	
HSBVDD pin voltage	VHSBVDD	-0.3		40	V	
Storage temperature	$T_{Storage}$	-40		150	℃	
Operating temperature	$T_{operation}$	-40		150	℃	
Junction temperature	Tj	-40		175	℃	
Latch up current	I_latch	-300		300	mA	Tj=125°C, MOUT PINs
		-1000		1000	mA	Tj=25°C, MOUT PINs
		-100		100	mA	Other PINs

3. ESD Ratings

	Ratings	Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD		
	● LIN pins	±8.0	kV
	● Other pins	±2.0	kV
	Charged device model (CDM), per AEC-Q100-011-RevB		
	● All pins	±500	V
	● Corner pins	±750	V

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4. Transient Supply Voltage

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
ISO 7637-2:2004 pulse 1	BVDD	-100			V	1)
ISO 7637-2:2004 pulse 2a	BVDD			75	V	3),7)
ISO 7637-2:2004 pulse 2b	BVDD			10	V	
ISO 7637-2:2004 pulse 3a	BVDD	-150			V	1),4)
ISO 7637-2:2004 pulse 3b	BVDD			100	V	4),5),7)
ISO 16750-2:2012	BVDD			-	V	6)
ISO 16750-2:2012	BVDD			40 400	V ms	
ISO 16750-2	BVDD			28 2	V min	

1) With reverse polarity diode.

2) Reverse polarity diode and 1 µF blocking capacitor with low ESR.

3)According to OEM requirement

4) 4.7 kΩ minimum series resistance for I/O ports.

5) The sum of the whole clamping currents must not exceed 100 mA.

6) Values according to OEM specifications.

7) With TVS diode.

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5. Specifications

4.1 Recommended operating conditions and Characteristics, Note: (TA= -40°C to 150°C)

Parameters	*Symbol*	*Min*	*Typ.*	*Max*	*Unit*	*Comments*
Ambient temperature	TA	-40		150	°C	
Junction temperature	TJ	-40		175	°C	
Thermal resistance (junction to housing)	RthJC		25.4		K/W	θJC-top Surface Temperature contours（JEDEC2S2P）3)
Thermal resistance (junction to the environment)	RthJA		34		K/W	θJA Surface Temperature contours （JEDEC2S2P）3)
Operating voltage range	BVDD	8		18	V	Power supply mode
		5.5		40	V	The performance of analog circuit drops and the motor operation cannot be guaranteed
RETENTION MODE Operating voltage	BVDD	2.5			V	
Half-bridge low-side power supply voltage	MVSS	-0.065		0.3	V	
Half-bridge high-side power supply voltage	MVDD	8		18	V	
Operating current	Isy		10	15	mA	Active Mode，all IO input
			4.6	6	mA	Idle mode Tj<=150°C
			35	50	μA	Sleep mode Tj<=150°C
5V output capacitor	CAVDD		22		nF	AVDD pin
1.8V output capacitor	CDVDD		22		nF	DVDD pin
Charge Pump output capacitor	CVCP		22		nF	VCP pin
BVDD capacitor	CBVDD		1		μF	VBAT pin
Low level of I/O input	VIL			0.3	AVDD	GPIO, TEST, SWD
I/O input high level	VIH	0.7			AVDD	GPIO, TEST, SWD
I/O trigger hysteresis voltage	VHYST	0.5			V	
I/O weak up/down resistance	Rpull		12000		Ω	
I/O input weak drop-down current	IIWPD		50		μA	

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Parameters	Symbol	Min	Typ.	Max	Unit	Comments
I/O input low-level current	IILOW	-5		5	μA	IO_VIN=0
I/O input weak pull-up current	IIWPD		50		μA	
I/O input high-level current	IILOW	-5		5	μA	IO_VIN=AVDD
I/O output low level	VIL			0.4	V	GPIO, TEST, SWD
I/O output high level	VIH	AVDD -0.4			V	GPIO, TEST, SWD
HSBVDD output voltage	VHSBVDD	1		VBVDD-1	V	
MOUT high-edge conduction impedance	RDSON_HS		0.5		Ω	
MOUT low-side conduction impedance	RDSON_LS		0.5		Ω	
MOUT drop-down impedance network	RMOUT		96000		Ω	
Output current	IOUT	-4		4	mA	GPIO
				15	mA	HSBVDD
			1000 (RMS)	1800	mA	MOUT Max Continue current =1A MOUT Peak current=1.8A
LIN bus voltage	VBUS	-2.7		20.7	V	
LIN wakes high-level time	TWHI	1			1/FAUX	
LIN output low level	VBUSOL		0.8	1.2	V	
LIN output high level	VBUSOH	0.8		1	VBVDD	
Internal pull-up resistance	RLIN_UP		38	60	KΩ	
Explicit shutdown current threshold	IBUS_LIM	40		200	mA	VBus=18V, 1)
Input leakage current state 1	IBUS_LEAK_1	1			mA	VBus=0V, VBAT=12V
Input leakage current state 2	IBUS_LEAK_2			20	μA	VBUS>VBAT, 8<VBUS<18, 8<VBAT<18
Input leakage current state 3	IBUS_LEAK_3	-1		1	mA	VGND=VBVDD, 0<VBUS<18, VBAT=12V

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Parameters	Symbol	Min	Typ.	Max	Unit	Comments
Input leakage current state 4	IBUS_LEAK_4			30	μA	VBVDD=VGND, 0<VBUS<18, VBAT=disconnected
Receiving dominant state level	VBUSdom			0.4	VBVDD	
Accept the hidden state level	VBUSrec	0.6			VBVDD	
Intermediate Level Threshold	VBUScent	0.475	0.5	0.525	VBVDD	1)
Receiving hysteresis threshold	VBUShyst			0.175	VBVDD	1)
Duty Cycle 1	D1	39.6			%	Speed=20.0 kbps, THREC(max)=0.744x VBVDD; THDOM(max)=0.581xVBVDD VBVDD = 7.0 V to 18 V; D1 = tBUS_rec(min) / (2 x Tbit)
Duty Cycle 2	D2			58.1	%	Speed=20.0 kbps, THREC(max)=0.422x VBVDD; THDOM(max)=0.284xVBVDD VBVDD = 7.6 V to 18 V; D1 = tBUS_rec(min) / (2 x Tbit)
Duty Cycle 3	D3	41.7			%	Speed=10.4 kbps, THREC(max)=0.778x VBVDD THDOM(max)=0.616xVBVDD VBVDD = 7.0 V to 18 V; D1 = tBUS_rec(min) / (2 x Tbit)
Duty Cycle 4	D4			59.0	%	Speed=10.4 kbps, THREC(max)=0.389x VBVDD THDOM(max)=0.251xVBVDD VBVDD = 7.6V to 18 V; D1 = tBUS_rec(min) / (2 x Tbit)
Delay in receiving	TRX_PD			6	μs	
slave capacitor	CSLAVE			30	pF	
falling slew rate	dV/dTfall		0.8		V/μs	SR=3
			1			SR=2
			1.3			SR=1
			1.5			SR=0
Rising slew rate	dV/dTRise		0.8			SR=3

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Parameters	Symbol	Min	Typ.	Max	Unit	Comments
			1		V/μs	SR=2
			1.3			SR=1
			1.45			SR=0
Wake-up time	TWUP	28		150	μs	VBUS<VBVDD/2-360mv
Auto-addressing constant current source	IAUTO_C	1.0	1.12	1.24	mA	SWC1
		1.85	2.05	2.25	mA	SWC2
		3.15	3.50	3.85	mA	SWC3
LIN shunt resistor	RSHUNT		1		Ω	Test in 0~50° C
Comparator delay	Tdelay		500	550	ns	
Comparator offset	BEMFCoffset		±5	±15	mV	
Comparer hysteresis voltage	BEMFChyst		0		mV	
		5	10	15	mV	1)
		10	20	30	mV	1)
		20	40	50	mV	1)
Comparator input voltage range	BEMFCVin	AVSS		AVDD	V	
Comparator startup time	BEMFCTon			5	μs	
Gain error.	DAC_GE	-1.5		1.5	%	1)
Zero point error	DAC_ZE	-1		1	mV	1)
Difference nonlinearity	DAC_DNL	-1		1	LSB	1)
Nonlinear integration	DAC_INL	-2		2	LSB	1)
PGA common-mode input voltage	PGA_VIC	-0.065		2	V	
PGA differential mode input voltage	PGA_VID	VREF/G		VREF/G	V	
PGA gain	PGA_Gain		1			PGA_Gx=000
			2			PGA_Gx=001
			4			PGA_Gx=010
			10			PGA_Gx=011
			20			PGA_Gx=100
			40			PGA_Gx=101

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Parameters	Symbol	Min	Typ.	Max	Unit	Comments
			Bypass			PGA_Gx=111
Resolution	ADC_RES		12		BIT	
Difference nonlinearity	ADC_DNL	-1.5		1.5	LSB	1)
Nonlinear integration	ADC_INL	-8		8	LSB	1)
Zero error (non-calibration)	ADC_ZE	-5		5	LSB	PGA=1, CHOP=Dis
		-50		50	LSB	PGA=10, CHOP=Dis
Gain error (non-calibration)	ADC_GE	-3		3	%	PGA=1, CHOP=Dis
		-10		10	%	PGA=10, CHOP=Dis
ADC clock frequency	Fadc		32		MHz	
ADC startup time				10	μs	2)
Conversion time	CT		1		μs	
Reference voltage	VREF		2		V	25°C
		1.94	2	2.06	V	
Temperature Errors	TEMPerr	-10		10	°C	
Thermal shut down temperature	TSD	155	165	175	°C	
Thermal shut down return temperature	TSDR	115	130	145	°C	
Main clock	Fmain1	31	32	33	MHz	ERM off
Auxiliary clock	Faux	14	35	56	kHz	
Analog power supply	AVDD	4.5	5	5.5	V	Output Current<25mA
Digital power supply	DVDD	1.62	1.8	1.98	V	Can't be used for external supply
BVDD undervoltage threshold	VBVDDup		6.5	7	V	threshold=00
			7.5	8	V	threshold=01
			8.5	9	V	threshold=10
			9.5	10	V	threshold=11
BVDD undervoltage threshold	VBVDDun	5.5	6		V	threshold=00
		6.5	7		V	threshold=01
		7.5	8		V	threshold=10
		8.5	9		V	threshold=11

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Parameters	Symbol	Min	Typ.	Max	Unit	Comments
BVDD under voltage hysteresis	VBVDDhys	0.3		1	V	1)
BVDD overvoltage threshold	VBVDDop	18.2	19	19.7	V	
BVDD overvoltage threshold	VBVDDon	17.2	18	18.5	V	
Active mode POR threshold	VPOR			5.5	V	2)BVDD pin voltage
Sleep mode POR threshold	VPOR_Sleep	0.5			V	2)BVDD pin voltage
Retent mode POR threshold	VPOR_Retent			2.5	V	2)BVDD pin voltage
TSD mode POR threshold	VPOR_TSD			3	V	2)BVDD pin voltage
Retent mode voltage	VRETENT			5.45	V	2)BVDD pin voltage
EEPROM erasure time	Tee_ers		6		ms	
EEPROM burning time	Tee_pgm		250		μs	
Number of EEPROM burns	NTIMES		1K		Cycles	Tj=175°C, each word
			10K		Cycles	Tj=125°C, each word
			100K		Cycles	Tj=25°C, each word
Number of Flash burns	NTIMES		1000		Cycles	Tj=125°C
Data retention time	TRETENT		3000		h	Tj=175°C
			10		years	Tj=105°C
			20		years	Tj=85°C

1) Parameter is derived from design characterization on a small sample size (mini-char data).

2) Using the checkpoint method for testing minimum or maximum parameter.

3) Parameter is simulated with model of 2s2p board according JEDEC. Values are only valid if the exposed pad is soldered onto the PCB.

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6. Function Description

6.1. Power supply

Novosns NSUC1610 can support the direct use of the 12V power supply of the automobile. The chip is integrated with a high voltage resistant LDO. The on-chip analog module uses 5VLDO for power supply, the digital module uses 1.8VLDO for power supply, and the chip can also support Load-Dump and cold-crank in a low power consumption mode. When NSUC1610 is cold started, when the voltage drops to retention voltage, the data can still be saved to SRAM. In this mode, the digital power supply 1.8V works normally, all peripherals and cores of the processor are in reset state, and the program cannot be executed. When the power supply voltage returns to the normal voltage, the CPU resets the program pointer, starts running from scratch, and records the retention status in the reset source. When the power supply voltage drops below the POR voltage, a POR signal will be generated first, and the chip will return to the normal power on startup mode. At this time, the data in the SRAM area cannot be saved.

6.2. Operating mode

NSUC1610 provides flexible operation modes according to system requirements, including active mode, retention mode, idle mode, sleep mode, TSD mode, and OV/UV mode.

-Active mode: all modules can be used. The CPU can choose 24MHz or 32MHz detection mode: the CPU and all peripherals are in reset state, and SRAM data will be saved - idle mode: the CPU is in reset state, other modules remain in the original state, and can be waked up by LIN port and Wakeup timer.

- sleep mode: the CPU and all modules are in power down state (except LIN port, low-speed clock, and low-power LDO that work normally), Can only be woken up by LIN port

- TSD mode: when the temperature exceeds 165 ° C, the system will enter the overtemperature mode. Only some digital modules are in the active state, and other modules will be turned off. Reduce the power consumption to prevent the chip from overheating.

- OV/UV mode: when the BVDD voltage exceeds the overvoltage threshold, the system will enter the overvoltage mode, and the charge pump will be turned off. The software can turn off other modules to reduce the current consumption. When the BVDD voltage is lower than the undervoltage threshold, the system will enter the undervoltage mode, and the HSBVDD will be turned off. The software can also turn off other modules for on-site protection.

6.3. Temperature detection

The NSUC1610 is internally integrated with two temperature sensors, one of which is used to monitor the overall temperature of the chip. It is used for the system to judge whether to enter the thermal shutdown mode. When the temperature exceeds the threshold, it will enter the TSD Handler interrupt function. The customer can define the software to shut down some modules. When the temperature returns to normal, the TSD flag will be cleared by the hardware. The other temperature sensor is connected to ADC, and the temperature with high accuracy can be obtained through ADC conversion. The customer can use the software method to set a software temperature shutdown threshold and close the module with high power consumption before reaching the hardware thermal shutdown. The temperature sensor can achieve ± 10 ° C within the full temperature range.

6.4. Processor core architecture

NSUC1610 is a processor chip based on ARMCortex-M3 core, which is a 32bit processor based on reduced instruction set and is widely used in automobile systems. The chip architecture is designed based on the Harvard architecture. The data bus and address bus are independent of each other and have three-level pipeline to improve the system operation efficiency, so that the performance of 1.2DMIPS/MHz can be achieved.

The NSUC1610 kernel mainly includes the following modules:

- NVIC: 10 system interrupts, 20 user interrupts, which can be configured into 4 group interrupts, each group has 8 levels of priority

- DAP: AHB-AP&SWD Serial Line Monitoring

- 3 data breakpoints

- 8 Flash patch Power off

NSUC1610 supports SWD serial debugging function and communicates through SWCLK and SWIO (the two Pins are not allowed to be reused into any other function), The SWD port can be locked by burning the SWD protection bit of EE2PROM, so that the program in Flash cannot be read through the SWD port, thus protecting the chip.

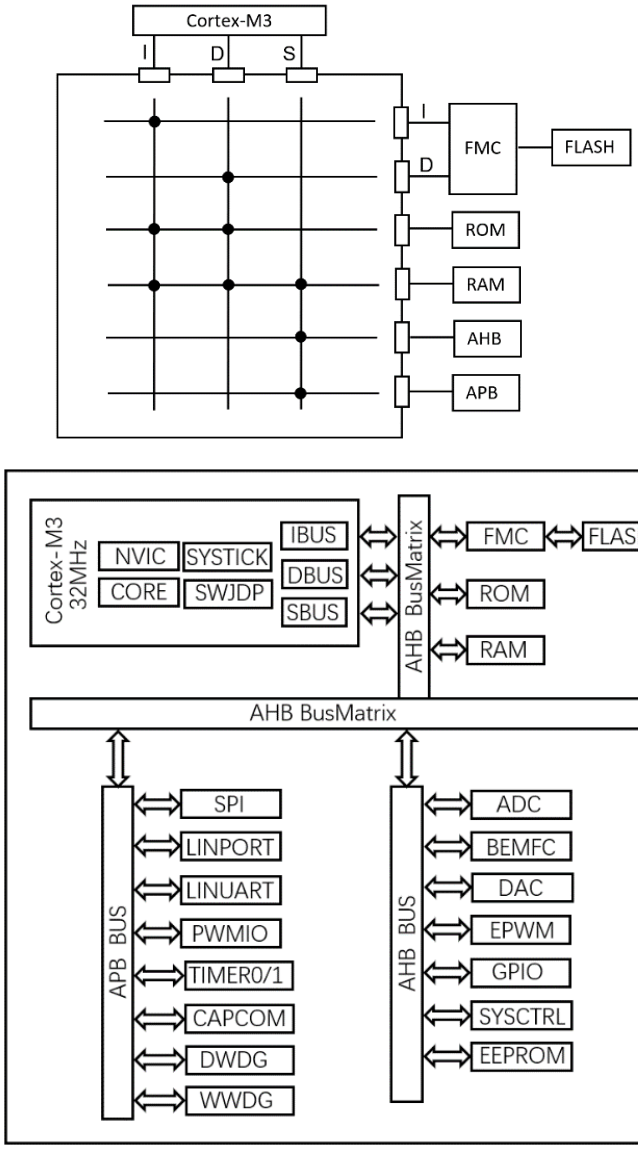
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6.5. Clock system

The NSUC1610 has three clocks. The main clock can be 32MHz or 24MHz. This clock mainly provides the core and digital peripherals with an operating clock (excluding the window watchdog). The secondary clock is 35KHz. This clock mainly provides the window watchdog, the wake-up timer, and the LIN port wake-up module with a clock. When the CPU enters IDLE and SLEEP modes, it can wake up through the wake-up timer module and LIN port. These three clocks are generated by using the RC oscillator principle. 24MHz and 32MHz also have frequency jitter modules. When the modules are enabled, EMI can be reduced.

6.6. Bus system

NSUC1610 integrated bus matrix is mainly composed of AHB bus and APB bus. The core can access Flash, ROM and RAM through I bus and D bus, and access AHB and APB peripherals through S bus. The APB bus is equipped with SPI, LINPORT, LINUART, PWMIO, TIMER0/1, CAPCOM, DWDG, WWDG and other peripherals, and the AHB bus is equipped with ADC, DAC, BEMFC, EPWM, SYSCTRL, and EEPROM, as shown in the figure below:



6.7. Memory address mapping

Program memory, data memory, registers and I/O ports are arranged in a 4GB address space in the same order.

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Each byte is encoded in the memory according to the small end format. The byte with the lowest number in the word is regarded as the least significant byte of the word, while the byte with the highest number is regarded as the most significant byte. Follow ARM ® CortexTM-M3 has the following basic organizational structure for storage:：

Table 5-1 Basic Organization Structure of Memory

Classification	Boundary address	Capacity
ROM	0x0000 0000 - 0x0000 01FF	512B
RAM（ID mapping）	0x1000 0000 - 0x1000 0FFF	4KB
FLASH	0x0800 0000 - 0x0800 FFFF	64KB
FLSAH Controller	0x0802 0000 - 0x0802 0FFF	4KB
RAM（S mapping）	0x2000 0000 - 0x2000 0FFF	4KB

All storage areas that are not allocated to on-chip memory and peripherals are considered "reserved areas". For details about peripheral register mapping, see the following table.

Table 5-2 Chip Peripheral Address Mapping Table

Classification	Boundary address	Peripheral
Reserved	0xE010 0000 - 0xFFFF FFFF	Reserved
Cortex™-M3	0xE000 0000 - 0xE00F FFFF	Cortex™-M3 internal peripherals
Reserved	0x4003 0000 - 0xDFFF FFFF	Reserved
AHB	0x4002 6000 - 0x4002 6FFF	EPWM
	0x4002 5000 - 0x4002 5FFF	BEMFC(Including DAC & CMP)
	0x4002 4000 - 0x4002 4FFF	ADC
	0x4002 2000 - 0x4002 22FF	EEPROM-MEM
	0x4002 2300 - 0x4002 2FFF	EEPROM-REG
	0x4002 1000 - 0x4002 1FFF	GPIO
	0x4002 0000 - 0x4002 0FFF	SYSCFG
APB	0x4000 9000 - 0x4000 9FFF	WWDG
	0x4000 8000 - 0x4000 8FFF	DWDG
	0x4000 6000 - 0x4000 6FFF	CAPCMP
	0x4000 5000 - 0x4000 5FFF	TIMER1
	0x4000 4000 - 0x4000 4FFF	TIMER0
	0x4000 3000 - 0x4000 3FFF	PWMIO
	0x4000 2000 - 0x4000 2FFF	LINPORT
	0x4000 1000 - 0x4000 1FFF	LINUART
	0x4000 0000 - 0x4000 0FFF	SPI

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6.8. Bootstrap configuration

In the chip, different bootstrap modes can be selected through TEST pin, as shown in Table 5-3.

Table 5-3 Bootstrap Mode

Bootstrap mode selection pin	Bootstrap mode	Bootstrap space
TEST/IO9/IO10		
0/x/x	FLASH	Select FLASH as bootstrap space
1/0/0	SRAM	Select SRAM as bootstrap space

6.9. SYSCTRL Module

The SYSCTRL module of NSUC1610 includes system clock control logic, reset logic, system wake-up logic, power control logic, low power consumption control logic, analog configuration logic, chip key lock logic, and chip ID number. Configure CPU clock, ERM module, clock settings and peripherals in debugging mode through the system control (SYSCTRL) module. In addition, the SYSCTRL module also provides control registers for calling power saving modes (IDLE, SLEEP), and control/status registers for resetting/awakening sources and control/status interrupt registers (BVDDUV, BVDDOV) related to BVDD and MON monitoring and returning from idle mode events (RFI).

6.10. GPIO Module

The GPIO of NSUC1610 is a programmable general purpose I/O peripheral, which contains one group of GPIOs, and a total of 11 I/Os. In input mode, each port can enable weak pull-up or weak pull-down resistors. The input of the port will be selected through the burr filter circuit and function multiplexing. The filtered input signal is stored in the data input register (GPIOx_DI). The input signal can also be used to generate GPIO interrupts on the rising or falling edge. In output mode, each port can be configured with push-pull or open drain mode and driven by data output register (GPIOx_DO). Some of the GPIO ports can be used as analog functions. In this mode, the input signals applied to the GPIO ports are sent to the ADC input multiplexer. Note that the range of analog input signals is limited from AVSS to AVDD. In the analog input mode, the digital function of the port is disabled, and the digital input signal is driven to "0". When the pin is configured as output, the value written to the output data register (ODR) will be output on the I/O pin. When the pin is configured as input, the input data register (ODR) captures the data of the I/O pin every 1 CPU clock cycle (FCLK). All GPIO pins have internal weak pull-up and pull-down resistance, which can be determined according to GPIOx_ PUR/GPIOx_ The value in the PDR register is used to select on/off. The specific pin definition abbreviations are shown in Table 5-4, and the multiplexing functions are shown in Table 5-5:

Table 5-4 Abbreviations of pin definitions

Name	Abbreviation	Definition
Pin Name	The pin functions during and after reset are the same as the actual pin names, unless otherwise specified in parentheses under the pin names.	
Pin type	S	Power supply pin
	SO	Power output pin
	I	Input pin only
	I/O	Input/output pin
Pin architecture	TT	5V tolerance I/O
Notes	Unless otherwise specified by notes, all I/Os are set to be suspended during and after reset	
Reuse function	Through GPIOx_ MUX register selection function	

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Table 5-5 Pin Function Reuse Table

No.	PAD Name	PAD Type	I/O Type	Pin Function Description							
				AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7 (ANALOG)
4	GPIO0	I/O	TT	-	-	CAP0_OUT	TIM0_OUT	SPI_CS	TIM0_IN	CAP0_IN	ADC0
5	GPIO1	I/O	TT	-	-	CAP1_OUT	TIM1_OUT	SPI_CK	TIM1_IN	CAP1_IN	ADC1
6	GPIO2	I/O	TT	-	-	CAP2_OUT	SWO	SPI_MOSI	LINUART_RX	CAP2_IN	ADC2
7	GPIO3	I/O	TT	-	-	TIM0_OUT	LINUART_RX	SPI_MISO	TIM0_IN	PWMIO_OUT	ADC3
8	GPIO4	I/O	TT	-	-	TIM1_OUT	LINUART_TX	SWO	TIM1_IN	PWMIO_IN	ADC4
9	GPIO5	I/O	TT	-	-	SYSDBG0	SPI_CS	CAP0_OUT	PWMIO_IN	CAP0_IN	ADC5
10	SWCLK	I/O	TT	-	-	SWCLK	-	-	-	-	-
11	SWIO	I/O	TT	-	-	SWIO	-	-	-	-	-
12	GPIO8	I/O	TT		-	SYSDBG1	SPI_CK	CAP1_OUT	PWMIO_IN	CAP1_IN	VREF+
13	GPIO9	I/O	TT	-	-	SYSDBG2	SPI_MOSI	CAP2_OUT	LINUART_TX	CAP2_IN	VREF-
14	GPIO10	I/O	TT	-	-	SYSDBG3	SPI_MISO	PWMIO_OUT	LINUART_RX	SWO	-
16	LIN	I/O	-	-	-	PWMIO_OUT	TIM0_OUT	LIN_DO	PWMIO_IN	LIN_DI	-
17	LIN_O	I/O	-	-	-	-	-	-	-	-	-

6.11. LIN Port Module

NSUC1610 integrates high-voltage LIN port, supports LIN protocol communication and PWM input/output functions, and has the following characteristics:

- supports LIN 2. X protocol - supports LIN automatic addressing - supports overcurrent protection

- multiple input source multiplexing (PWMIO, UART, LIN_DO)

- IDLE and SLEEP wake-up function

- supports LIN TX timeout shutdown

6.12. High side drive output Module

The NSUC1610 integrates a high side switch, which can switch the voltage on the battery to other peripherals for power supply. For example, in sensor control of the BLDC motors, it can supply power to the external HALL. When over-current occurs, the module also has over-current shutdown function. When an undervoltage event occurs, the module supports automatic hardware shutdown and software shutdown. HSBVDD_Handler interrupt will be triggered in case of overcurrent, and BVDD_UV_Handler interrupt will be generated in case of undervoltage.

6.13. ADC Module

The NSUC1610 integrates a high-precision 16BitADC, which can convert analog voltage from - VREFADC to VREFADC into digital signals. VREF-ADC is derived from internal BandGap voltage. ADC module mainly has the following characteristics:

- 12-bit A/D converter

- 1 μ s fast conversion time/1 MSPS sampling rate

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- input multiplexer with 15 analog channels (LGPIO0 to LGPIO5 single ended, LGPIO4/5 differential, internal temperature sensor VTEMP, motor current detection through the shunt resistor on MVSS0 and MVSS1, differential inputs STDAp/n and STDBp/n for stepper motor locked rotor detection, differential inputs for LIN automatic addressing, etc.)

-The internal reference voltage VREFADC from the internal BandGap

- supports the acquisition queue of automatic sequential conversion with up to eight entries

- Programmable gain amplifier (PGA) with seven gain configurations: 4/11, 1, 2, 4, 10, 20, and 40

- Event driven or time related start trigger source of the optional acquisition queue (software, timer, and EPWM)

- supports the conversion end interrupt and event conflict interrupt

- supports single sequence conversion, continuous sequence conversion, single channel conversion, continuous single channel conversion

6.14. Back EMF comparator module

BEMFC module（that NUSC1610 integrated） has three identical channels for processing the output signal of the BEMF comparator. BEMFC mainly has the following characteristics:

- supports parallel processing of three channels

- supports BEMF voltage zero crossing detection in BLDC motor applications

- supports voltage/current control mode in stepping motor applications

- Each channel's input polarity is programmable

- Each channel's deglitch filter is programmable

- Each channel's blanking filter is programmable and synchronized with the EPWM output signal

- All channels share an interrupt source to CPU, and which is triggered by the rising edge and/or falling edge of the zero crossing detection logic output

6.15. Enhanced PWM module

The NSUC1610 integrates enhanced pulse width modulation (EPWM) module. The EPWM can generate control signals for the built-in power bridge and synchronization signals for the ADC module and BEMF module. It is optimized for BLDC, brush DC (BDC) and bipolar stepper motors control and supports open-loop control (fixed voltage/fixed current) and closed-loop current control with minimum software interaction. EPWM mainly has the following features:

- support BLDC, BDC and bipolar stepper motor control

- support four independent programmable cycles EPWM control module for duty cycle and ADC triggering events

- support PWM duty cycle capture current limiting mode

- support overcurrent and cross current protection of each half bridge

- support PWM minimum conduction time programmable

- support power bridge conversion rate programmable

- support configuration as single or paired half bridge mode

- support configurable register buffer mechanism

- support multiplexer, Select the control signal for the high side/low side switch of each half bridge (fixed as logic "0" or "1", inverse or non-inverse PWM signal)

- four interrupt lines are supported, and each interrupt line is triggered by five interrupt events (cycle end, comparison value matching, trigger value matching, capture event and overcurrent)

6.16. PWMIO module

NSUC1610 integrated PWMIO module supports bidirectional communication through PWM protocol, with minimum CPU interaction. It can generate PWM output signal (PWM out) and measure the high and low time of applied PWM input signal (PWM in). The input and output signals of the PWMIO module are multiplexed to the LIN port and the LGPIO port. PWMIO mainly has the following characteristics:

- Periodic input signal measurement (1Hz to 10kHz)

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- Interruption generated at the falling and rising edges of the input signal, overflow of the input counter and the end of the output cycle

- High and low time measurement

- Optional input deburring filter with 3 μ s filtering time

- LIN pin or PWM signal output with LGPIO replacement function (single pulse, periodic or static)

- Two independent 14-bit counters for input capture and output comparison

6.17. SPI Module

The NSUC1610 integrated serial bus interface provides a SPI communication main interface with bit rates ranging from 125kHz to 16MHz. The clock polarity, clock phase and data order (MSB or LSB first) can be configured, and the data word width of 8, 16, 24 or 32 bits can be selected. SPI module mainly has the following characteristics:

- Serial input and output are connected to external hardware

- 4-wire interface (CS, CK, MISO, MOSI), full duplex

- 3-wire interface (CS, CK, MOSI), Half duplex

- master operation only

- bit rate from 125kHz to 16MHz - programmable clock phase and polarity

- 8, 16, 24 and 32 bit data frames supported by hardware chip selection (CSN)

- chip selection managed by hardware or software (CS)

- programmable data sequence (MSB/LSB priority)

- one receives and one transmit FIFO, each 8 × 8-bit, organized according to data frame width

- RX/TX events or FIFO flags generate interrupts

- can be used to connect external devices, such as EEPROM, external ADC or display

6.18. Timer Module

The NSUC1610 integrated universal timer has two instances of the timer module (TIM0, TIM1), which have the same implementation mode and operate independently of each other. The timer module is based on a 16 bit input clock prescaler and a 16 bit timer counter. The Timer module mainly has the following characteristics:

- Optional input clock: internal or external

- 16-bit input clock prescaler

- 16-bit timer counter

- Optional operation mode: timer, compare or capture

- prescaler, optional buffer for reloading and capturing values

- Optional output signal: static value, PWM signal or timer input signal

- Interrupt triggered by update, compare, capture, and capture overcurrent events

6.19. CAPCOM Module

The NSUC1610 integrated capture and comparison unit module has a capture and comparison unit (CAPCOM), which is optimized to capture and process up to three channels in parallel, such as three Hall sensor signals for sensor based six step BLDC motor control. The comparison function can be used to generate up to three output signals, which can be multiplexed to the IO port through the GPIO function. The capture and comparison module mainly has the following characteristics:

- three input channels - 16-bit clock prescaler

- 16-bit free running CAPCOM counter

- 16-bit capture and comparison registers for each channel

- rising edge Input capture event on falling edge or double edge

- advanced capture mode with input mode comparison - optional cache of configuration register

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- three independently configurable output signals (static is logic "0", triggering comparison and/or overflow event)
- one middle break per CAPCOM channel, triggered by overflow, comparison, capture and capture overflow events
- Function description of additional right/wrong mode detection events for channel 0

6.20. DWDG Module

The NSUC1610 integrated digital watchdog has the characteristics of high security and flexible use. It can be used to detect and solve faults caused by software errors, and trigger the system reset when the timer reaches the specified timeout value. DWDG mainly has the following features:

- 16-bit down counter
- clock supports 4 to 512 frequency division
- reset when down counter value reaches 0x0 (if watchdog is activated)

6.21. WWDG Module

The NSUC1610 integrated window watchdog (WWDG) clock is provided by the APB clock after pre frequency division. The window watchdog is usually used to monitor the abnormal late or early operation of the application through a configurable time window. Software failure caused by external interference or unpredictable logic conditions that cause the application program to deviate from the normal operation sequence. Unless the value of the down counter is refreshed when it is greater than the window value, a system reset will be generated when the preset time period is reached. If the down counter is smaller than the window register value, a reset will also be generated. This means that the counters must be refreshed within a limited time window. WWDG mainly has the following characteristics:

- Free running down counter
- Reset when the down counter value counts to 0x0 (if the watchdog is activated)
- Reset when the down counter is overloaded in the window (if the watchdog is activated)

6.22. UART Module

The NSUC1610 integrated full duplex universal UART module can process 8-bit data with or without parity and one or two stop bits. The bit timing logic allows the necessary bit rate to be adjusted in the bit stream to synchronize to the LIN bit rate with the minimum residual error. The module has two 8-byte fifo for data reception and transmission. The bit rate adjustment logic can be used to automatically synchronize the UART bit rate to the LIN master bit rate. The enhanced features are optimized for the LIN slave mode. The UART module has the following features:

- 8bit frame
- parity check
- baud rate automatic adjustment
- support TX, RX, FIFO empty, FIFO full, frame error, TX and RX loop error, break and sync interrupt
- break and sync automatic detection of two independent transmit receive FIFO
-LIN modes
- automatic LIN packet header reception

6.23. Flash Module

NSUC1610 integrated FLASH has 64KB storage space for storing application code and data. Read access to FLASH supports zero wait execution. The default programming mode of FLASH is to operate by page, while the default erasing mode is to execute by sector. The Flash module has the following features:

- 64KB storage space
- supports ECC correction, one check and two check
- supports zero wait fast read access

6.24. EEPROM Module

The NSUC1610 integrated EEPROM is used to store non-volatile application data. Of the 512 bytes of the EEPROM, 448 bytes are the client area, and the remaining 64 bytes are the FAB manufacturer area. The EEPROM module has the following characteristics:

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- 512 bytes in size, 448 bytes for application data
- divided into 128 Word storage

6.25. MOUT Module

NSUC1610 integrated MOUT port is driven by N/N channel half bridge for direct motor drive (such as brushless motor or brushless DC motor or bipolar stepping motor). Each half bridge is composed of two n-channel power FETs, which are respectively used as the low side of motor grounding (MVSS0/1) and the high side of motor power supply (MVDD0/1). The power MOSFET is driven by an internal gate driver controlled by the EPWM module. The diagnostic module monitors the gate voltage of the power field-effect transistor and provides a signal for the EPWM module to achieve short-circuit current protection. In addition, the over-current condition can be detected through the current monitoring of the power FET. If the over-current condition occurs in the EPWM module, all four half bridges can be closed or only the affected half bridges can be closed, and over-current interruption will occur. The MOUT module has the following characteristics:

- four N-N Mos half bridges
- internal integrated over-current protection monitoring
- the high side is driven by charge pump, and supports 100% duty cycle conduction
- integrated resistance network and three back EMF comparators, Support non inductive BLDC drive
- integrated current limiting DAC, support step motor subdivision drive
- support low side single resistance, dual resistance network, can be used for ADC of current
- support automatic shutdown in sleep, retention, tsd modes

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7. Application note

6.1. Typical application circuit of Stepper Motor Controlling

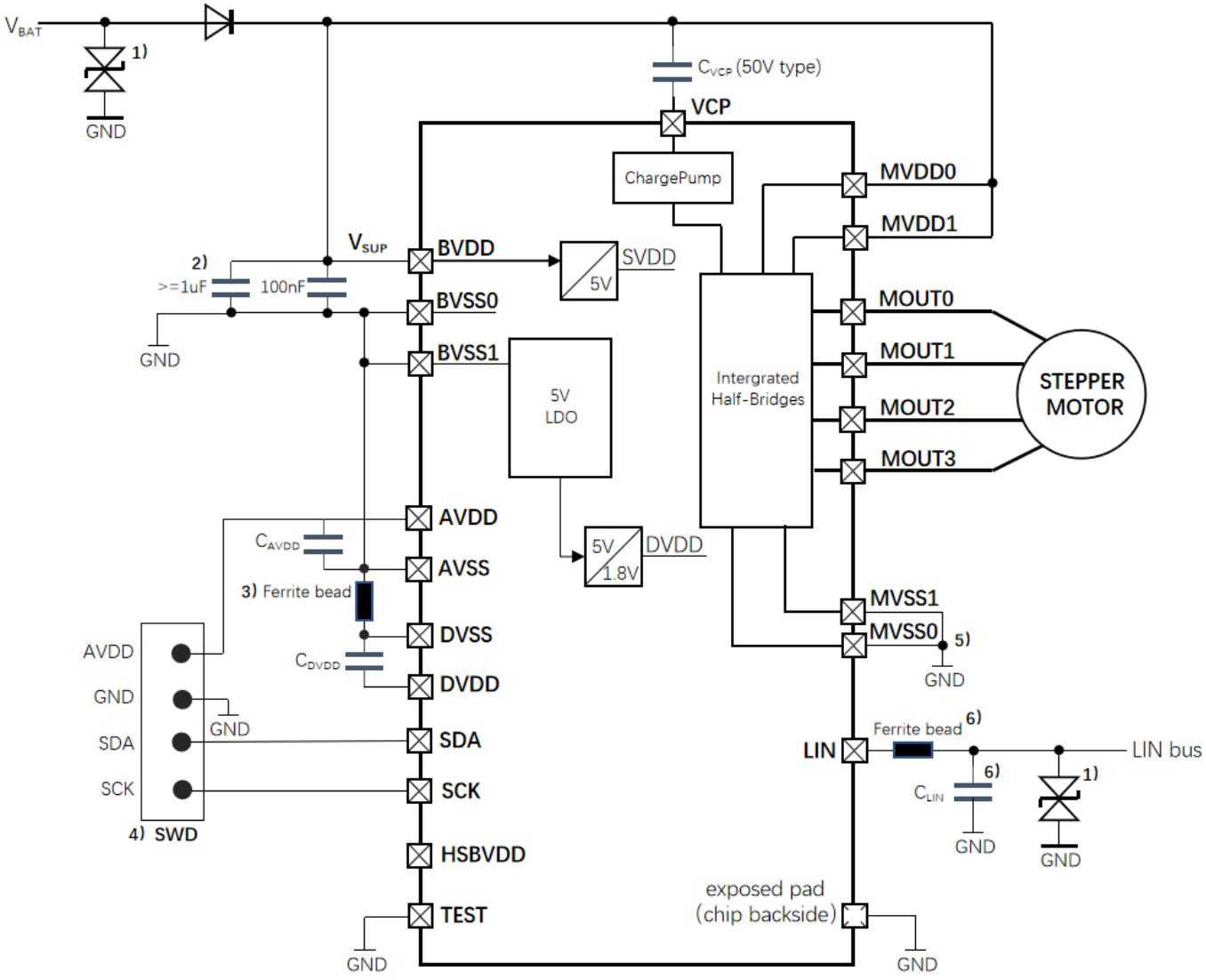


Figure 6.1 Typical application diagram

1） TVS diode or decoupled capacitor is recommended with respect to ISO7637-2 Pulse 2a.

2） Decoupled capacitor on BVDD should be considered by different application, such as the voltage of BVDD is under voltage then you need use bigger capacitor while writing some data in EEPROMNVRAM.

3） Ferrite bead is referred to requirements of OEM and the demo solution of Novosense doesn't need to add this bead.

4） SWD is used for debugging code or downloading code into flash.

5） Don't need extra shunt resister here as we have integrated current sensor in every half-bridge.

6） Ferrite bead and decoupled capacitor on LIN bus should take care for EMC standard or refer to requirements of OEM.

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6.2. Typical application circuit of BLDC Motor Controlling

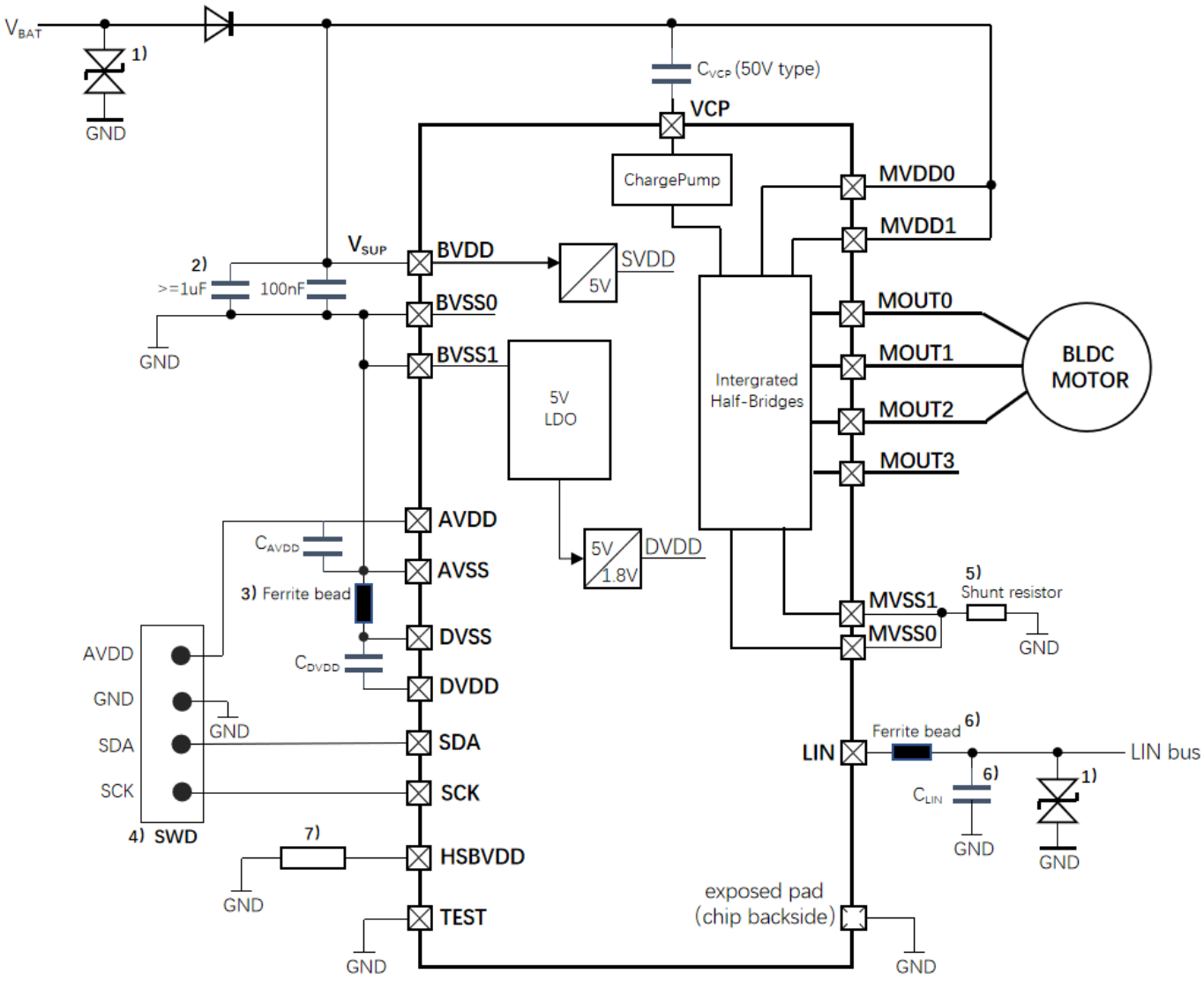
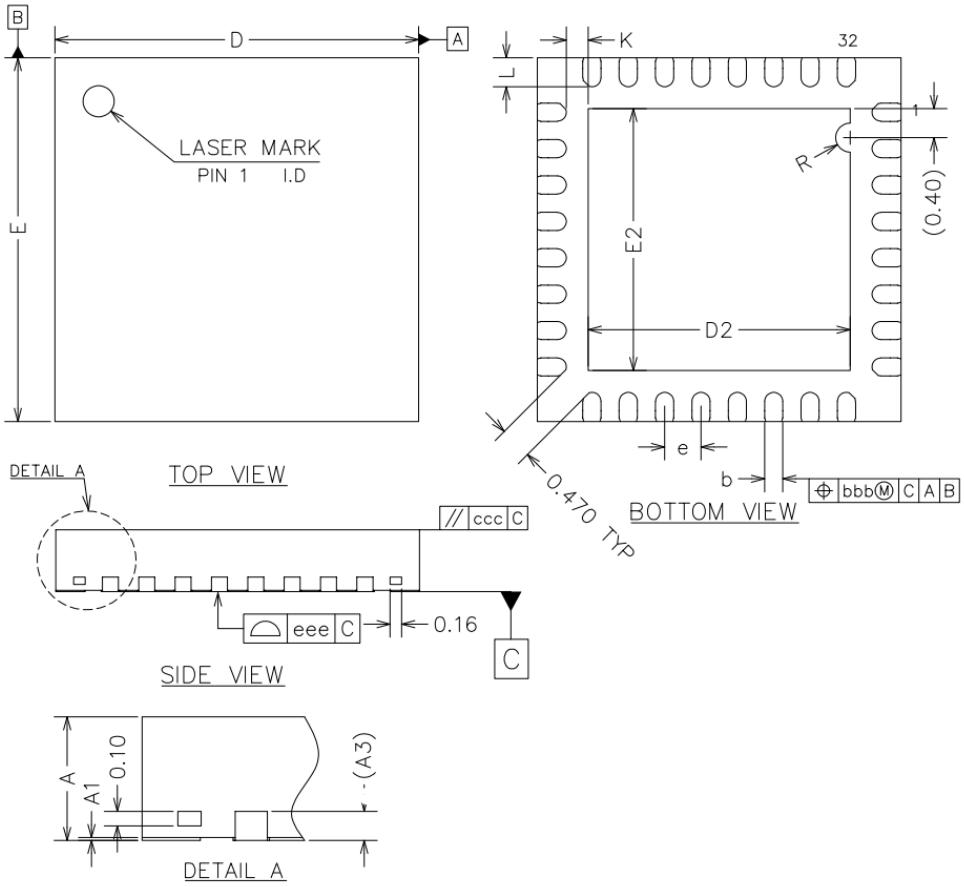


Figure 6.2 Typical application diagram

1) TVS diode or decoupled capacitor is recommended with respect to ISO7637-2 Pulse 2a.
2) Decoupled capacitor on BVDD should be considered by different application, such as the voltage of BVDD is under voltage then you need use bigger capacitor while writing some data in EEPROMNVRAM.
3) Ferrite bead is referred to requirements of OEM and the demo solution of Novosense doesn't need to add this bead.
4) SWD is used for debugging code or downloading code into flash.
5) Don't need extra shunt resister here as we have integrated current sensor in every half-bridge.
6) Ferrite bead and decoupled capacitor on LIN bus should take care for EMC standard or refer to requirements of OEM.

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8. Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.50	3.60	3.70
E2	3.50	3.60	3.70
e		0.50 BSC	
R		0.20REF	
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–
bbb		0.10	
ccc		0.10	
eee		0.08	

Figure 7.1 QFN32(5*5) Package Shape and Dimension in millimeters and (inches)

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9. Order Information

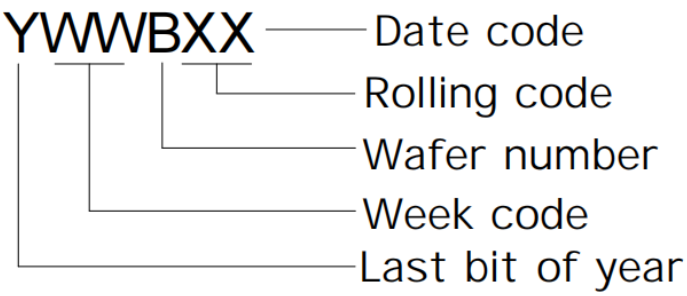
Standard Ordering Item No.:

Part Number	*Temperature*	*Flash Size (KB)*	*SRAM Size (KB)*	*Power Supply Voltage (V)*	*Package*	*MSL*	*SPQ*
NSUC1610-Q1QNR	-40~150℃	64	4	12	QFN32(5*5)	MSL1	5000

*Other order part numbers are acceptable. If you need other specifications, please contact Novosense for special support.

Marking rules:





10. Revision History

Revision	Description	Date
0.0	Initial Version.	2022/12/15
0.1	Update the POD picture & Product Number name	2023/08/12
0.2	Add MSL & SPQ	2023/10/7
0.3	Update RthJA & RthJC	2023/11/20
0.4	Modify some descriptions of different block	2023/12/20
0.5	Modify ESD style for new template & Marking rules	2023/12/28

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