Features

- 3 input reference clocks
  - Two differential clock pair up to 3.1GHz, accepting single-ended clock source up to 350MHz
  - One crystal input, accepting 8MHz to 50MHz crystal or single-ended clock source
- 4 output clocks:
  - Two power banks with 2 differential outputs each, supporting LVPECL, LVDS and LP-HCSL
  - One independent LVCMOS output clock
- Frequency range:
  - LVCMOS: DC to 350MHz
  - LVDS: DC to 3.1GHz
  - LVPECL: DC to 3.1GHz
  - LP-HCSL: DC to 1GHz
- Excellent PSRR :
  - LVDS: -74dBC @156.25Mhz
  - LVPECL: -67dBC @156.25Mhz
  - LPHCSL: -76dBC @156.25Mhz
- Ultra-low latency and skew
- Additive Jitter:
  - 34 fs RMS (12kHz to 20MHz) typical @LP-HCSL 156.25MHz
  - 10 fs RMS typical @ PCIe Gen5 jitter (CC)
- Three independently configurable 1.8V-3.3Vpower supplies for:
  - Core
  - Differential outputs
  - Single-ended outputs
- Pin-based control for flexible input reference selection and output enable/disable
- Glitch-free switchover supported in the "G" version
- Working temperature: -40°C to +85°C
- Package: 32-pin WQFN

1.SYKB*****: No glitch-free switchover.
2.SYKB*****G: Includes glitch-free switchover.
3.F: Supports LVPECL, LVDS, and LP-HCSL differential clock outputs.
4.Unless otherwise stated, the terms "clock buffer" and "buffer" refer to the entire series.

General Description

SYKB23F04(G)[1,2,3,4] is a type of high-performance clock fanout buffer operating at up to 3.1GHz with 4 outputs. The buffer is designed for low-jitter, high-frequency clock/data distribution and level translation.

The buffer supports clock input selection from either two differential clock pairs or one crystal input, distributing the selected clock to two output banks, each with 2 differential outputs, along with a dedicated LVCMOS output. Both differential output banks can be configured as LPPECL,LVDS,LP-HCSL or disabled

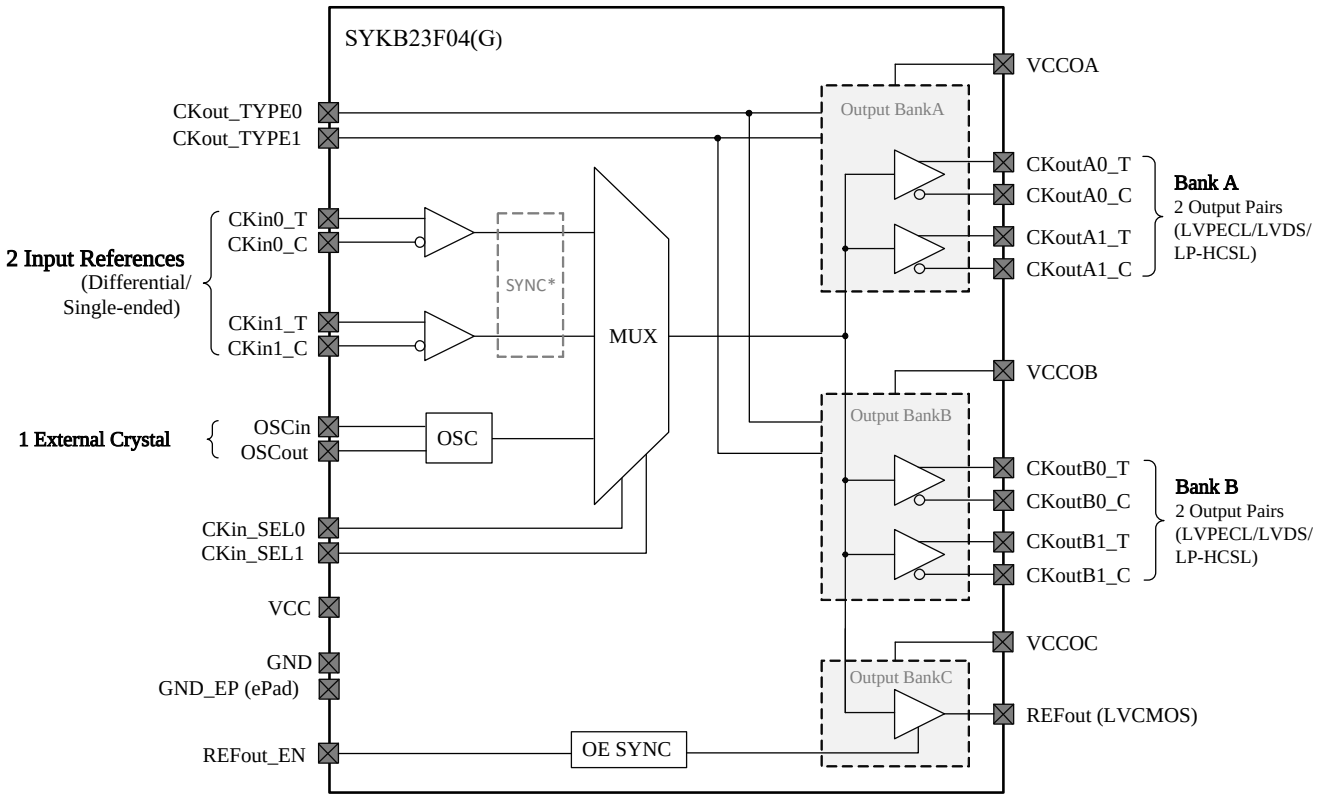
Operating with a core supply of 1.8V-3.3V and three independent output supplies of 1.8V-3.3V, the clock buffer provides flexible control via logic pins for input reference clock selection and output enable/disable functions.

The buffer can be paired with SYNK Technology’ s SYKG010xx clock generator to deliver a robust clock tree solution. With broad input and output frequency ranges, optimized power management, and reduced propagation delay, the buffer operates across a wide temperature range, making it an ideal choice for demanding applications.

Applications

- PCIe® 1.0 to 6.0 and NVLink
- Clock distribution and level translation for ADCs, DACs, SATA/SAS, SONET/SDH, multi-gigabit Ethernet, and Fibre Channel line cards
- Servers, storage systems, switches, routers, and display panels
- Reference clock distribution for BBU and RRU applications

Functional Block Diagram



Note: Only the "G" (includes glitch-free switchover) version supports the synchronization function.

Ordering Information

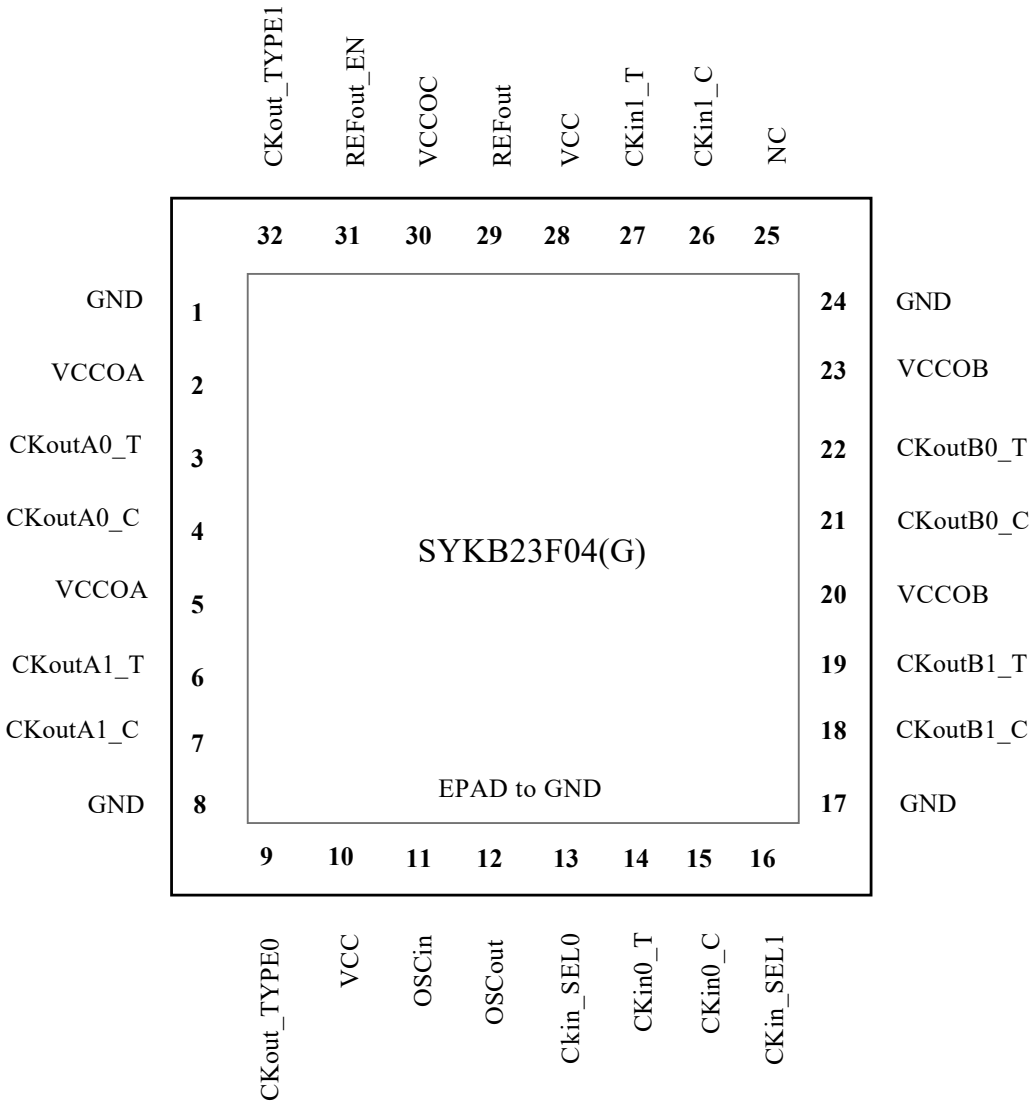
Part Number	Package	Operating Temperature
SYKB23F04	32-pin WQFN, 5.0mm x 5.0mm x 0.75mm	-40°C to +85°C

This document is a brief product specification sheet that outlines only the basic features. For detailed electrical specifications, please contact https://www.yxc.hk/ to request the complete version of the specification sheet.

1 Pin Information

1.1 Pin Assignment

Figure 3. 32-pin WQFN, 5.0mm x 5.0mm x 0.75mm (Top View)



1.2 Pin Description

Table 1. Pin Description

Pin Name	Pin No.	Type[1]	Description
Clock Inputs			
CKin0_T, CKin0_C	14, 15	I	Input reference 0, differential-pair (true & complementary) or single-ended.
CKin1_T, CKin1_C	27, 26	I	Input reference 1, differential-pair (true & complementary) or single-ended.
OSCin	11	I	Crystal in or single-ended clock in.
OSCout	12	O	Crystal out or floating if OSCin is used as single-ended clock in.
Clock Outputs			
CKoutA0_T, CKoutA0_C	3, 4	O	Bank A differential clock output 0 (true & complementary).
CKoutA1_T, CKoutA1_C	6, 7	O	Bank A differential clock output 1 (true & complementary).
CKoutB0_T, CKoutB0_C	22, 21	O	Bank B differential clock output 0 (true & complementary).
CKoutB1_T, CKoutB1_C	19, 18	O	Bank B differential clock output 1 (true & complementary).
REFout	29	O	Single-ended LVCMOS output.
Control Pins			
CKin_SEL0, CKin_SEL1	13, 16	I	Input reference selection {CKin_SEL1, CKin_SEL0}: • 2'b00 = CKin0_T & CKin0_C; • 2'b01 = CKin1_T & CKin1_C; • 2'b1x = OSCin.
CKout_TYPE0, CKout_TYPE1	9, 32	I	Output type selection {CKout_TYPE1, CKout_TYPE0}: • 2'b00 = LVPECL; • 2'b01 = LVDS; • 2'b10 = LP-HCSL; • 2'b11 = Disabled (HiZ).
REFout_EN	31	I	REFout enable input, internally synchronized with REFout.
Power & Ground			
VCC	10, 28	P	Core power supply, 1.8V-3.3V.
VCCOA	2, 5	P	Power supply for bank A clock outputs, 1.8V-3.3V.
VCCOB	20, 23	P	Power supply for bank B clock outputs, 1.8V-3.3V.
VCCOC	30	P	Power supply for bank C (REF) clock output, 1.8V-3.3V.
GND	1, 8, 17, 24	P	Ground.
GND_EP (ePad)	-	P	Exposed pad of package. Connect to ground.
No Connection			
NC	25	-	No connection. This pin must not be pulled high. It may be pulled down or left floating.

1."I," "O," and "P" in this column refer to "Input", "Output," and "Power Supply/Ground", respectively.

2 Function Description

2.1 Product Overview

Table 2 presents the key features of the clock buffer.

Table 2. Feature Summary

Input Reference Clocks			Output Clocks		
Crystal Input	Differential Clock Inputs	Single-ended Support	Differential Clock Outputs	Differential Output Type	LVCMOS Output
1(OSCin)	2(CKin[1:0]_T&C)	Yes(allinputs)	4(2banks×2)	LVPECL,LVDS,LP-HCSL	1

2.2 Chip Control

The clock buffer supports pin-based control, allowing input reference selection, output type selection, and output enable/disable functionality. The enable and disable control of the single-ended LVCMOS output is synchronized to the currently selected reference clock.

2.2.1 Input Reference Selection via Pins

The clock buffer offers three input reference sources, with one selected as the output clock reference through the two control pins, CKin_SEL1 and CKin_SEL0. The selection logic is given in Table 3.

Table 3. Reference Source Selection

{CKin_SEL1, CKin_SEL0}	Selected Input Reference Source
2'b00	CKin0_T, CKin0_C
2'b01	CKin1_T, CKin1_C
2'b10 or 2'b11	OSCin

The reference source can be dynamically switched during runtime. In the SYKB23F04 version, the pin selection logic is not synchronized with the selected input reference, which may result in undefined output levels during the switchover. In contrast, the SYKB23F04(G) version includes synchronized pin selection logic, enabling a glitch-free switchover with a gapped clock inserted.

Switchover between CKin1_T & C and CKin0_T & C can be either an asynchronous action or a glitch-free, gapped clock switching process. Support for glitch-free switchover is part-number dependent. When supported, the output will consistently buffer the entire clock signal and maintain a DC low level throughout the switchover process. Two conditions must be met to use this function:

1. Both reference sources must be active during the switching process;
2. The target source must not be of the crystal type.

When the crystal source is not selected, the internal crystal module will be turned off or reset, and it will be automatically re-enabled once the reference source is switched back to the crystal source.

2.2.2 Differential-Pair Output Control

Two pins, CKout_TYPE1 and CKout_TYPE0, allow selection of one of the three output types or set the output status to HiZ (Disable), as shown in Table 4.

Table 4. Differential Output Type Selection

{CKout_TYPE1, CKout_TYPE0}	CKoutX[1:0]_T & C1
2'b00	LVPECL
2'b01	LVDS
2'b10	LP-HCSL
2'b11	Disable (HiZ)

1. X = A or B, standing for output bank A or B.

Table 5 illustrates the logic state of the differential outputs versus the input reference state. The differential outputs can be set to DC logic 0 based on the input reference connection mode when the output type is one of the three differential output types (LVPECL, LVDS, and LP-HCSL).

Table 5. Differential-Pair Output Operation Map

{CKout_TYPE1, CKout_ TYPE0}1	{CKin_SEL1, CKin_SEL0}	State of Selected Input Reference CKinx_T & C2	State of Differential Output CKoutX[1:0]_T & C1
2'b11	Don't Care	Don't Care	HiZ
2'b002'b012'b10	2'b10 or 2'b11	Don't Care	Crystal Fanout
	2'b00 or 2'b01	Both Open	• CKoutX[1:0]_T = Logic Low • CKoutX[1:0]_C = Logic High
		Shorted together	Don't Care
		Both tied to ground	
		Both tied to VCC	
		Others	Same as input

1. X = A or B, standing for output bank A or B. 2.
x = 0 or 1.

2.2.3 Single-ended LVCMOS Output Control

The single-ended output can be set to a DC low level by configuring the input reference connection status. The operation map is provided as follows.

Table 6. Single-ended LVCMOS Output Operation Map (Sheet 1 of 2)

REFout_EN	{CKin_SEL1,CKin_SEL0}	State of Selected Input Reference CKinx_T & C1	State of Single-ended Output REFout
1'b0	Don't Care	Don't Care	HiZ

Table 6. Single-ended LVCMOS Output Operation Map (Sheet 2 of 2)

REFout_EN	{CKin_SEL1,CKin_SEL0}	State of Selected Input Reference CKinx_T & C1	State of Single-ended Output REFout
1'b1	2'b10 or 2'b11	Don't Care	Crystal Fanout
	2'b00 or 2'b01	Both Open	Logic Low
		Shorted together	Don't Care
		Both tied to ground	
		Both tied to VCC	
		Others	Same as input

1.x = 0 or 1.