SiT1588

1.2 mm^2 µPower, 5 ppm, 32.768 kHz TCXO with In-System Auto-Calibration

Features

- 32.768 kHz ±5 ppm all-inclusive frequency stability
- Maintains tight stability after overmold
- Optional in-system auto calibration:
  - Compensates for board-level stress-induced frequency errors
- World's smallest TCXO footprint: 1.2 mm^2
  - 1.5 mm x 0.8 mm CSP
- LVCMOS output drives multiple loads
- Low integrated phase jitter (IPJ) suitable for multiplying up for portable audio: 2.5 ns_{RMS}
- Ultra-low power: 4.5 µA
- Supply voltage: 1.8 V ±10%
- Operating temperature ranges: -40°C to +85°C
- Pb-free, RoHS and REACH compliant
- Hermetically sealed against gas intrusion to exceed test conditions such as MIL-STD-883G Method 1014.12

Applications

- Smart watches, health and wellness monitors
- Ultra-accurate RTC reference clock
- Smart utility meters, E-meters

TempFlat MEMS™ AstroMEMS™

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Electrical Characteristics

Table 1. Electrical Characteristics

Conditions: Min/Max limits are over temperature, Vdd = 1.8 V ±10%, unless otherwise stated. Typicals are at 25°C and Vdd = 1.8 V.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency and Stability						
Output Frequency	Fout		32.768		kHz	
Total Frequency Stability with Overmold[1]	F_stab	-5		5	ppm	All inclusive. Includes initial tolerance and stability over temperature, voltage, and load variations
Allan Deviation	AD		1e-8	4e-8	–	1 second averaging time
First Year Frequency Aging	F_aging		±1		ppm	T_A = 25°C, Vdd = 1.8 V, with overmold
Humidity Sensitivity			±0.1		ppm/%RH	Humidity effect on Frequency stability
Jitter						
Integrated Phase Jitter	IPJ		1.8	2.5	ns_{RMS}	Integration bandwidth = 100 Hz to 16.384 kHz. Inclusive of 50 mV peak-to-peak sinusoidal noise on Vdd. Noise frequency 100 Hz to 20 MHz
RMS Period Jitter	PJ_{RMS}		2.5	4	ns_{RMS}	10,000 samples, per JEDEC standard 65B
Peak-to-Peak Period Jitter	PJ_{p-p}		20	30	ns_{p-p}	
Supply Voltage and Current Consumption						
Operating Supply Voltage	Vdd	1.62	1.8	1.98	V	
Supply Current	Idd		4.5	5.3	µA	No Load
Start-up Time at Power-up	t_start			300	ms	Measured when supply reaches 90% of final Vdd to the first output pulse
Operating Temperature Range						
Operating Temperature Range	Vdd	-20		70	°C	"C" ordering code
		-40		85	°C	"I" ordering code
LVCMOS Output						
Output Rise/Fall Time	tr, tf		9	20	ns	10-90% (Vdd), 15 pF Load
Output Clock Duty Cycle	DC	45		55	%	
Output Voltage High	VOH	90%			Vdd	I_{OH} = -1 µA
Output Voltage Low	VOL			10%	Vdd	I_{OL} = 1 µA

Note:

1. Tested with Agilent 53132A frequency counter. Measured with 100 ms gate time for accurate frequency measurement.

Table 2. Pin Configuration

CSP Pin	Symbol	I/O	Functionality
1	Auto-Cal or NC	Control Input	Used for communicating calibration information to the chip for improving stability in the presence of board level induced stresses. Leave pin floating (NC) when not using the calibration function.
2	CLK Out	OUT	Oscillator clock output, LVCMOS compatible. Output driver will sink/source sufficient current to drive multiple loads without signal degradation.
3	Vdd	Power Supply	SiT1588 includes on-chip filtering capacitance. If your power supply cannot deliver fast response for the rise/fall time, we recommend a 10-100 nF bypass capacitor.
4	GND	Power Supply Ground	Connect to ground.

CSP Package (Top View)

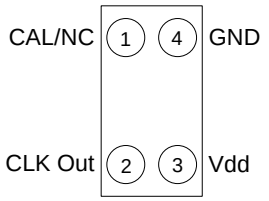


Figure 1. Pin Assignment

Table 3. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameters	Test Conditions	Value	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 4.0	V
Continuous Maximum Operating Temperature Range		105	°C
Human Body Model (HBM) ESD Protection	JESD22-A114	2000	V
Charge-Device Model (CDM) ESD Protection	JESD22-C101	750	V
Machine Model (MM) ESD Protection	JESD22-A115	200	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	Mil 883, Method 2002	20,000	*g*
Mechanical Vibration Resistance	Mil 883, Method 2007	70	*g*
Maximum Junction Temperature		150	°C
Storage Temperature		-65 to 150	°C

System Block Diagram

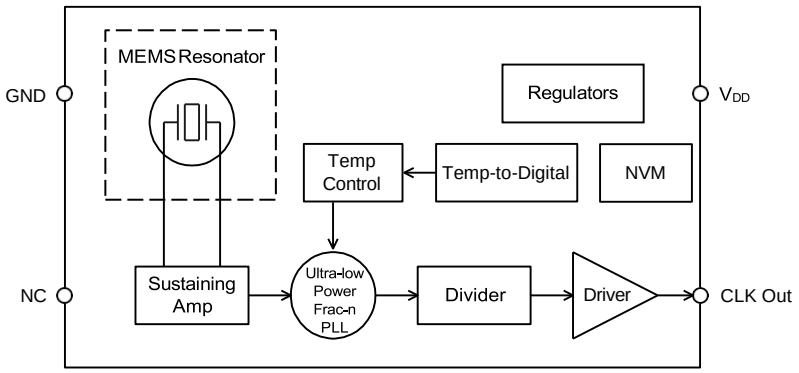


Figure 2. SiT1588 Block Diagram

Description

SiT1588 is an ultra-small, µPower 32.768 kHz TCXO optimized for battery-powered applications. SiTime's silicon MEMS technology enables the first 32 kHz TCXO in the world's smallest footprint and chip-scale packaging (CSP). Typical supply current is 4.5 µA under no load condition.

SiTime's MEMS oscillator consists of a MEMS resonator and a programmable analog circuit. SiT1588 MEMS resonator is built with SiTime's unique MEMS First™ process. A key manufacturing step is EpiSeal™ during which the MEMS resonator is annealed with temperatures over 1000°C. EpiSeal creates an extremely strong, clean, vacuum chamber that encapsulates the MEMS resonator and ensures the best performance and reliability. During EpiSeal, a poly silicon cap is grown on top of the resonator cavity, which eliminates the need for additional cap wafers or other exotic packaging. As a result, SiTime's MEMS resonator die can be used like any other semiconductor die. One unique result of SiTime's MEMS First and EpiSeal manufacturing processes is the capability to integrate SiTime's MEMS die with a SOC, ASIC, microprocessor or analog die within a package to eliminate external timing components and provide a highly integrated, smaller, cheaper solution to the customer.

TCXO Frequency Stability

SiT1588 is factory calibrated (trimmed) over multiple temperature points to guarantee extremely tight stability over temperature. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover point with a -0.04 ppm/C^2 temperature coefficient, the SiT1588 temperature coefficient is calibrated and corrected over temperature with an active temperature correction circuit. The result is a 32 kHz TCXO with extremely tight frequency variation over the -40°C to +85°C temperature range.

When measuring the output frequency of SiT1588 with a frequency counter, it is important to make sure the counter's gate time is ≥100 ms. Shorter gate times may lead to inaccurate measurements.

In-System Auto Calibration

SiT1588 provides a unique, in-system calibration feature that compensates for assembly-related frequency offsets for improved overall frequency stability. The on-chip auto-calibration function is performed one-time during the customer's production system manufacturing process. In order to initiate the one-time auto calibration process, refer to the pin 1 auto-calibration description.

After assembly, follow the calibration steps as shown in the flow chart (Figure 3). Connect pin 1 to a 10 MHz reference (GPS disciplined or equivalent) and monitor the SiT1588 CLK Out for status and error flags. A summary of these flags is shown in Table 7. SiT1588 will compare its 32.768 kHz (plus the assembly-related error) frequency to the accurate 10 MHz reference, calibrate (remove) the error and store the calibration in its internal non-volatile memory. The result is a calibrated 32.768 kHz output frequency with an overall stability (accuracy) of ±5 ppm. The entire auto-calibration process typically takes about 2 seconds.

Auto calibration is intended to be performed one time to remove the board-related offset errors. The auto-calibration procedure can be repeated if process fails during the initial steps (see Table 7). The maximum number of retries is determined by the customer.

Post Stress Frequency Stability

The SiT1588 is designed to be robust and maintain frequency accuracy after overmold or underfill or even in the presence of the smallest molecular gases that may be encountered either in manufacturing, qualification stress or general usage. In such cases, the SiT1588 is designed to withstand external influences and stay within the ±5 ppm all-inclusive frequency stability.

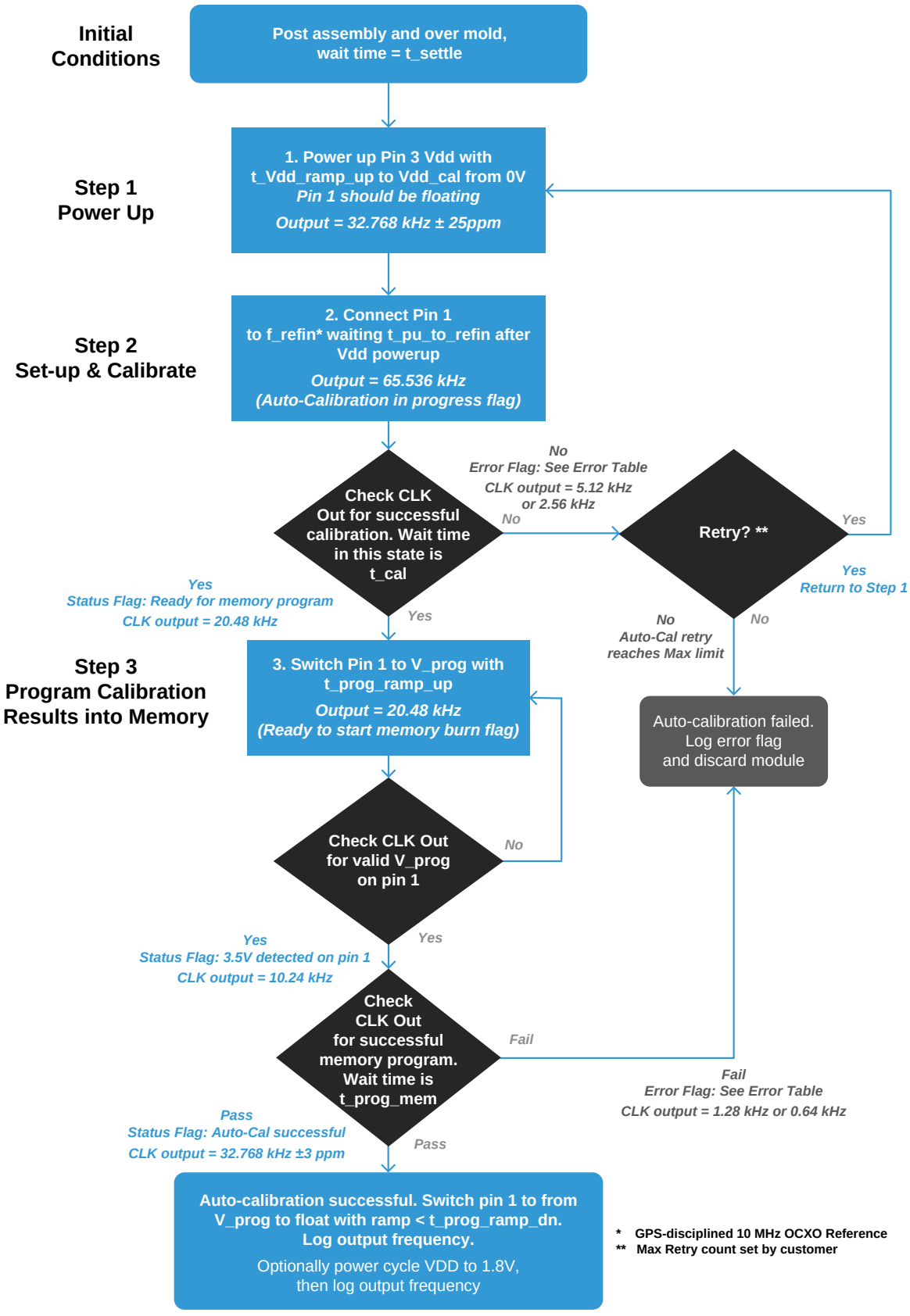


Figure 3. Initial Offset Auto-Calibration Procedure

In-System Auto-Calibration

Table 4. Pin 1 Auto-Calibration Mode DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Impedance	Z_IN	80			kΩ	Internal pull-down
Input VIH	VIH	70%			Vdd	
Input VIL	VIL			30%	Vdd	
Input Overshoot Voltage	V_IN_OD			75	mV	
Program Voltage	V_prog	3.4	3.5	3.63	V	Pin 1 NVM program voltage
Program Current	I_prog			30	mA_{pk}	Peak current required on pin 1 during auto-calibration
				5	mA_{avg}	Average current required on pin 1 during auto-calibration
Auto-Cal Voltage Noise Ripple				50	mVpp	Max noise on 3.5 V auto-calibration voltage (pin 1)
Auto-Cal Vdd Supply	Vdd_cal	1.71	1.8	1.98	V	Vdd (pin 3) supply voltage during auto-calibration
Vdd Bypass Capacitor			0.1		µF	Vdd (pin 3) bypass cap required during auto-calibration
Pin 3 Idd Prog Current	Idd_prog			1	mA	Idd (pin 3) current required during auto-calibration
Pin 3 Min Power Down Threshold Voltage	Vdd_pd			0.7	V	Pin 1 Vdd threshold to guarantee internal device power-down

Table 5. Auto-Calibration Mode Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Post System Assy Settling Time	t_settle	24			hr	Wait time between > absolute max storage temp exposure (150°C) and auto-cal start
Pin 3 Power Supply Ramp Rate	t_Vdd_ramp			100	ms	Ramp rate for Vdd pin during auto-calibration
Auto-Cal Ref-in Wait Time	t_pu_to_refin	0.5			sec	Time to supply auto-cal clock on pin 1 after within spec Vdd (pin 3)
Ref In Detection Time	t_refin_to_CLK_flag_65k			1.2	ms	Time to detect 10 MHz auto-cal reference inputs, 65.536 kHz output
Auto-Cal Time	t_cal		2	5	sec	Time in Step 2, auto-calibration
Pin 1 Float Duration	t_refin_to_float	200			µs	Pin 1 float time required prior to applying prog voltage
Pin 1 Prog Voltage Ramp Rate	t_prog_ramp_up	1		100	µs	Ramp rate on Cal pin to V_prog during auto-calibration
Prog Voltage Detection Time	t_prog_to_CLK_flag_10k			100	ms	Time to detect program voltage, 10.24 kHz output flag
Pin 1 Prog Voltage Ramp Down	t_prog_ramp_dn	1		100	µs	Time to power-down prog voltage
Memory Programming Time	t_prog_mem			100	ms	Time in Step 3, Memory program
Pin 3 Power-Down Delay	t_prog_to_pd	1			ms	Pin 3 Vdd power-down delay from Pin 1 prog voltage power down

Table 6. Auto-Calibration Reference Clock Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Auto-Cal Ref Clock Freq	f_refin	9.999999	10	10.000001	MHz	(10 MHz ±100 ppb) Correct reference frequency for auto-calibration
Auto-Cal Ref Clock Rise/Fall Time	t_refin_r/f	4		20	ns	20/80%; Rise and fall time of the auto-cal 10 MHz ref clock
Auto-Cal Ref Clock Duty Cycle	dc_refin	40		60	%	
Auto-Cal Ref Clock Period Jitter	pj_refin			200	ps_{RMS}	
Auto-Cal Ref Clock Allan Deviation	ad_refin			10	ppb	For averaging time = 1 second

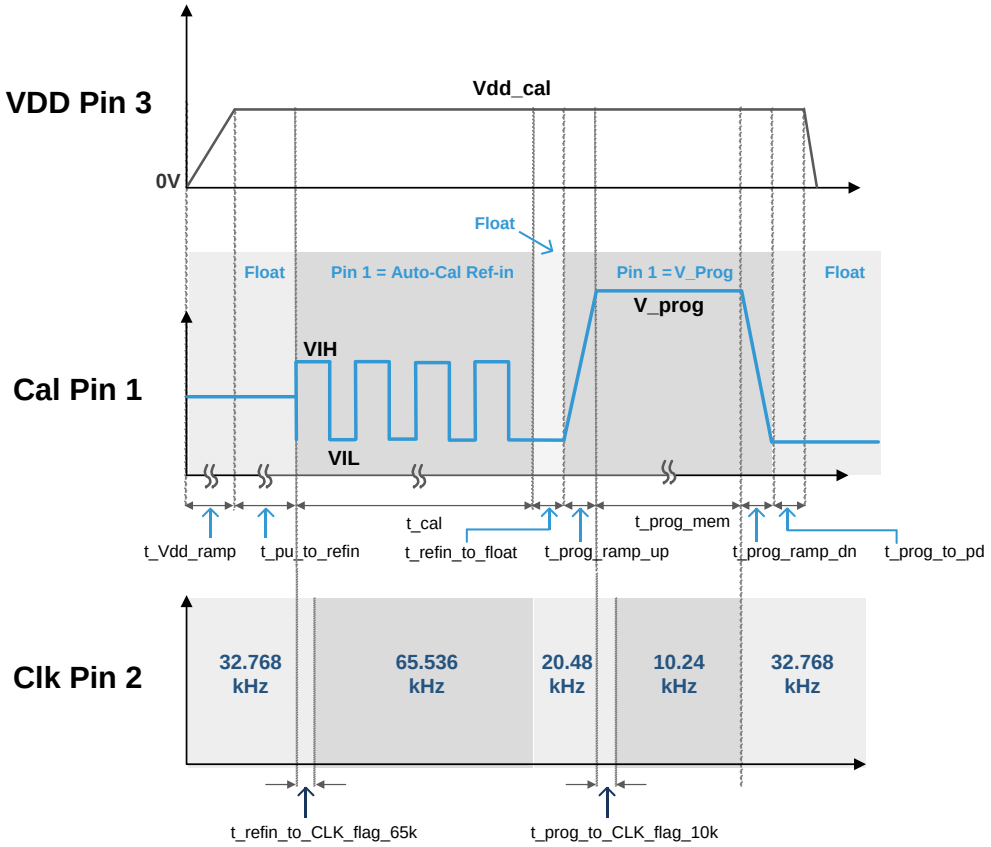


Figure 4. Auto-Calibration Timing Diagram

Table 7. Auto-Calibration Status and Error Flags

Flag Name	Output Frequency[2]	Recommended Minimum Gate Time	Status or Error Flag	Retry Calibration
Auto-Calibration in progress	65.536 kHz	10 ms	Status	N/A
Ready to start memory burn	20.48 kHz	10 ms	Status	N/A
3.3 V on Pin 1 detected	10.24 kHz	10 ms	Status	N/A
Auto-Calibration successful	32.768 kHz ±3 ppm	100 ms	Status	No
10 MHz reference lost during calibration step 3	5.12 kHz	10 ms	Error	Yes
Frequency correction out of range in step 3	2.56 kHz	10 ms	Error	Yes
Memory burn failed in step 3	1.28 kHz	10 ms	Error	No
3.3 V lost on Pin 1 during memory burn step 3	0.64 kHz	10 ms	Error	No

Note:

2. Frequency tolerance is ±5% except for 32 kHz frequency output.

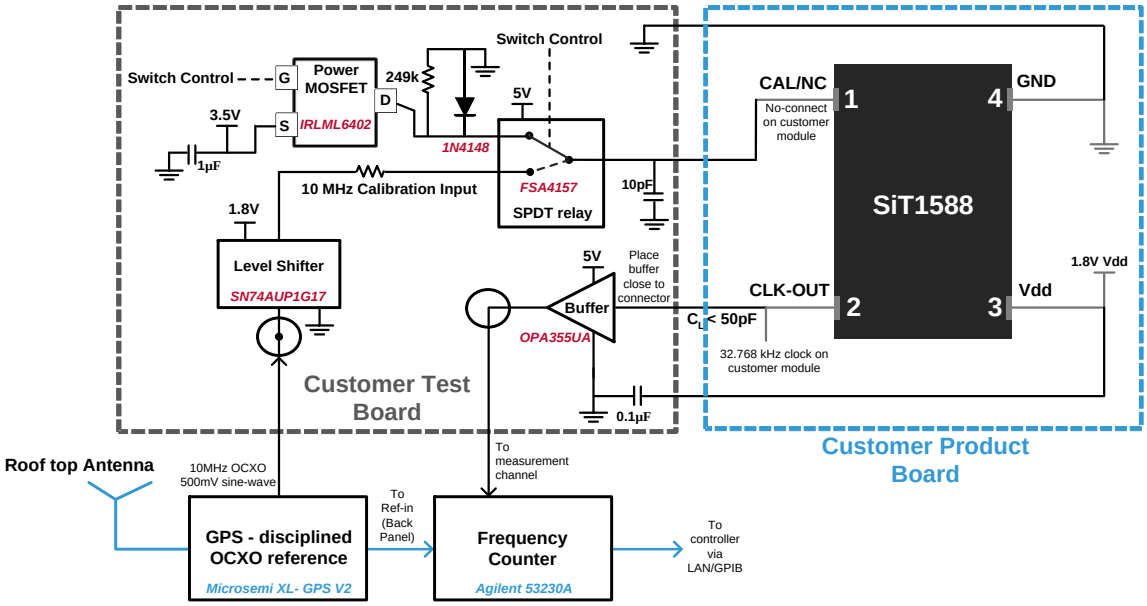
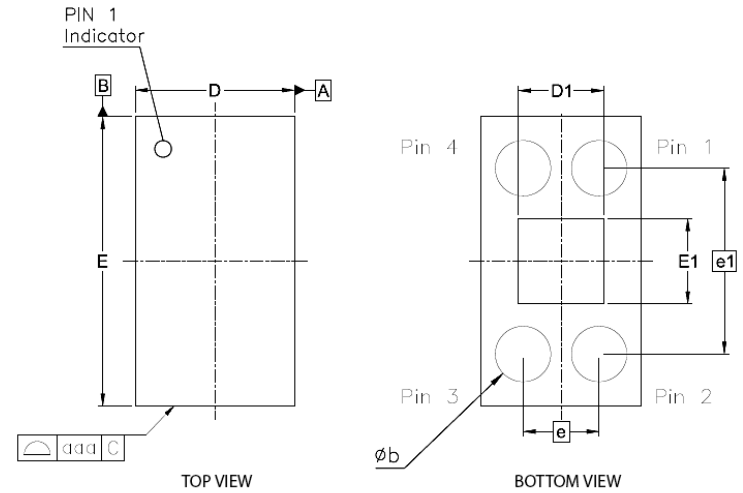
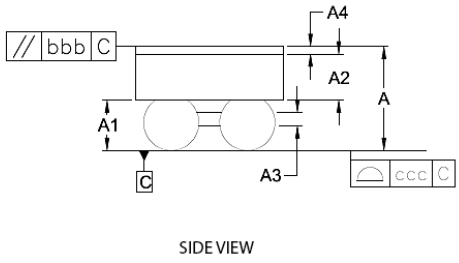


Figure 5. In-System Auto-Calibration Hardware Interface

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)



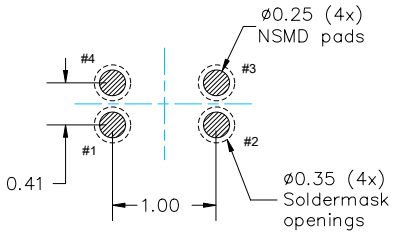


		SYMBOL	MIN	NOM	MAX
PACKAGE THICKNESS		A	0.481	0.540	0.599
STAND OFF		A1	0.220	0.250	0.280
WAFER THICKNESS		A2	0.225	0.250	0.275
		A3	0.101	0.114	0.127
FILM THICKNESS		A4	0.036	0.040	0.044
BODY SIZE	X	D		0.845	
	Y	E		1.545	
CHILD DIE SIZE	X	D1		0.460	
	Y	E1		0.492	
BALL PITCH		e		0.410 BSC	
		e1		1.000 BSC	
BALL SIZE				0.300	
BALL DIAMETER/WIDTH		b	0.285	0.315	0.345
PACKAGE TOLERANCE		aaa		0.030	
WAFER FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.030	

NOTES
1. Dimensioning and tolerance conform to ASME Y14.5-2009
2. All dimensions are in millimeters.

TITLE	4L NCSP	SiTime	
		DWG NO.	
		POD-032-NCSP-004-C01508	
0.845x1.545x0.54 mm		REV.	SHEET
DATE	10-MAR-2019	B03	1 OF 2

Recommended Land Pattern (Unit: mm)



(soldermask openings shown with dashed line around NSMD pad)

Recommended 4-mil (0.1mm) stencil thickness

Manufacturing Guidelines

1) No Ultrasonic or Megasonic cleaning: Do not subject the SiT1588 to an ultrasonic or megasonic cleaning environment. Permanent damage or long term reliability issues may occur.
2) Applying board-level underfill and overmold is acceptable and will not impact the reliability of the device. Any post assembly frequency shift can be calibrated with the in-system auto-calibration feature.
3) Reflow profile, per JESD22-A113D.
4) The SiT1588 CSP includes a protective, opaque polymer top-coat. If the SiT1588 is exposed to intense light, especially in the 1.0-1.2 µm IR spectrum, we recommend a protective “glob-top” epoxy or other cover to keep the light from negatively impacting the frequency stability.
5) For additional manufacturing guidelines and marking/tape-reel instructions, refer to SiTime Manufacturing Notes.

Ordering Information

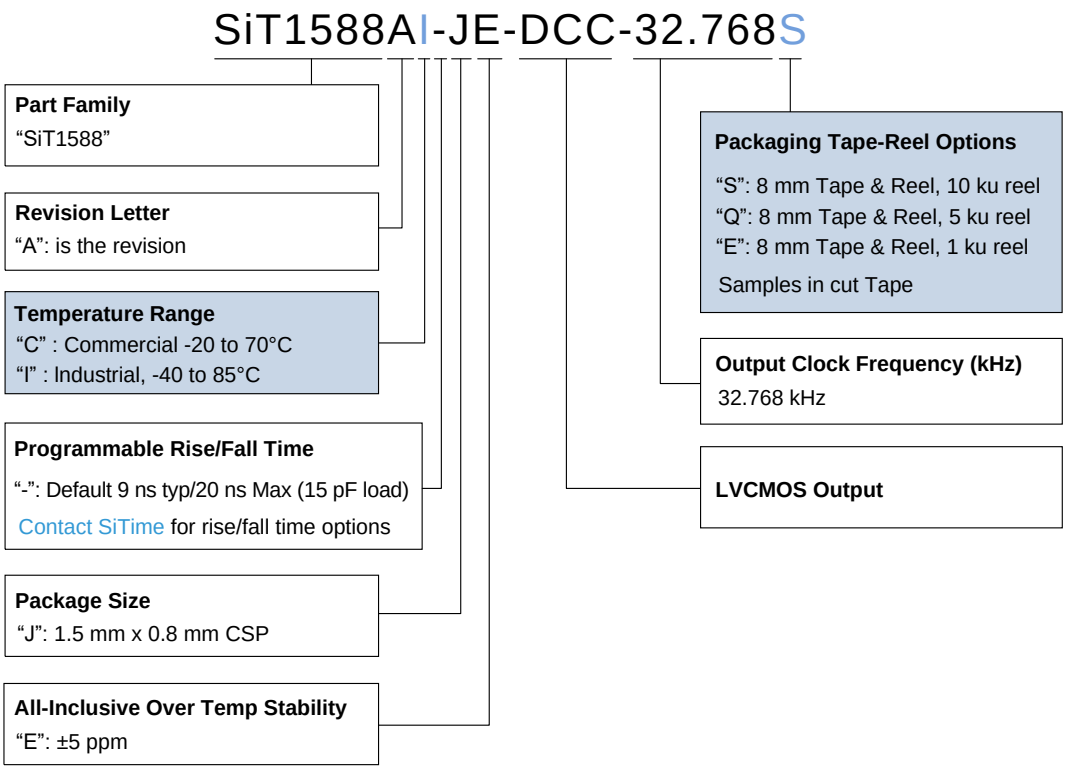


Table 8. Revision History

Version	Release Date	Change Summary
0.9	07/24/2018	Preliminary Datasheet Release
1.0	05/01/2020	Final Release
1.01	06/18/2020	Added System Block Diagram, Deprecated Initial Tolerance Specification

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