Features

- Transient Protection for Gigabit Ethernet Lines-to-Lines.
- Provide transient protection for the protected lines to
  IEC 61000-4-2 (ESD) ±30kV (air/contact)
  IEC 61000-4-4 (EFT) 80A (5/50ns)
  IEC 61000-4-5 (Lightning) 45A (8/20μs)
  Cable Discharge Event (CDE)
- DFN3020P10E (3.0x2.0mm) package.
- Specific pin out for easy board layout.
- Fast turn-on and low clamping voltage.
- Low capacitance for high speed interfaces.
- Low operating voltage: 2.5V.
- Low leakage current
- Solid-state silicon-avalanche and active circuit triggering technology.
- ***Green Part***

Applications

- WAN/LAN Device
- 10/100/1000 Ethernet
- Switching Systems
- Computers
- Instruments

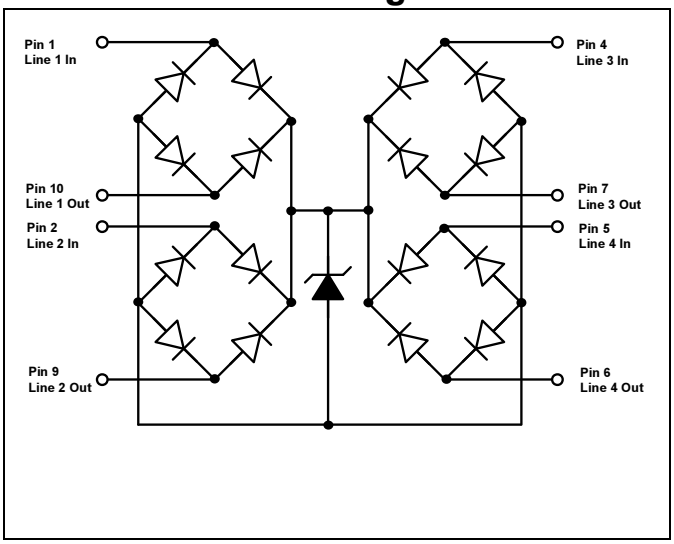
Description

AZ3125-08F is a design which includes surge rated diode arrays to protect high speed data interfaces in an electronic system. The AZ3125-08F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

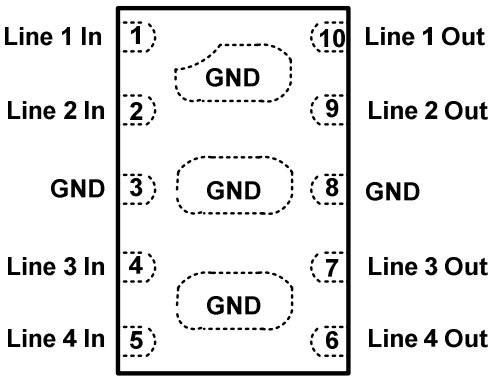
AZ3125-08F is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the proprietary clamping cells prevent over-voltage on the signal lines, protecting any downstream components.

AZ3125-08F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



DFN3020P10E (3.0x2.0mm) (Top View)

SPECIFICATIONS

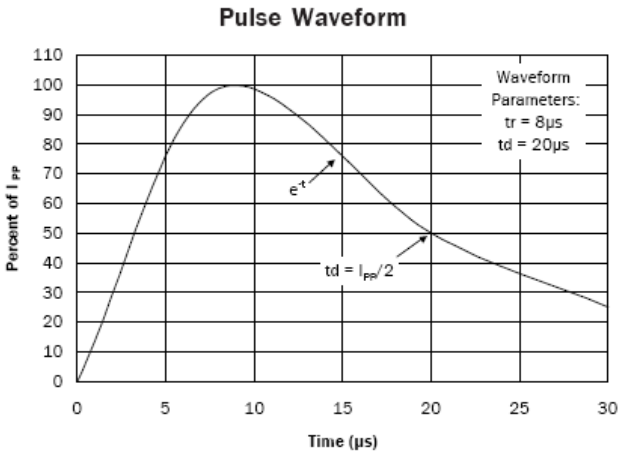
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20μs) (Note 1)	I_{PP}	45	A
ESD per IEC 61000-4-2 (Air/Contact)	V_{ESD}	±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C

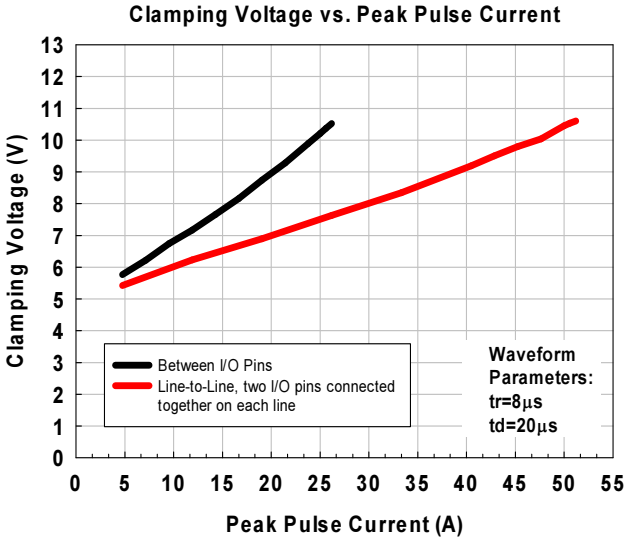
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Between I/O Pins, T=25 °C.			2.5	V
Channel Leakage Current	I_{Leak}	V_{RWM} = 2.5V, T=25 °C, Between I/O Pins.			1	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, Between I/O Pins.	3		7	V
Surge Clamping Voltage	$V_{CL-surge}$	I_{PP}=5A, tp=8/20μs, T=25 °C. Between I/O Pins.			6.5	V
		I_{PP}=10A, tp=8/20μs, T=25 °C. Between I/O Pins.			7.5	V
		I_{PP}=25A, tp=8/20μs, T=25 °C. Between I/O Pins.			11.5	V
		I_{PP}=45A, tp=8/20μs, T=25 °C. Line-to-Line, two I/O pins connected together on each line (Note 1).			11	V
ESD Clamping Voltage (Note 2)	V_{clamp}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), T=25 °C, Contact mode, Between I/O Pins.		8		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2 0~+8kV, T=25 °C, Contact mode, Between I/O Pins.		0.12		Ω
Channel Input Capacitance	C_{IN}	V_R = 1.25V, f = 1MHz, T=25 °C. Between I/O Pins		1.7	2.5	pF

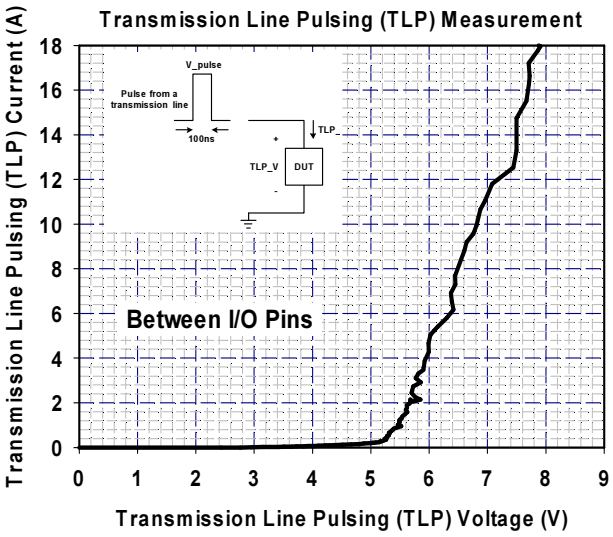
Note 1: Ratings with 2 pins connected together per the recommended configuration (i.e. pin-1 connected to pin-10, pin-2 connected to pin-9, pin-4 connected to pin-7, and pin-5 connected to pin-6).

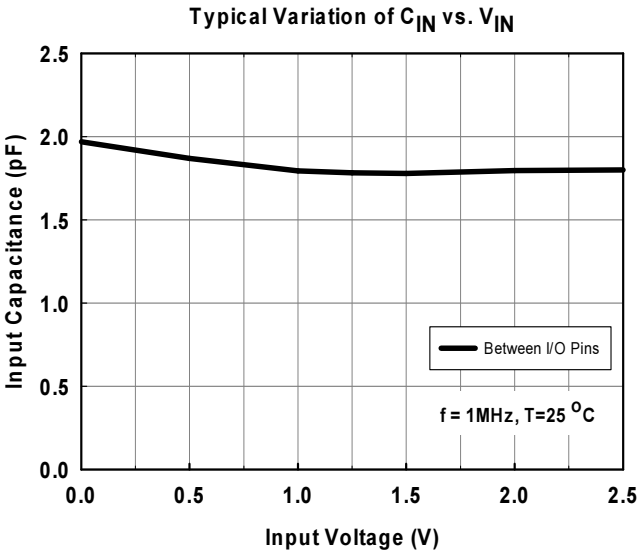
Note 2: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics









Applications Information

The AZ3125-08F is designed to protect four high speed data lines operating at 2.5 volts to against system ESD/EFT/Lightning pulses by clamping them to an acceptable reference.

The AZ3125-08F designed with a flow through pin configuration is shown in Fig. 1. Fig. 2 shows a typical PCB layout example with AZ3125-08F for ESD/EFT/Lightning protection. In the Gigabit Ethernet application, pins 1, 2, 4, and 5 should be connected to pins 10, 9, 7, and 6 respectively. The traces should be unbroken and run under the device as shown. To get minimum parasitic inductance, the path length should keep as short as possible. Pins 3, 8 and the three center tabs are electrically connected, which should be left floating (i.e. not connected to ground) in the Ethernet application. Fig. 3 shows a typical Gigabit Ethernet protection circuit with AZ3125-08F.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ3125-08F.
- Place the AZ3125-08F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path should be kept as short as possible.
- NEVER route critical signals near board edges and near the lines which the ESD transience easily injects to.

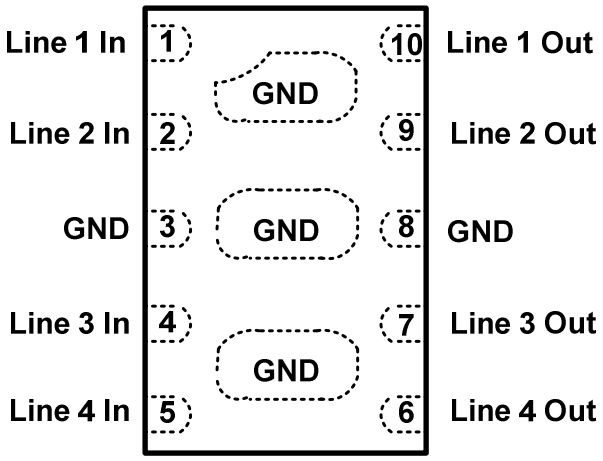


Fig. 1 Pin configuration of AZ3125-08F.

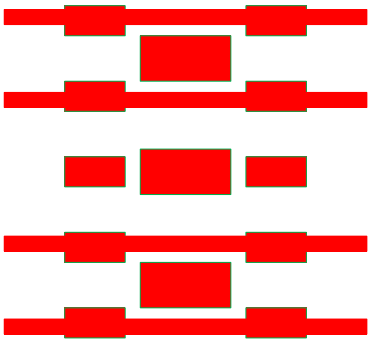


Fig. 2 Layout example of AZ3125-08F.

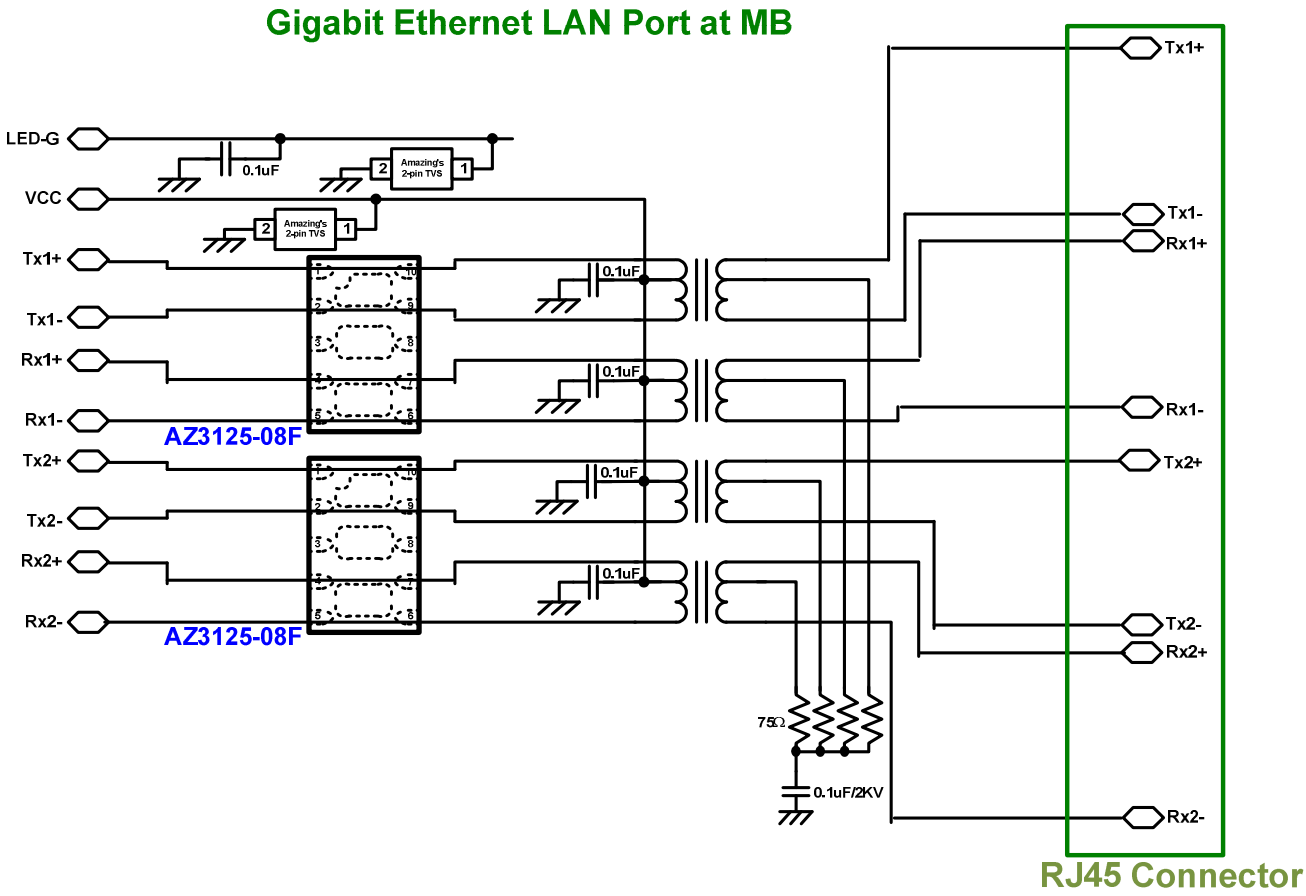
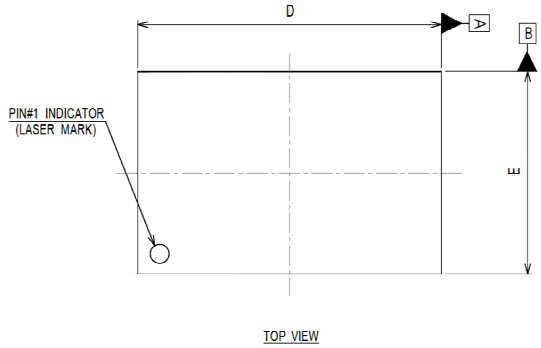


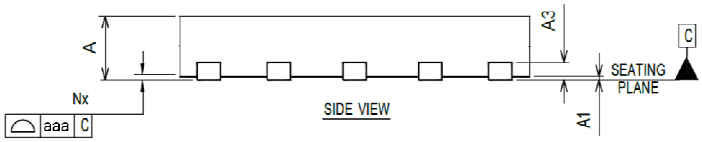
Fig. 3
Gigabit Ethernet surge protection circuit with AZ3125-08F.

Mechanical Details

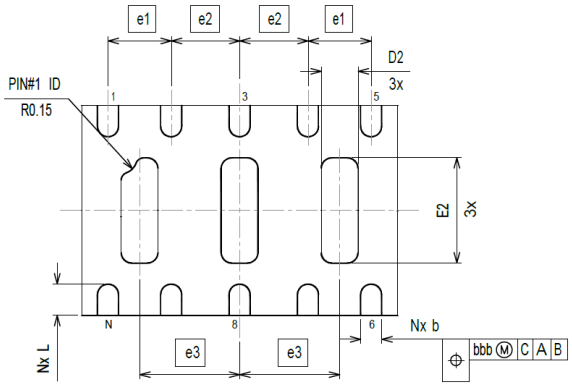
DFN3020P10E (3.0x2.0mm)
PACKAGE DIAGRAMS



TOP VIEW



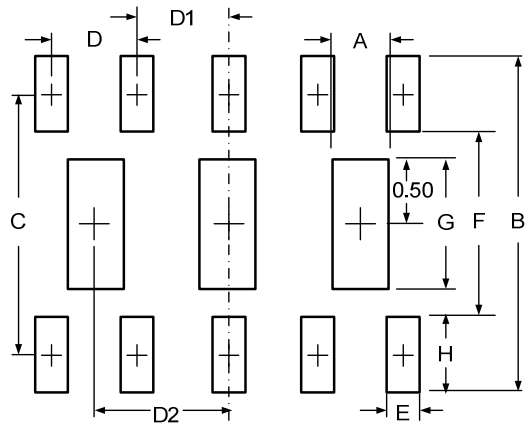
SIDE VIEW



BOTTOM VIEW

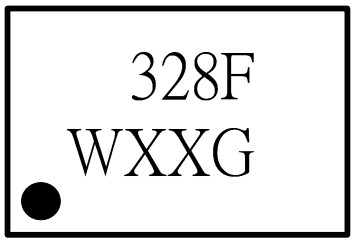
Symbol	Millimeters		
	min	nom	max
A	0.51	0.55	0.60
A1	0.00	0.02	0.05
A3		0.153REF	
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	1.90	2.00	2.10
e1		0.60BSC	
e2		0.65BSC	
e3		0.95BSC	
D2	0.25	0.35	0.45
E2	0.95	1.00	1.05
L	0.25	0.30	0.35
aaa		0.08	
bbb		0.10	

Land Layout



DIMENSIONS	
DIM	MILLIMETERS
A	0.40
B	2.56
C	1.98
D	0.60
D1	0.65
D2	0.95
E	0.25
F	1.40
G	1.00
H	0.58

MARKING CODE



328F = Device Code
W = Date Code
XX = Control Code
G = Green Part Indication

Part Number	Marking Code
AZ3125-08F.R7G (Green Part)	328F WXXG

Note : Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ3125-08F.R7G	Green	T/R	7 inch	3,000/reel	4 reels=12,000/box	6 boxes=72,000/carton

Revision History

Revision	Modification Description
Revision 2016/04/18	Preliminary Release
Revision 2017/05/11	Formal Release