Features

- ESD/Surge protection for one automotive LIN bus line
- Provide transient protection for one line to
  IEC 61000-4-2 (ESD) ±30kV (air), ±30kV (contact)
  IEC 61000-4-5 (Lightning) 8A (8/20μs)
  Cable Discharge Event (CDE)
- Provide ISO 7637-3
  Pulse 3a: -600V
  Pulse 3b: +600V
- Fast turn-on and low clamping voltage
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***
- ***AEC-Q101 qualified***

Applications

- Automotive application
- LIN bus application
- Power management system
- Industrial control
- Portable instrumentation
- Peripherals

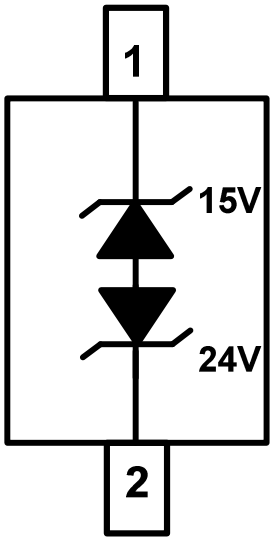
Description

AZ9824-01L is a design which includes one bi-directional ESD rated clamping cell to protect one power line, or one control line, or one low-speed data line in an electronic system. The AZ9824-01L has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Lightning, and Cable Discharge Event (CDE).

AZ9824-01L is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ9824-01L may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram / Pin Configuration



SOD323-2L (Top View)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**RATING**	**UNIT**
Peak Pulse Current (tp=8/20μs)	I_{PP}	8	A
Operating Voltage	V_{DC1} (15V)	16	V
	V_{DC2} (24V)	25	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD-1} V_{ESD-2}	±30 ±30	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +125	°C
Storage Temperature	T_{STO}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNIT**
Reverse Stand-Off Voltage	V_{RWM1} (15V)	Pin-1 to pin-2, T=25°C			15	V
	V_{RWM2} (24V)	Pin-2 to pin-1, T=25°C			24	V
Reverse Leakage Current	I_{Leak}	V_{RWM1} = +15V, T=25°C			100	nA
		V_{RWM2} = +24V, T=25°C			100	nA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, pin-1 to pin-2, T=25°C	17	19	21	V
		I_{BV} = 1mA, pin-2 to pin-1, T=25°C	25.5	28	31	V
ESD Clamping Voltage (Note 1)	V_{CL-ESD}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), contact mode, pin-1 to pin-2, T=25°C		21		V
		IEC 61000-4-2 +8kV (I_{TLP} = 16A), contact mode, pin-2 to pin-1, T=25°C		31		V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0~+8kV, contact mode, T=25°C		0.2		Ω

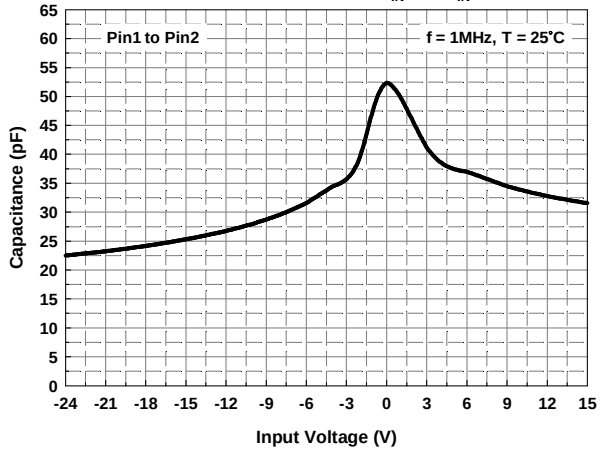
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNIT**
Surge Clamping Voltage	$V_{CL-surge}$	I_{PP} = 5A, tp = 8/20μs, pin-1 to pin-2, T=25°C		20		V
		I_{PP} = 8A, tp = 8/20μs, pin-1 to pin-2, T=25°C		21		V
		I_{PP} = 5A, tp = 8/20μs, pin-2 to pin-1, T=25°C		29		V
		I_{PP} = 8A, tp = 8/20μs, pin-2 to pin-1, T=25°C		31		V
Channel Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1MHz, T=25°C		55	65	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

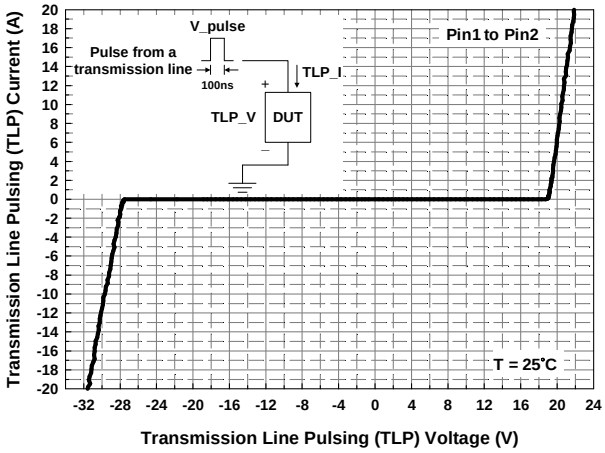
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

Typical Characteristics

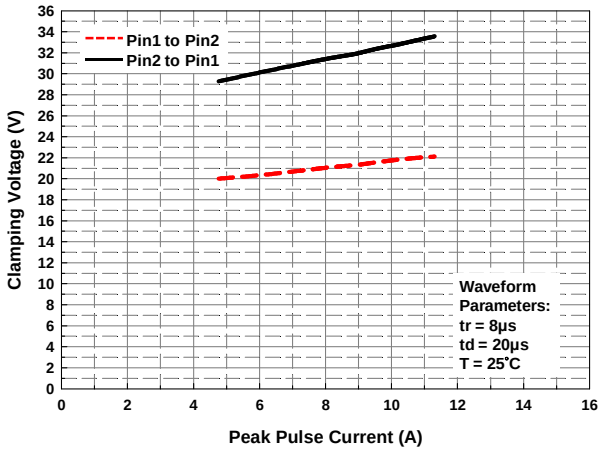
Typical Variation of C_{IN} vs. V_{IN}



Transmission Line Pulsing (TLP) Measurement



Clamping Voltage vs. Peak Pulse Current



Application Information

The AZ9824-01L is designed to protect one automotive LIN bus line against system ESD/Lightning pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ9824-01L for LIN bus protection is shown in Fig. 1. The protected line is connected at pin 2. The pin 1 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ9824-01L should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, a good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ9824-01L.
- Place the AZ9824-01L near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

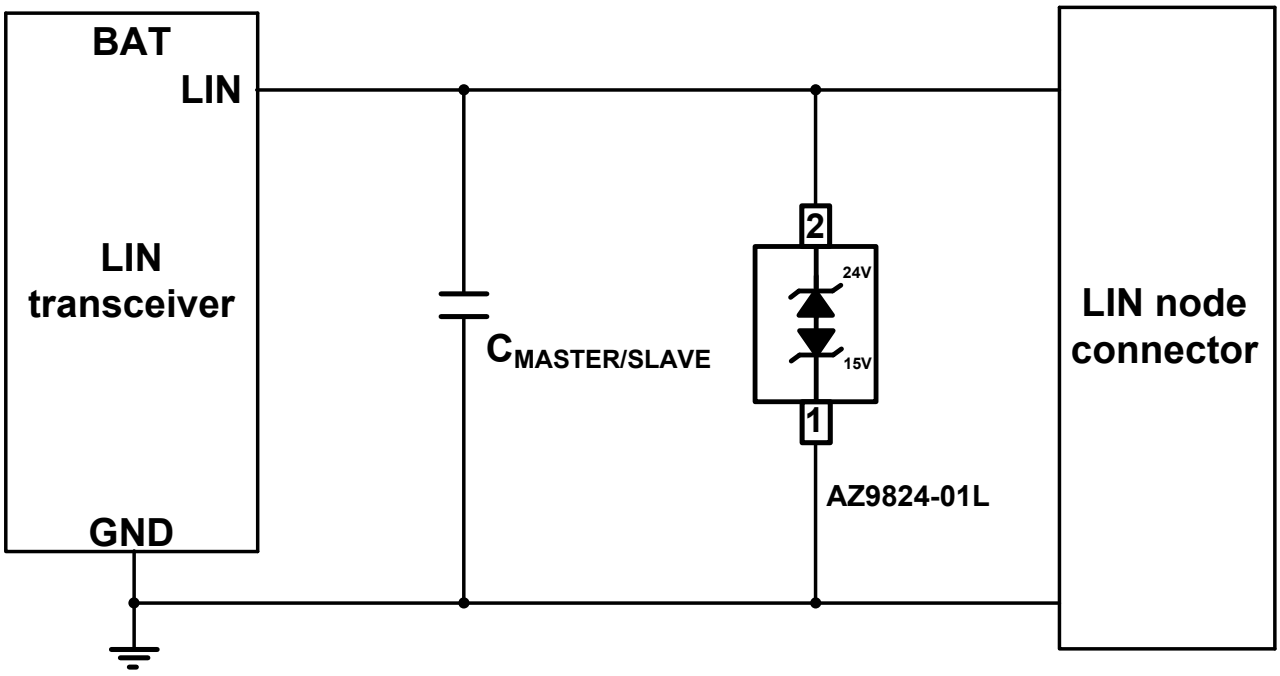
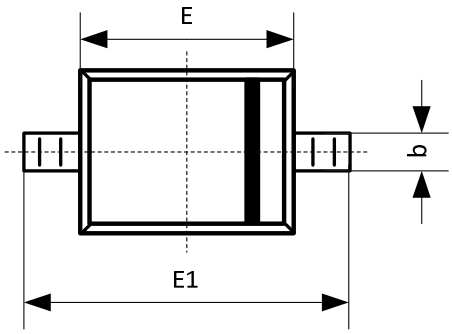


Fig. 1

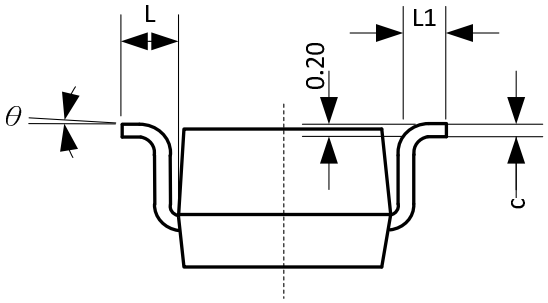
Mechanical Details

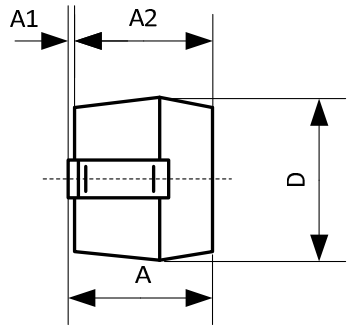
SOD323-2L
PACKAGE DIAGRAMS

TOP VIEW



SIDE VIEW

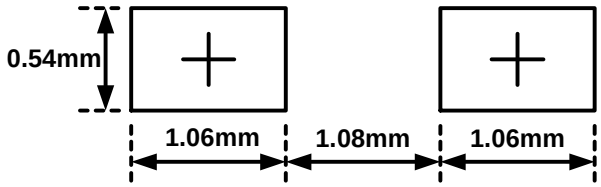




PACKAGE DIMENSIONS

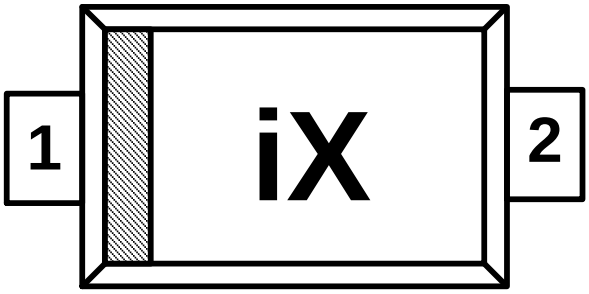
SYMBOL	MILLIMETERS	
	MIN.	MAX.
A	0.80	1.00
A1	0.00	0.10
A2	0.80	0.90
b	0.25	0.35
c	0.08	0.15
D	1.20	1.40
E	1.60	1.80
E1	2.50	2.70
L	0.475 REF	
L1	0.25	0.40
θ	0	8

LAND LAYOUT



Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Part Number	Marking Code
AZ9824-01L.R7G (Green Part)	iX

Note. Green means Pb-free, RoHS, and Halogen free compliant.

i = Device Code
X = Date Code

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ9824-01L.R7G	Green	T/R	7 inch	3,000/reel	4 reels=12,000/box	6 boxes=72,000/carton

Revision History

Revision	Modification Description
Revision 2018/11/07	Preliminary Release.
Revision 2019/08/06	Formal Release.