Proximity Sensor With Interrupt, IRED, and I²C Interface



LINKS TO ADDITIONAL RESOURCES

Design Tools | Related Documents | 3D Models

DESCRIPTION

VCNL36821S integrates a proximity sensor (PS), and a IRED into one small package. It incorporates photodiodes, amplifiers, and analog to digital converting circuits into a single chip by CMOS process. PS programmable interrupt features of individual high and low thresholds offer the best utilization of resource and power saving on the microcontroller.

APPLICATIONS

- Handheld device
- Consumer device
- Industrial application
- Earphone

FEATURES

- Package type: surface-mount
- Dimensions (L x W x H in mm): 2.55 x 2.05 x 1.0
- Integrated modules: infrared emitter (IRED), proximity sensor (PS), and signal conditioning IC
- Interrupt function
- Smallest light hole opening design
- Immunity to red glow issue (940 nm)
- Supply voltage range V_{DD}: 1.7 V to 3.6 V
- Low power consumption I²C (SMBus compatible interface)
- Floor life: 168 h, MSL 3, according to J-STD-020
- Output type: I²C bus (PS)
- Temperature compensation: -40 °C to +85 °C
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
e4
RoHS COMPLIANT
HALOGEN FREE
GREEN (5-2008)

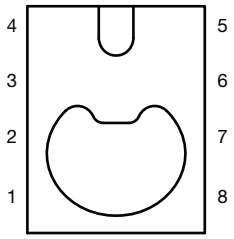
PROXIMITY FUNCTION

- Immunity to red glow (940 nm IR LED)
- Programmable IR LED sink current
- Intelligent cancellation to reduce cross talk phenomenon
- Smart persistence scheme to reduce PS response time
- Low power consumption mode

INTERRUPT

- Programmable interrupt function for PS with upper and lower thresholds
- Adjustable persistence to prevent false triggers for PS

PIN DEFINITION



1	GND	5	LED_A
2	INT	6	V_{DD}
3	NC	7	SDA
4	LED_C	8	SCL

PRODUCT SUMMARY

PART NUMBER	OPERATING RANGE (mm)	OPERATING VOLTAGE RANGE (V)	I²C BUS VOLTAGE RANGE (V)	IRED DRIVING CURRENT (mA)	OUTPUT CODE	ADC RESOLUTION PROXIMITY / AMBIENT LIGHT
VCNL36821S	300	1.7 to 3.6	1.7 to 3.6	156	12 bit, I²C	12 bit / -

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ORDERING INFORMATION			
ORDERING CODE	**PACKAGING**	**VOLUME (1)**	**REMARKS**
VCNL36821S	Tape and reel	MOQ: 3000 pcs, 3000 pcs/reel	2.55 mm x 2.05 mm x 1.0 mm

Note

(1) MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)					
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**MAX.**	**UNIT**
Supply voltage		V_{DD}	1.7	3.6	V
Operation temperature range		T_{amb}	-40	+85	°C
Storage temperature range		T_{stg}	-40	+100	°C

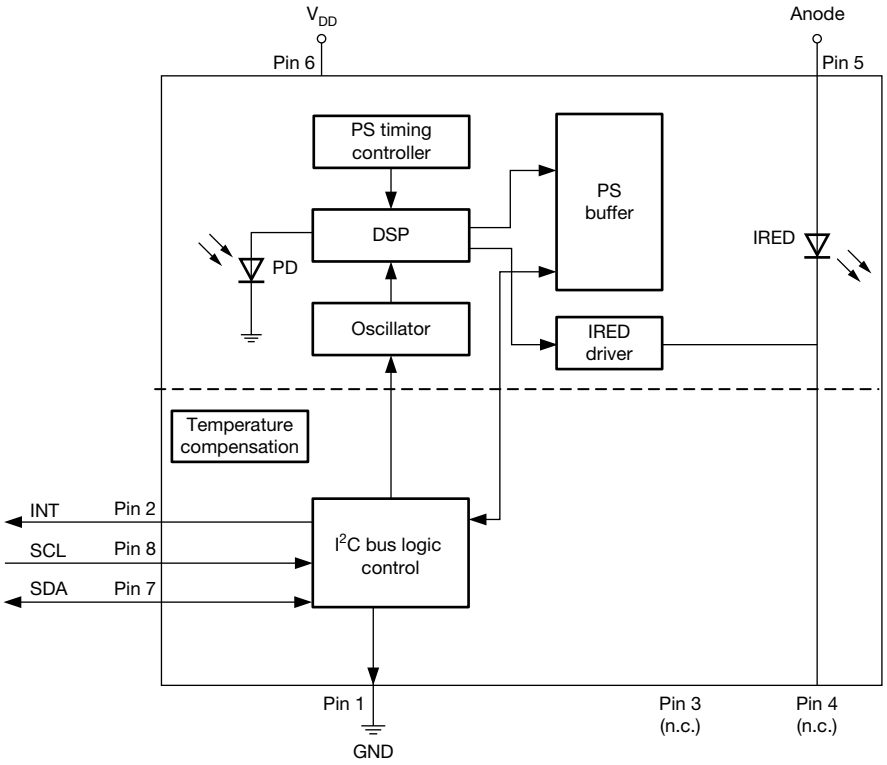
BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Sensor supply voltage		V_{DD}	1.7	-	3.6	V
IR LED supply voltage		V_{DD}	2.5	-	3.6	V
Supply current	Excluding LED driving	I_{DD}	100	200	300	µA
Shutdown current	Light condition = dark; V_{DD} = 1.8 V, T_{amb} = 25 °C	I_{DD} (SD)	-	1	-	µA
I^2C supply voltage		$V_{PULL\ UP}$	1.65	-	-	V
I^2C signal input, logic high	V_{DD} = 3.3 V	V_{IH}	1.26	-	-	V
I^2C signal input, logic low	V_{DD} = 3.3 V	V_{IL}	-	-	0.73	V
Peak wavelength of IRED	I_F = 50 mA	λ_{pLED}	-	940	-	nm
IRED driving current			-	-	156	mA

PIN DESCRIPTIONS			
PIN ASSIGNMENT	**SYMBOL**	**TYPE**	**FUNCTION**
1	GND	-	Ground
2	INT	O (open drain)	Interrupt pin
3	NC	-	Connected to GND or floating
4	LED_Cathode	I	Cathode (LED) connection
5	LED_Anode	I	Anode of LED
6	V_{DD}	-	Power supply input
7	SDA	I / O (open drain)	I^2C digital bus data input / output
8	SCL	I (open drain)	I^2C digital bus clock input

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BLOCK DIAGRAM



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I²C BUS TIMING CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**SYMBOL**	**STANDARD MODE**		**FAST MODE**		**UNIT**
		MIN.	**MAX.**	**MIN.**	**MAX.**	
Clock frequency	$f_{(SMBCLK)}$	10	100	10	400	kHz
Bus free time between start and stop condition	$t_{(BUF)}$	4.7	-	1.3	-	µs
Hold time after (repeated) start condition; after this period, the first clock is generated	$t_{(HDSTA)}$	4.0	-	0.6	-	µs
Repeated start condition setup time	$t_{(SUSTA)}$	4.7	-	0.6	-	µs
Stop condition setup time	$t_{(SUSTO)}$	4.0	-	0.6	-	µs
Data hold time	$t_{(HDDAT)}$	0	3450	0	900	ns
Data setup time	$t_{(SUDAT)}$	250	-	100	-	ns
I²C clock (SCK) low period	$t_{(LOW)}$	4.7	-	1.3	-	µs
I²C clock (SCK) high period	$t_{(HIGH)}$	4.0	-	0.6	-	µs
Clock / data fall time	$t_{(f)}$	-	300	-	300	ns
Clock / data rise time	$t_{(r)}$	-	1000	-	300	ns

Note

- Data based on standard I²C protocol requirement, not tested in production

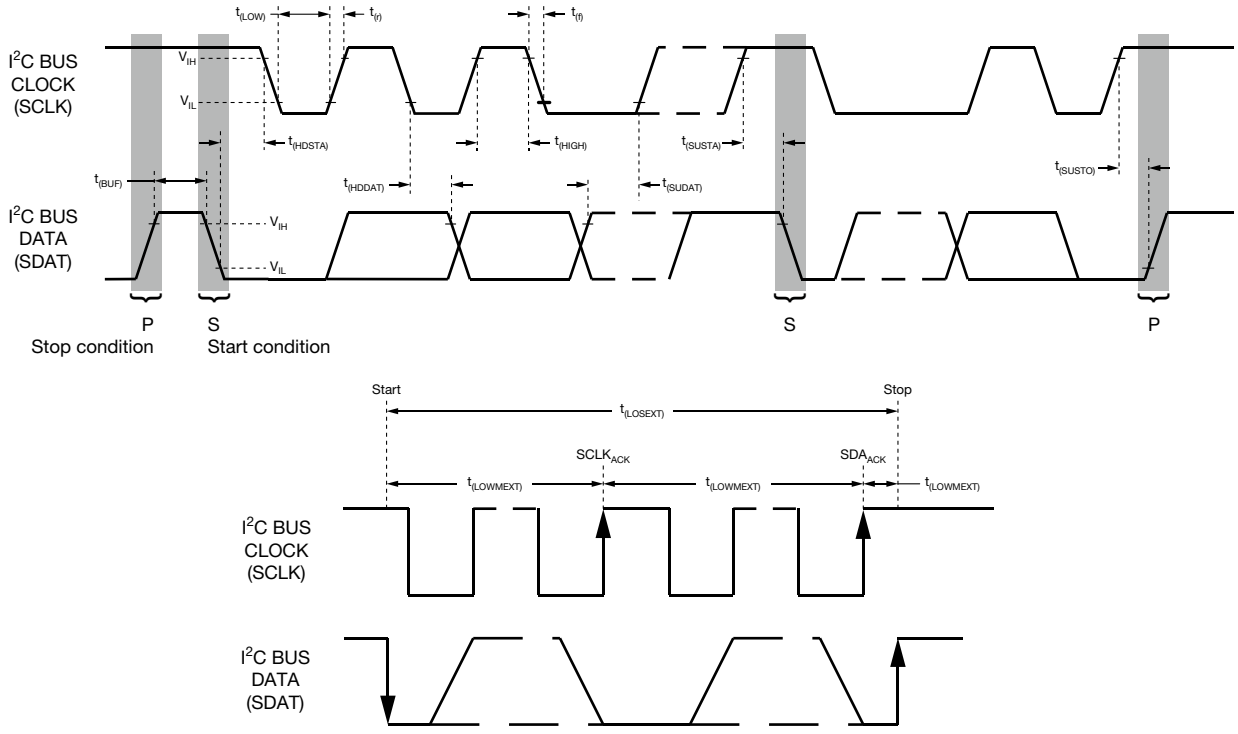


Fig. 1 - I²C Bus Timing Diagram

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PARAMETER TIMING INFORMATION

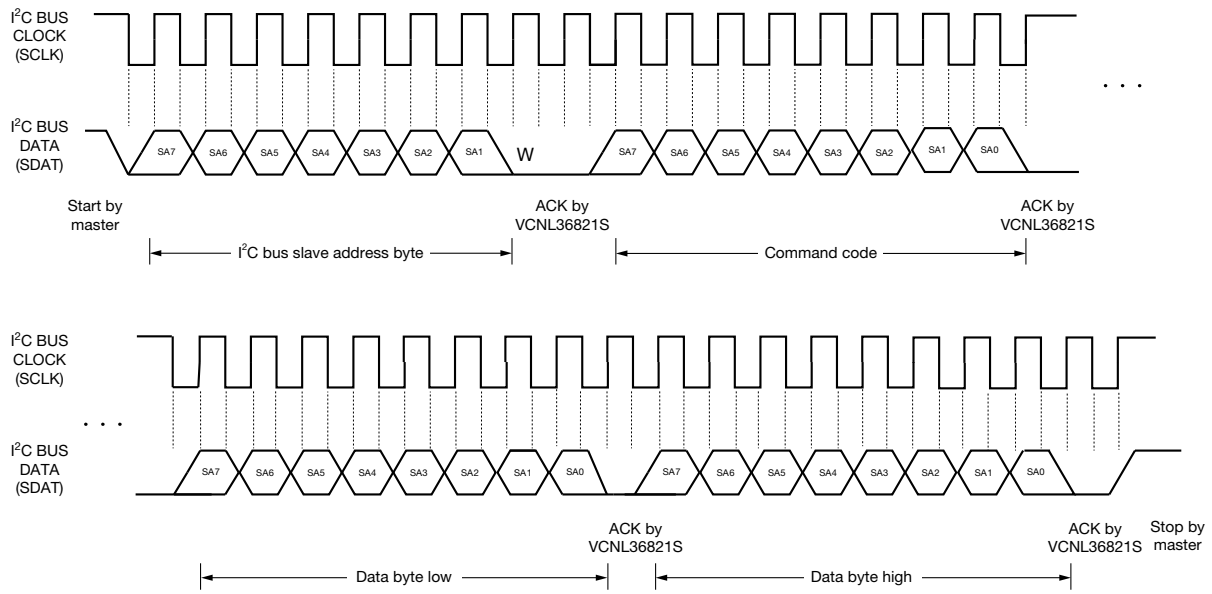


Fig. 2 - I²C Bus Timing for Sending Word Command Format

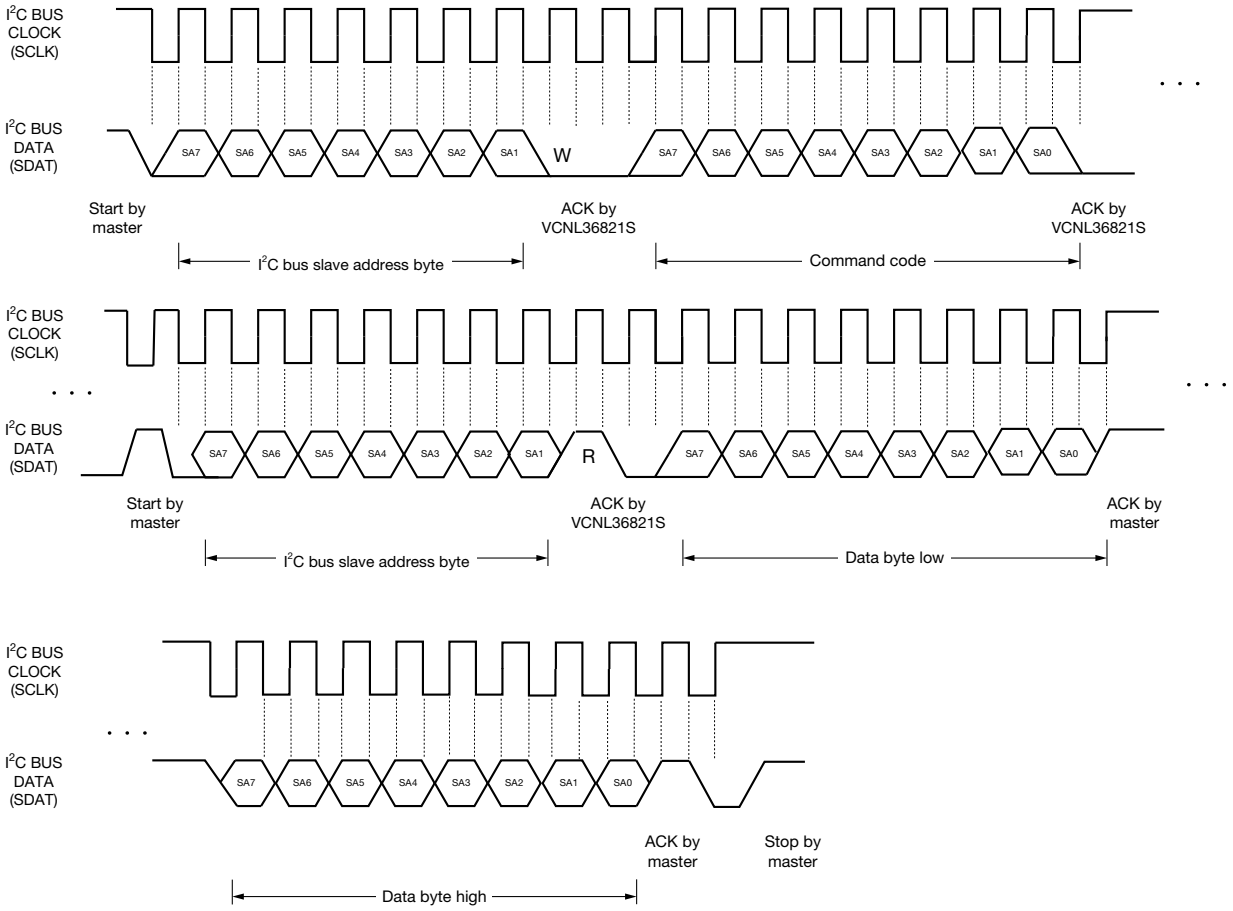


Fig. 3 - I²C Bus Timing for Receiving Word Command Format

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TYPICAL PERFORMANCE CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

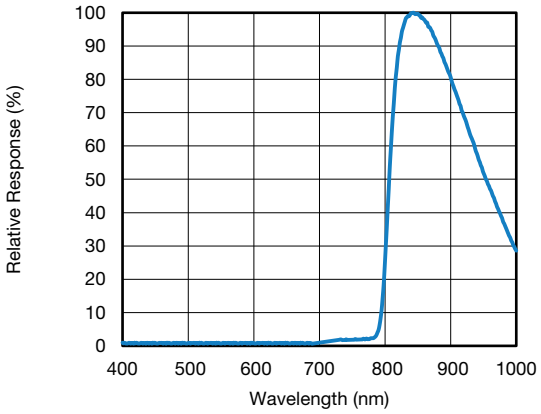


Fig. 4 - PS Sensor Spectral Response

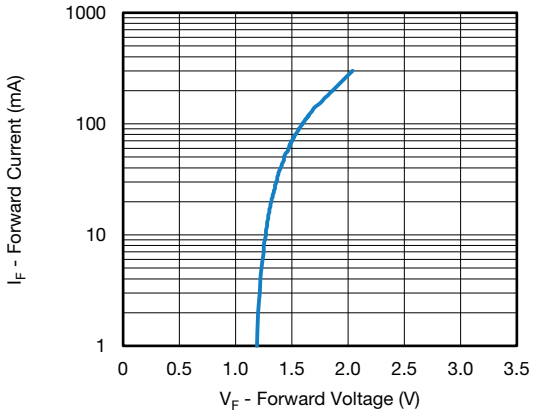


Fig. 6 - Forward Current vs. Forward Voltage

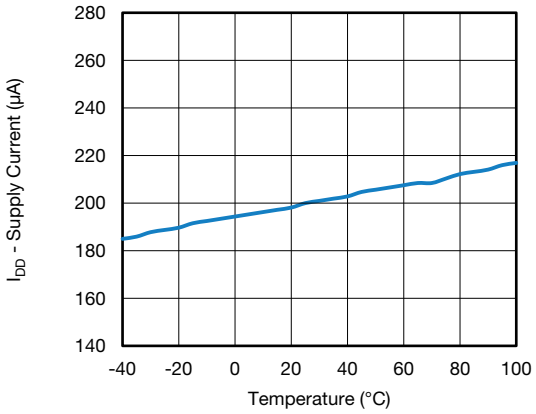


Fig. 5 - I_{DD} vs. Temperature

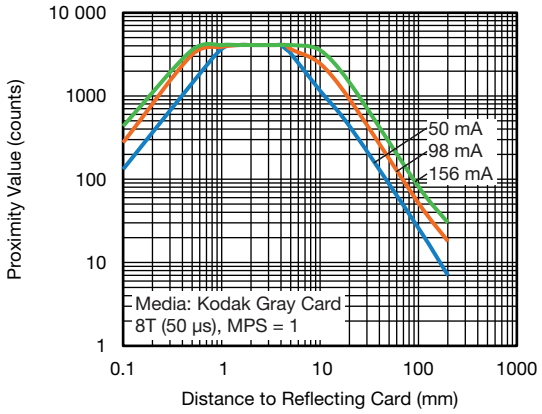


Fig. 7 - Proximity Value vs. Distance; PS_IT = 8T

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APPLICATION INFORMATION

Pin Connection with the Host

VCNL36821S integrates proximity sensor, and IRED all together with I²C interface. It is very easy for the baseband (CPU) to access PS output data via I²C interface without extra software algorithms. The hardware schematic is shown in the following diagram.

Two additional capacitors in the circuit can be used for the following purposes: (1) one 1 µF capacitor near the V_{DD} pin is used for power supply noise rejection, a second one, close to the anode pin, is used to prevent the IRED voltage from instantly dropping when the IRED is turned on and (2) 2.2 kΩ is suitable for the pull high resistor of I²C except 10 kΩ applied on INT pin.

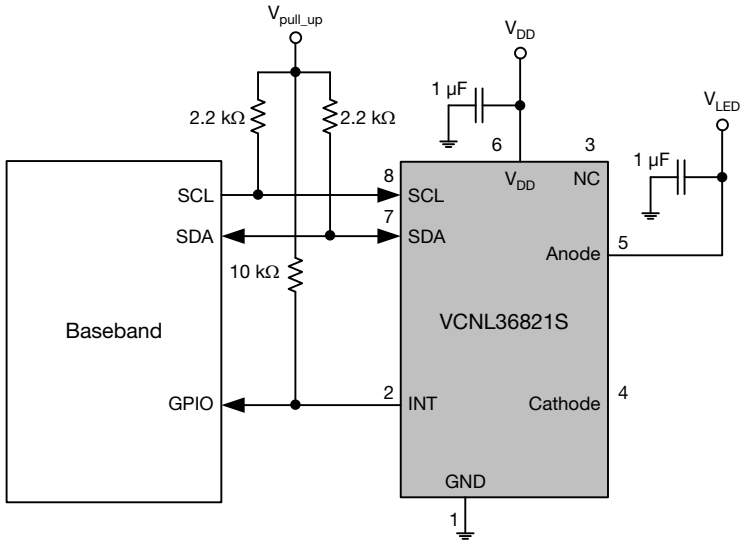


Fig. 8 - Hardware Pin Connection Diagram

Digital Interface

VCNL36821S applies single slave address 0x60 (HEX) of 7-bit addressing following I²C protocol. All operations can be controlled by the command register. The simple command structure helps users easily program the operation setting and latch the light data from VCNL36821S. As Fig. 9 shows, VCNL36821S's I²C command format is simple for read and write operations between VCNL36821S and the host. The white sections indicate host activity and the gray sections indicate VCNL36821S's acknowledgement of the host access activity. Write word and read word protocol is suitable for accessing registers particularly for 12-bit PS data. Interrupt can be cleared by reading data out from register: INT_Flag. All command codes should follow read word and write word protocols.



Fig. 9 - Write Word and Read Word Protocol

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Function Description

VCNL36821S supports different kinds of mechanical designs to achieve the best proximity detection performance for any color of object with more flexibility. The basic PS function settings, such as duty ratio, integration time, interrupt, and PS enable / disable and persistence, are handled by the register: PS_CONF2_LOW. Duty ratio controls the PS response time. Integration time represents the duration of the energy being received. The interrupt is asserted when the PS detection levels over the high threshold level setting (register: PS_THDH) or lower than low threshold (register: PS_THDL). If the interrupt function is enabled, the host reads the PS output data from VCNL36821S that saves host loading from periodically reading PS data. More than that, INT flag (register: INT_Flag) indicates the behavior of INT triggered under different conditions. PS persistence (PS_PERS) sets up the PS INT asserted conditions as long as the PS output value continually exceeds the threshold level. The intelligent cancellation level can be set on register: PS_CANC to reduce the cross talk phenomenon.

A smart persistence (register: PS_SMART_PERS) is provided to get faster PS response time and prevent false trigger for PS.

TABLE 1 - COMMAND CODE AND REGISTER DESCRIPTION

COMMAND CODE	DATE BYTE LOW / HIGH	REGISTER NAME	R / W	DEFAULT VALUE	FUNCTION DESCRIPTION
0x00	L	PS_CONF1_LOW	R / W	0x01	Standby and on / off
	H	PS_CONF1_HIGH	R / W	0x00	Standby and on / off
0x03	L	PS_CONF2_LOW	R / W	0x01	PS period, persistence, interrupt, smart persistence and PS start / stop
	H	PS_CONF2_HIGH	R / W	0x00	PS integration time, multi pulse and interrupt function
0x04	L	PS_CONF3	R / W	0x00	PS force mode and sunlight light protect interrupt setting
	H	PS_CONF4	R / W	0x00	PS LED current
0x05	L	PS_THDL	R / W	0x00	PS low interrupt threshold setting
	H	PS_THDL	R / W	0x00	PS low interrupt threshold setting
0x06	L	PS_THDH	R / W	0x00	PS high interrupt threshold setting
	H	PS_THDH	R / W	0x00	PS high interrupt threshold setting
0x07	L	PS_CANC_L	R / W	0x00	PS cancellation LSB setting
	H	PS_CANC_M	R / W	0x00	PS cancellation MSB setting
0x08	L	PS_AC_L	R / W	0x00	PS auto-calibration period, number, interrupt setting
	H	PS_LPPERI	R / W	0x00	PS low power mode setting
0xF8	L	PS_Data_L	R	0x00	PS channel LSB output data
	H	PS_Data_M	R	0x00	PS channel MSB output data
0xF9	L	Reserved	R	0x00	Reserved
	H	INT_Flag	R	0x00	PS interrupt flag
0xFA	L	ID_L	R	0x26	Device ID LSB
	H	ID_M	R	0x00	Device ID MSB
0xFB	L	PS_AC_Data_L	R	0x00	PS auto-calibration LSB data
	H	PS_AC_Data_H	R	0x00	PS auto-calibration MSB data, busy and sunlight protect

Note

- All of reserved register are used for internal test. Please keep as default setting

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Command Register Format

VCNL36821S provides an 8-bit command register for PS controlling independently. The description of each command format is shown in the following tables.

TABLE 2 - REGISTER: PS_CONF1_LOW DESCRIPTION

REGISTER NAME		COMMAND CODE: 0x00_L (0x00 DATA BYTE LOW)
Command	Bit	Description
PS_INIT	7	Must be set to “1” when power on ready
Reserved	6 : 2	Default = (0 : 0 : 0 : 0 : 0)
PS_ON	1	Set this bit = “1” to enable bias circuit **Note** • Initiallization process: step 1: set PS_ON = “1”; step 2: set PS_INIT = “1”
Reserved	0	Default = 1, must always stay = 1

TABLE 3 - REGISTER: PS_CONF1_HIGH DESCRIPTION

REGISTER NAME		COMMAND CODE: 0x00_H (0x00 DATA BYTE HIGH)
Command	Bit	Description
Reserved	7 : 2	Default = (0 : 0 : 0 : 0 : 0)
Reserved	1	Must be set to “1” when power on ready
Reserved	0	Default = 0

TABLE 4 - REGISTER: PS_CONF2_LOW DESCRIPTION

REGISTER NAME		COMMAND CODE: 0x03_L (0x03 DATA BYTE LOW)
Command	Bit	Description
PS_Period	7 : 6	(0 : 0) = 10 ms, (0 : 1) = 20 ms, (1 : 0) = 40 ms, (1 : 1) = 80 ms PS sample period setting
PS_PERS	5 : 4	(0 : 0) = 1, (0 : 1) = 2, (1 : 0) = 3, (1 : 1) = 4 PS interrupt persistence setting
PS_ INT	3 : 2	(0 : 0) = interrupt disable, (0 : 1) = logic high / low mode, (1 : 0) = first high, (1 : 1) = interrupt enable
PS_SMART_PERS	1	0 = disable PS smart persistence, 1 = enable PS smart persistence
PS_ST	0	0 = PS start, 1 = PS stop, default = 1; for active force mode set AF = 1 before setting PS_ST = 0

TABLE 5 - REGISTER: PS_CONF2_HIGH DESCRIPTION

REGISTER NAME		COMMAND CODE: 0x03_H (0x03 DATA BYTE HIGH)
Command	Bit	Description
PS_IT	7 : 6	(0 : 0) = 1T, (0 : 1) = 2T, (1 : 0) = 4T, (1 : 1) = 8T
PS_MPS	5 : 4	(0 : 0) = 1, (0 : 1) = 2, (1 : 0) = 4, (1 : 1) = 8; PS multi-pulse setting
PS_ITB	3	0: ITB = 25 µs, 1: ITB = 50 µs
PS_HG	2	0 = disable, 1 = enable, PS high gain mode
Reserved	1 : 0	Default = (0 : 0)

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TABLE 6 - REGISTER: PS_CONF3 DESCRIPTION		
REGISTER NAME		**COMMAND CODE: 0x04_L (0x04 DATA BYTE LOW)**
Command	Bit	Description
Reserved	7	Default = 0
PS_AF	6	0 = auto mode; 1 = force mode
PS_FOR_Trig	5	0 = no PS active force mode trigger, 1 = trigger one time cycle VCNL36821S output one cycle data every time host writes in “1” to sensor. The state returns to “0” automatically
PS_FORCENUM	4	0 = one detect cycle after trigger, 1 = two detect cycle after trigger
Reserved	3	When use PS function, must write “1”
PS_SP_INT	2	0 = disable, 1 = enable, PS sunlight light protect INT setting
Reserved	1 : 0	Reserved

TABLE 7 - REGISTER: PS_CONF4 DESCRIPTION		
REGISTER NAME		**COMMAND CODE: 0x04_H (0x04 DATA BYTE HIGH)**
Command	Bit	Description
PS_SC	7 : 5	Default = (0 : 0 : 0), with all 3 bit = “1”, (1 : 1 : 1), sunlight cancellation is enabled
Reserved	4	Default = 0
LED_I	3 : 0	(1 : 0 : 0 : 0) = 50 mA; (1 : 0 : 0 : 1) = 66 mA; (1 : 0 : 1 : 0) = 82 mA; (1 : 0 : 1 : 1) = 98 mA; (1 : 1 : 0 : 0) = 114 mA; (1 : 1 : 0 : 1) = 130 mA; (1 : 1 : 1 : 0) = 144 mA; (1 : 1 : 1 : 1) = 156 mA; LED current selection setting

TABLE 8 - REGISTER: PS_THDL DESCRIPTION		
REGISTER NAME		**COMMAND CODE: 0x05_L (0x05 DATA BYTE LOW) AND 0x05_H (0x05 DATA BYTE HIGH)**
Command	Bit	Description
PS_THDL	7 : 0	0x00 to 0xFF, PS interrupt low threshold setting
PS_THDL	3 : 0	0x00 to 0x0F, PS interrupt low threshold setting

TABLE 9 - REGISTER: PS_THDH DESCRIPTION		
REGISTER NAME		**COMMAND CODE: 0x06_L (0x06 DATA BYTE LOW) AND 0x06_H (0x06 DATA BYTE HIGH)**
Command	Bit	Description
PS_THDH	7 : 0	00H to FFH, PS interrupt high threshold setting
PS_THDH	3 : 0	00H to 0FH, PS interrupt high threshold setting

TABLE 10 - REGISTER: PS_CANC DESCRIPTION		
REGISTER NAME		**COMMAND CODE: 0x07_L (0x07 DATA BYTE LOW) AND 0x07_H (0x07 DATA BYTE HIGH)**
Command	Bit	Description
PS_CANC_L	7 : 0	0x00 to 0xFF, PS intelligent cancellation level setting
PS_CANC_H	3 : 0	0x00 to 0x0F, PS intelligent cancellation level setting

TABLE 11 - REGISTER: PS_AC DESCRIPTION		
REGISTER NAME		**COMMAND CODE: 0x08_L (0x08 DATA BYTE LOW)**
Command	Bit	Description
PS_AC_PERIOD	7 : 6	(0 : 0) = 3 ms, (0 : 1) = 6 ms, (1 : 0) = 12 ms, (1 : 1) = 24 ms; PS auto-calibration detect sample period setting
PS_AC_NUM	5 : 4	(0 : 0) = 1, (0 : 1) = 2, (1 : 0) = 4, (1 : 1) = 8; PS auto-calibration detect sample number setting
PS_AC	3	0 = disable, 1 = enable; PS auto-calibration enable; need set PS_AF = 1
PS_AC_TRIG	2	0 = disable, 1 = enable; trigger one time auto-calibration
Reserved	1	Reserved
PS_AC_INT	0	0 = disable, 1 = enable; PS auto-calibration INT setting

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TABLE 12 - REGISTER: PS_LP DESCRIPTION		
REGISTER NAME		**COMMAND CODE: 0x08_H (0x08 DATA BYTE HIGH)**
Command	Bit	Description
Reserved	7 : 3	Default = (0 : 0 : 0 : 0 : 0)
PS_LPPER	2 : 1	(0 : 0) = 40 ms, (0 : 1) = 80 ms, (1 : 0) = 160 ms, (1 : 1) = 320 ms; PS detection period setting at low power mode (PS_LPEN = 1)
PS_LPEN	0	0 = disable, 1 = enable = starts proximity low power measurements; now PS_LPPER used as periode, but LED_I, PS_IT, PS_ITB, PS_MPS as defined within register 3 and register 4

TABLE 13 - READ OUT REGISTER DESCRIPTION			
Register	Command Code	Bit	Description
PS_Data_L	0xF8_L (0xF8 data byte low)	7 : 0	0x00 to 0xFF, PS output data
PS_Data_M	0xF8_H (0xF8 data byte high)	3 : 0	0x00 to 0x0F, PS output data
INT_Flag	0xF9_H (0xF9 data byte high)	7 : 6 5 4 3 2 1 0	Reserved PS_ACFLAG, after PS finishing auto-calibration, INT raise PS_SPFLAG, PS entering protection mode Reserved Reserved PS_IF_CLOSE, PS rises above PS_THDH INT trigger event PS_IF_AWAY, PS drops below PS_THDL INT trigger event
ID_L	FAH_L (FAH data byte low)	7 : 0	Default = 0010 0110, device ID LSB byte
ID_M	FAH_H (FAH data byte high)	7 : 6 5 : 4 3 : 0	(0 : 0) (0 : 0) slave address = 0x60 Version code (0 : 0 : 0 : 0) device ID MSB byte
PS_AC_Data_L	0xFB_L (0xFB data byte low)	7 : 0	0x00 to 0xFF, PS auto-calibration data (LSB)
PS_AC_Data_H	0xFB_H (0xFB data byte high)	7 6 5 : 4 3 : 0	AC_BUSY, when AC, the bit will be “1” AC_SUN, PS enters sunlight protect during auto-calibration Reserved 0x00 to 0xFF, PS auto-calibration data (MSB)

Initialization

VCNL36821S includes default values for each register. As long as power is on, it is ready to be controlled by host via I^2C bus.

Proximity Interrupt

There are three different Interrupt methods: “normal” interrupt mode, first high mode and so-called “logic high / low” mode.

The first high mode is selected by setting (0x03_L, bit 3:2 = 1:0) within register PS_CONF2_LOW. In this mode, the initial interrupt that is triggered needs to be with regard to the high threshold (PS_THDH). Passing underneath the low threshold will have no effect until the first high threshold event has occurred. In this mode, the interrupt event will remain set, until it is cleared, by reading the interrupt register.

The “normal” interrupt mode is selected with PS_INT = interrupt enabled (0x03_L, bit 3 : 2 = 1 : 1) within register PS_CONF2_LOW.

Tests with ready-made application will show where to set the value for high threshold (PS_THDH) and low threshold (PS_THDL). For more information and explanation please study also the application note www.vishay.com/doc?80178.

The “logic high / low” mode is selected with PS_INT = trigger by logic high/low mode (0x03_L, bit 3 : 2 = 0 : 1) within register PS_CONF2_LOW. When this mode is selected, the interrupt pin is pulled low when the proximity counts reach the programmed high threshold (PS_THDH) and will return to high level when counts drop below the count value for low threshold (PS_THDL).

With help of the function PS persistence one may also improve a reliable detection that not just one short event directly triggers an interrupt, but only when 2 (or up to 4) consecutive proximity measurements are above the programmed threshold value the interrupt will be set; please see also within the application note www.vishay.com/doc?80178.

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PROXIMITY LOW POWER CONSUMPTION MODE

While register PS_LPEN set to 1, proximity sensor operates in a special low power consumption mold offering significant lower power consumption of just 17.6 µA with response time of 320 ms for proximity detection that is a remarkable feature for any fuctions required a lower power consumtion operations and did not want to always request one proximity measurement with proximity force mode (PS_AF and PS_TRIG).

PS period (ms)	10	20	40	80	160	320
Normal mode (µA)	2794	1492	841	515	n/a	n/a
Low power mode (µA)	n/a	n/a	106	56	30	17.6

Notes

- IR LED = 130 mA, PS_IT = x 4, PS_ITB = 50 µs
- While register PS_LPEN = 1, proximity sensor

PROXIMITY DETECTION HYSTERESIS

A PS detection hysteresis is important that keeps PS state in a certain range of detection distance. For example, PS INT asserts when PS value over PS_THDH. Host switches off panel backlight and then clears INT. When PS value is less than PS_THDL, host switches on panel backlight. Any PS value lower than PS_THDH or higher than PS_THDL, PS INT will not be asserted. Host does keep the same state.

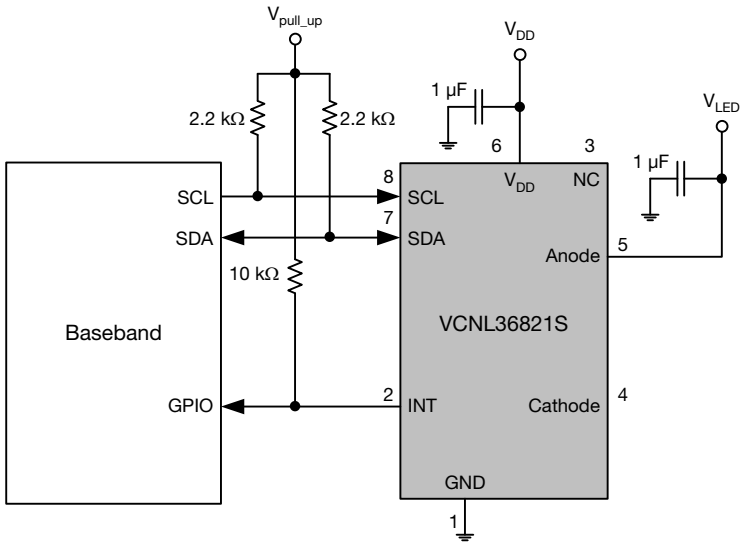
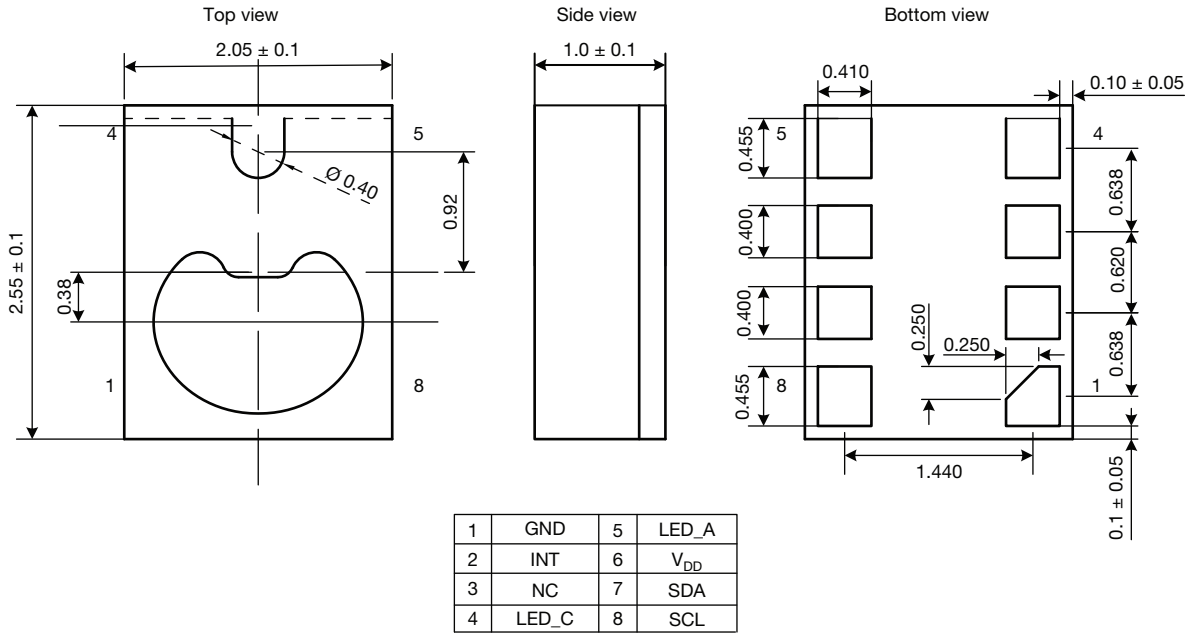


Fig. 10 - VCNL36821S Reference Circuit Connection With Host (proximity detection logic output mode)
(VCNL36821S INT pin connecting to BB GPIO instead of INT pin)

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PACKAGE INFORMATION in millimeters



1	GND	5	LED_A
2	INT	6	V_{DD}
3	NC	7	SDA
4	LED_C	8	SCL

Fig. 11 - VCNL36821S Package Dimensions

LAYOUT PAD INFORMATION in millimeters

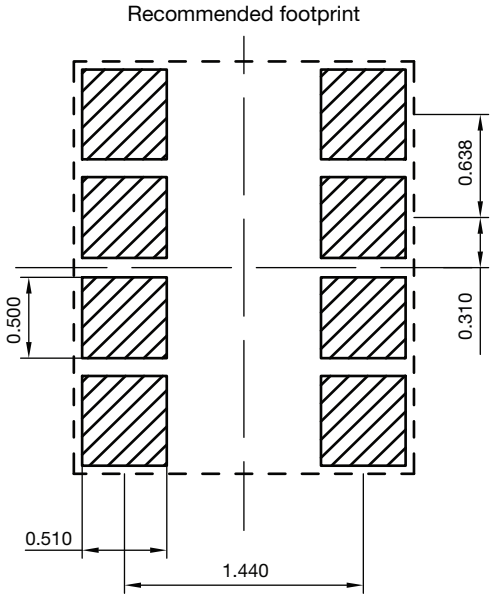


Fig. 12 - VCNL36821S PCB Layout Footprint

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APPLICATION CIRCUIT BLOCK REFERENCE

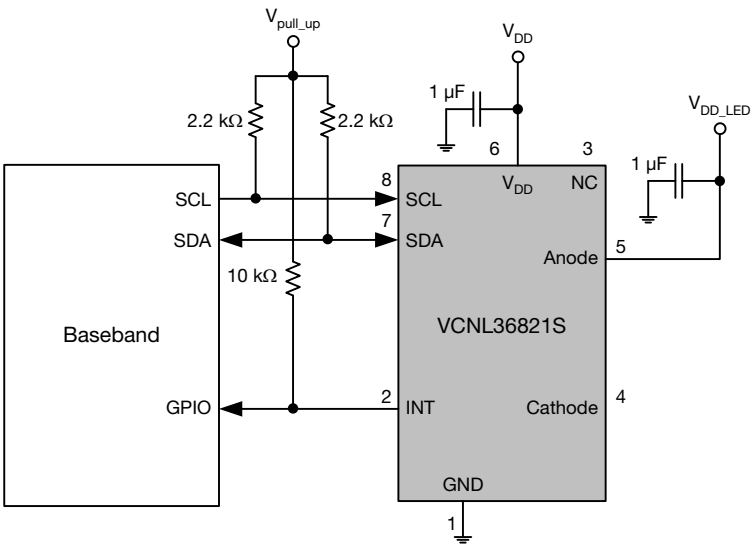


Fig. 13 - VCNL36821S Application Circuit

RECOMMENDED STORAGE AND REBAKING CONDITIONS				
PARAMETER	**CONDITIONS**	**MIN.**	**MAX.**	**UNIT**
Storage temperature		5	50	°C
Relative humidity		-	60	%
Open time		-	168	h
Total time	From the date code on the aluminized envelope (unopened)	-	12	months
Rebaking	Tape and reel: 60 °C	-	22	h
	Tube: 60 °C	-	22	h

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RECOMMENDED INFRARED REFLOW

Soldering conditions which are based on J-STD-020 C

IR REFLOW PROFILE CONDITION			
PARAMETER	**CONDITIONS**	**TEMPERATURE**	**TIME**
Peak temperature		260 °C + 5 °C / - 5 °C (max.: 265 °C)	10 s
Preheat temperature range and timing		150 °C to 200 °C	60 s to 180 s
Timing within 5 °C to peak temperature		-	10 s to 30 s
Timing maintained above temperature / time		217 °C	60 s to 150 s
Timing from 25 °C to peak temperature		-	8 min (max.)
Ramp-up rate		3 °C/s (max.)	-
Ramp-down rate		6 °C/s (max.)	-

Recommend Normal Solder Reflow is 235 °C to 265 °C

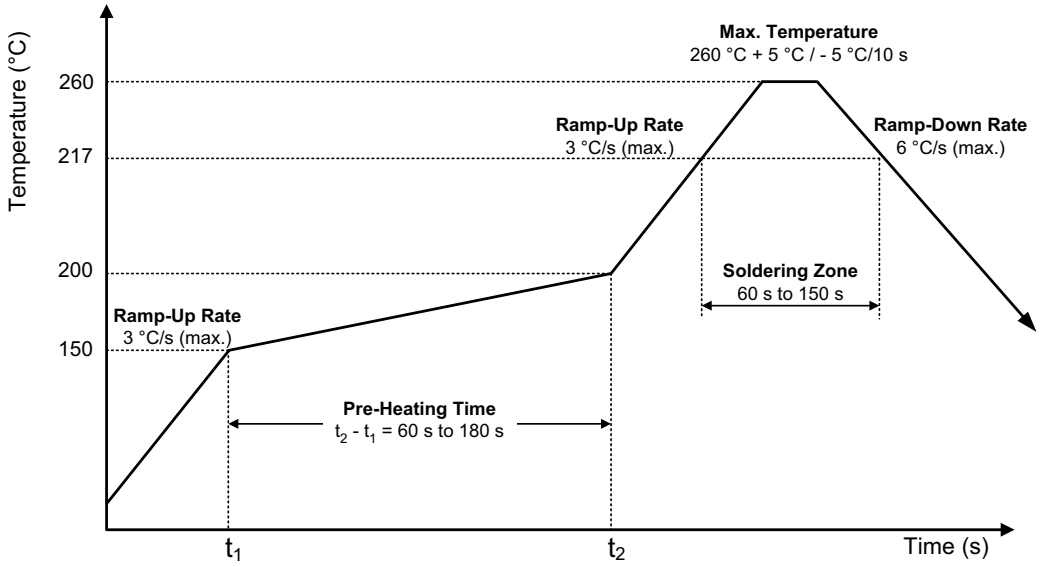


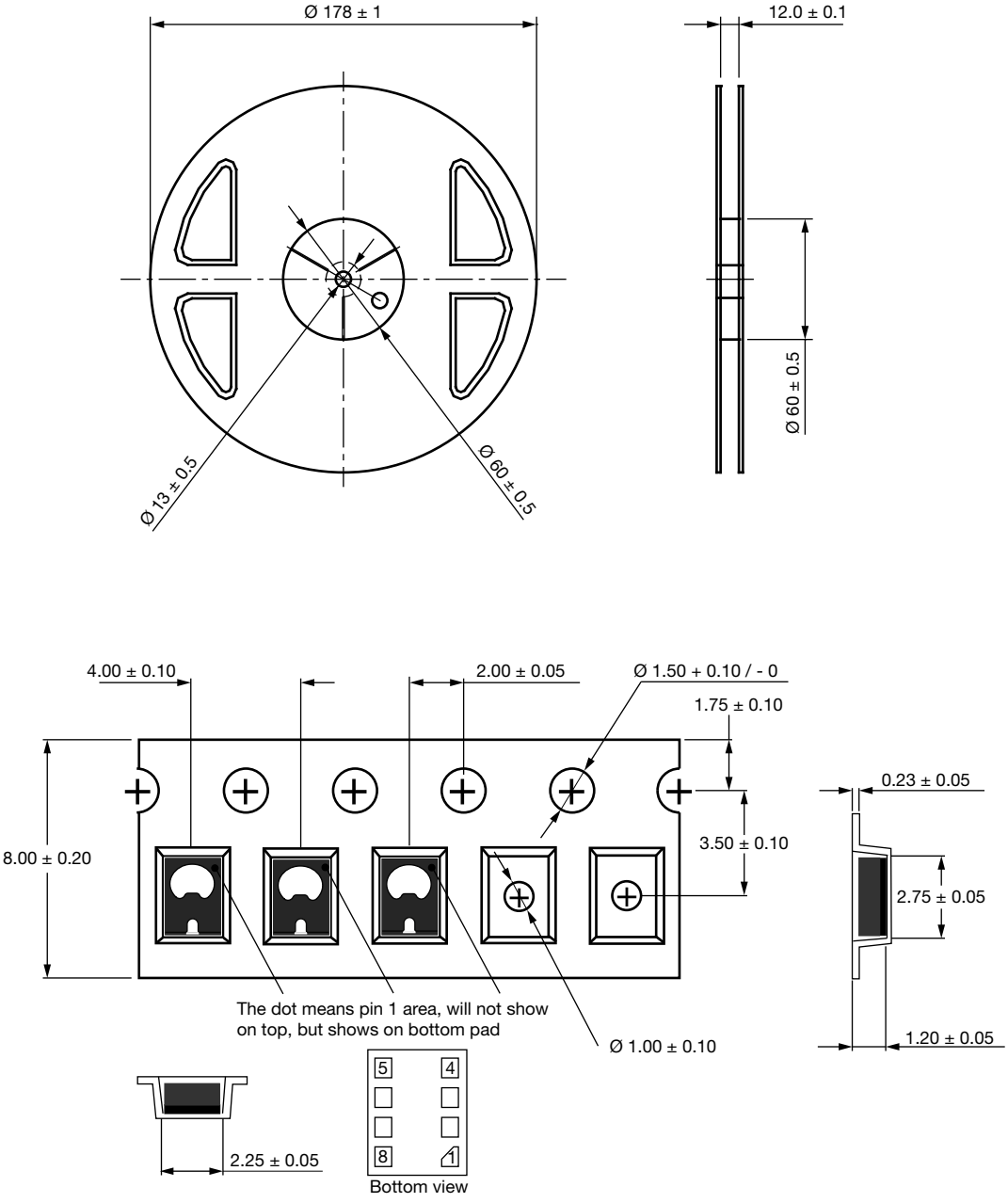
Fig. 14 - VCNL36821S Solder Reflow Profile Chart

RECOMMENDED IRON TIP SOLDERING CONDITION AND WARNING HANDLING

1. Solder the device with the following conditions:
   1.1. Soldering temperature: 400 °C (max.)
   1.2. Soldering time: 3 s (max.)
2. If the temperature of the method portion rises in addition to the residual stress between the leads, the possibility that an open or short circuit occurs due to the deformation or destruction of the resin increases
3. The following methods: VPS and wave soldering, have not been suggested for the component assembly
4. Cleaning method conditions:
   4.1. Solvent: methyl alcohol, ethyl alcohol, isopropyl alcohol
   4.2. Solvent temperature < 45 °C (max.)
   4.3. Time: 3 min (min.)

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TAPE PACKAGING INFORMATION in millimeters



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