XB112 Breakout Board Product Brief

XB112 Breakout Board Product Brief

Proprietary and Confidential

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1 Introduction

This document describes the Acconeer XB112 breakout board for the XM112 module. It has been designed with the purpose of flashing, debugging and supplying power to the Acconeer XM112 Module.

For More information please read:

- XM112 Data Sheet
- XM112 Module Evaluation Kit User Guide

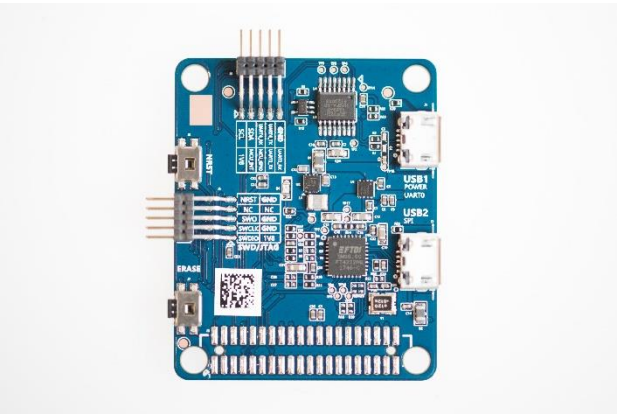
2 XB112 Breakout Board

2.1 Overview

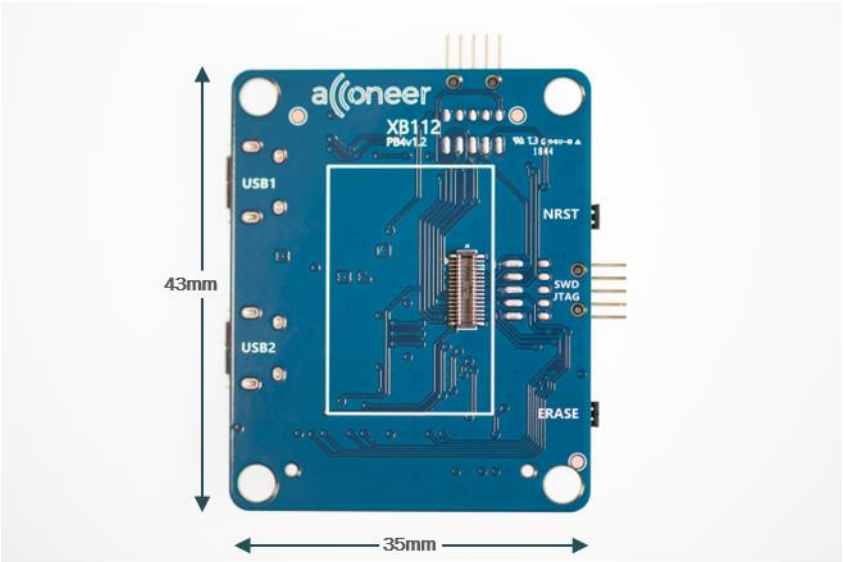
The XB112 breakout board for the XM112 module is designed to make the interfaces from the XM112 module accessible for evaluation and debug. It also enables flashing of the XM112 via USB-UART or SW-DP. The XM112 is connected to the XB112 via a board-to-board connector on the top side of the PCB.

In addition to the board-to-board connector for the XM112, the XB112 comprises two USB connectors, two 2x5 pin headers and one not mounted 2x20 pin header. There are two buttons that are to be used when flashing via USB-UART. The buttons control the pins “ERASE” and “NRST” on the MCU on the XM112. A dual LDO, a switched power regulator and two FTDI chips that converts USB into UART and SPI are also available on the board.

The pictures below shows the XB112 radar module breakout board. The leftmost picture shows the front side of the XB112, with the board-to-board connector for the XM112 module, and the rightmost picture shows the reverse side of the XB112.



The picture below shows the dimensions of the XB112.



The thickness of the PCB is 1.2 mm.

The block diagram of XB112 is found in Figure 1 below.

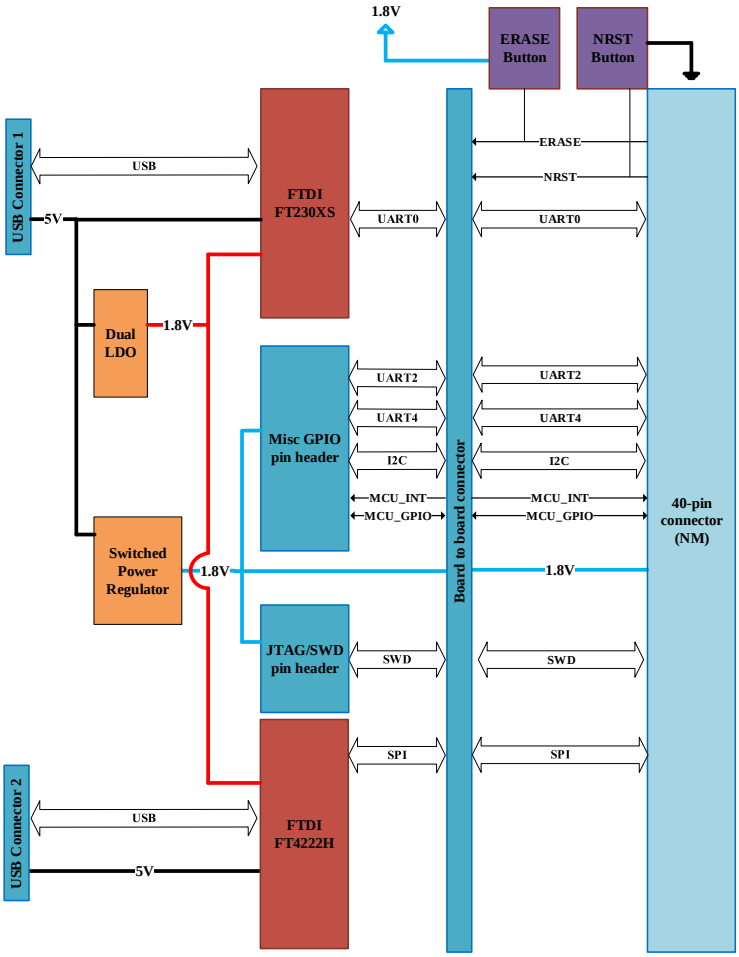


Figure 1. The block diagram of XB112 radar module breakout board.

2.2 Power

The XB112 is powered via the USB connectors. USB1 powers the USB-UART chip (U4) and the XM112. USB2 powers the USB-SPI chip (U5). If no SPI data is needed, the USB2 can be left unconnected. USB1 must however always be connected. If the USB-UART interface is not used, a dedicated USB charger can be inserted to USB1.

When the power LED on the XB112 is lit, the Breakout board and the XM112 module (if connected to the board-to-board connector on the top side of XB112) are powered on and ready for use.

The 5V from the USB1 connector is supplied directly to the USB-UART chip 5V input. It also powers a dual LDO (Low DropOut power regulator) that generates 1.8V for the USB-UART and USB-SPI chip GPIOs as well as a switched power regulator which generates 1.8V that supplies XM112 via the board-to-board connector J4.

The ENABLE signal of the switched power regulator (U2) is controlled by GPIOs on the USB-UART chip FT230XS. As shown in Figure 2, the GPIOs “CBUS0” and “CBUS1” are connected to a NAND

gate (U3) which in turn enables the switched power regulator. “CBUS0” is configured as “BCDCHARGER#” and “CBUS1” is configured as “PWREN#” as default.

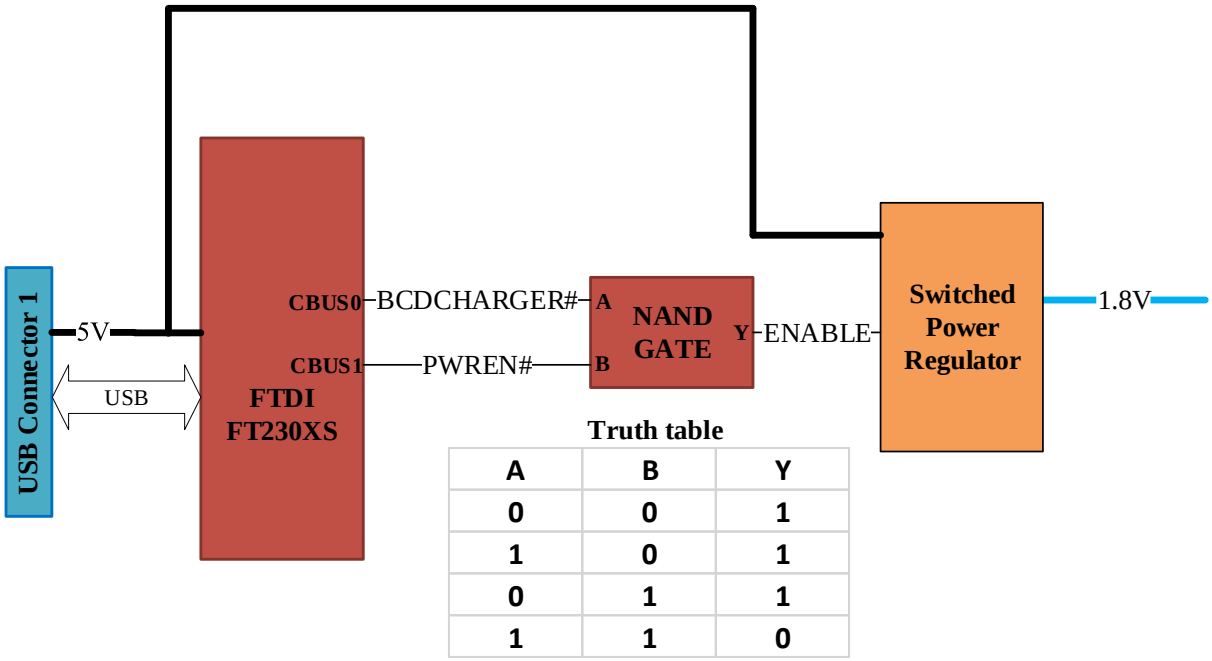


Figure 2. Block Diagram showing the logic control of the Switched Power Regulator ENABLE signal.

“BCDCHARGER#” will output a logic “0” if a USB Dedicated Charger is detected on USB1. This means that the XB112 can be powered from a USB Dedicated Charger if no data is to be sent on USB1. “PWREN#” will output a logic “0” as soon as the FT230XS has been configured by the USB host. This prevents the switched power regulator from being activated and drawing too much current during USB enumeration of FT230XS. For details regarding the configuration of FT230XS refer to chapter 2.5.

The 5V from the USB2 connector only supplies the USB-SPI chip 5V input.

2.3 Connectors

2.3.1 USB1 (J1)

USB1 is used as power supply for the XB112 and the XM112 as well as for flashing and communicating over UART. USB1 is connected to the FTDI chip FT230XS which converts the UART interface from XM112 into USB signals. The pinout of USB1 is shown in Table 1.

Table 1. The pinout of J1.

Pin Number	Signal
1	VBUS
2	D-
3	D+
4	ID (GND)
5	GND

2.3.2 USB2 (J2)

USB2 is used for high speed data output from the module SPI interface. It is converted to USB via the FTDI chip FT4222H. The pinout of USB2 is shown in Table 2.

Table 2. The pinout of J2.

Pin Number	Signal
1	VBUS
2	D-
3	D+
4	ID (GND)
5	GND

2.3.3 2x20 pin header (J3)

The 2x20 pin header (1.27mm pitch) is not mounted. The reason is that it is intended for Acconeer internal use only. All the interfaces available in the 2x20 pin header are also available in the other connectors. The pinout of the 2x20 pin header is shown in Table 3.

Table 3. The pinout of J3.

Pin Number	Signal	Pin Number	Signal
1	NC	2	ERASE
3	GND	4	GND
5	NC	6	UART0_RX_TX
7	SPI_MOSI	8	UART0_TXRX
9	SPI_MISO	10	GND
11	GND	12	SPI_CLK
13	SPI_SS	14	GND
15	NC	16	TRACESWO
17	GND	18	SWDCLK
19	GND	20	GND
21	GND	22	GND
23	GND	24	1V8
25	GND	26	GND
27	GND	28	MCU_GPIO
29	GND	30	MCU_INT
31	GND	32	GND
33	GND	34	SWDIO
35	GND	36	NRST
37	GND	38	1V8
39	NC	40	GND

2.3.4 30 pin board-to-board connector (J4)

The 30-pin board-to-board connector is intended to connect the XM112 to the XB112. The pinout is found in Table 4.

Table 4. The pinout of J4.

Pin Number	Signal	Pin Number	Signal
1	SPI_CLK	2	GND
3	GND	4	1V8
5	SPI_MOSI	6	1V8
7	GND	8	GND
9	SPI_MISO	10	MCU_GPIO
11	GND	12	UART4_TXRX[1]
13	SPI_SS	14	UART4_RXTX[1]
15	GND	16	ERASE
17	UART0_TXRX[1]	18	NRST (SWD_NRST)
19	UART0_RXTX[1]	20	SWDIO
21	GND	22	TRACESWO
23	UART2_TXRX[1]	24	GND
25	UART2_RXTX[1]	26	SWDCLK
27	I2C_SDA	28	GND
29	I2C_SCL	30	MCU_INT

2.3.5 2x5 JTAG/SWD pin header (J5)

The 2x5 JTAG/SWD pin header (1.27mm pitch) contains the signals needed for flashing the XM112 MCU via the SW-DP interface. The pinout matches that of the Cortex 10-pin JTAG/SWD Connector and is found in Table 5.

Table 5. The pinout of J5.

Pin Number	Signal	Pin Number	Signal
1	1.8V	2	SWDIO
3	GND	4	SWDCLK
5	GND	6	TRACESWO
7	NC	8	NC
9	GND	10	NRST

[1] The first two letters in the part of the signal name that is following the "_" character indicate the direction of the UART on the external host. The last two letters of the signal name that is following the "_" character indicate the direction of the UART on the XM112 MCU.

2.3.6 2x5 pin header (J6)

The 2x5 pin header (1.27mm pitch) contains miscellaneous 1.8V signals from the XM112. The pinout is found in Table 6.

Table 6. The pinout of J6.

Pin Number	Signal	Pin Number	Signal
1	1.8V	2	I2C_SCL
3	MCU_INT	4	I2C_SDA
5	MCU_GPIO	6	UART4_TXRX[1]
7	UART2_RXTX[1]	8	UART4_RXTX[1]
9	UART2_TXRX[1]	10	GND

2.4 Buttons

There are two buttons on the XB112. J7 controls the signal “ERASE” from XM112 and J8 controls “NRST” from the XM112. In Table 7 the state of the buttons and the corresponding signal states are listed.

Table 7. The states of the buttons J7 and J8.

Button	Open (default)	Closed
J7	ERASE=0	ERASE=1
J8	NRST=1	NRST=0

2.5 FTDI FT230XS USB-UART (U4)

The FT230XS is a USB 2.0 Full Speed compatible USB to serial UART converter. It is integrated on the XB112 to enable communication with the XM112 UART0 via USB interface. USB1, connector J1, is connected to FT230XS. For details regarding the FT230XS refer to the datasheet [1]. For details regarding how to use the XB112 to communicate with XM112, refer to the XB112_XM112 User Guide.

The connections of the FT230XS UART interface pins are described in Table 8.

Table 8. The FT230XS UART interface pins.

FT230XS Pin Name	XB112 Connection	Comment
TXD	UART0_TXRX	Connected to XM112 UART0_RX
RXD	UART0_RXTX	Connected to XM112 UART0_TX
RTS	TP4	Available on test point
CTS	TP5	Available on test point

Except for the UART interface there are four GPIOs on the FT230XS. The usage and XB112 default configuration of the GPIOs are listed in Table 9. The GPIOs can be flashed via the USB interface by using the program FTPROG from FTDI. For details, refer to the FT230XS datasheet [1].

Table 9. The FT230XS GPIOs.

FT230XS Pin Name	XB112 Usage	Comment
CBUS0	BCDCHARGER#	Will output “0” if a USB dedicated charger is detected on USB1.
CBUS1	PWREN#	Will output “0” when the FT230XS has been configured by the USB host. Will output “1” during USB enumeration of FT230XS and if the USB host goes into suspend mode.
CBUS2	GPIO driving low, available on testpoint	For future use. Could be reconfigured via FT Prog.
CBUS3	GPIO tristate, available on testpoint	For future use. Could be reconfigured via FT Prog.

2.6 FTDI FT4222H USB-SPI

A FT4222H USB-SPI chip is mounted on the XB112 and connected to USB2. It makes SPI data from XM112 available on the USB2 interface.

The connections of the FT4222H SPI interface pins are described in Table 10.

Table 10. The FT4222H SPI interface.

FT4222H Pin Name	XB112 Connection	Comment
SCK	SPI_CLK	Connected to SPI0_SPCK on ATSAME70 on XM112.
MISO	SPI_MISO	Connected to SPI0_MISO on ATSAME70 on XM112.
MOSI	SPI_MOSI	Connected to SPI0_MOSI on

FT4222H Pin Name	XB112 Connection	Comment
		ATSAME70 on XM112.
SS0O	SPI_SS	Connected to SPI0_NPCS0 on ATSAME70 on XM112.

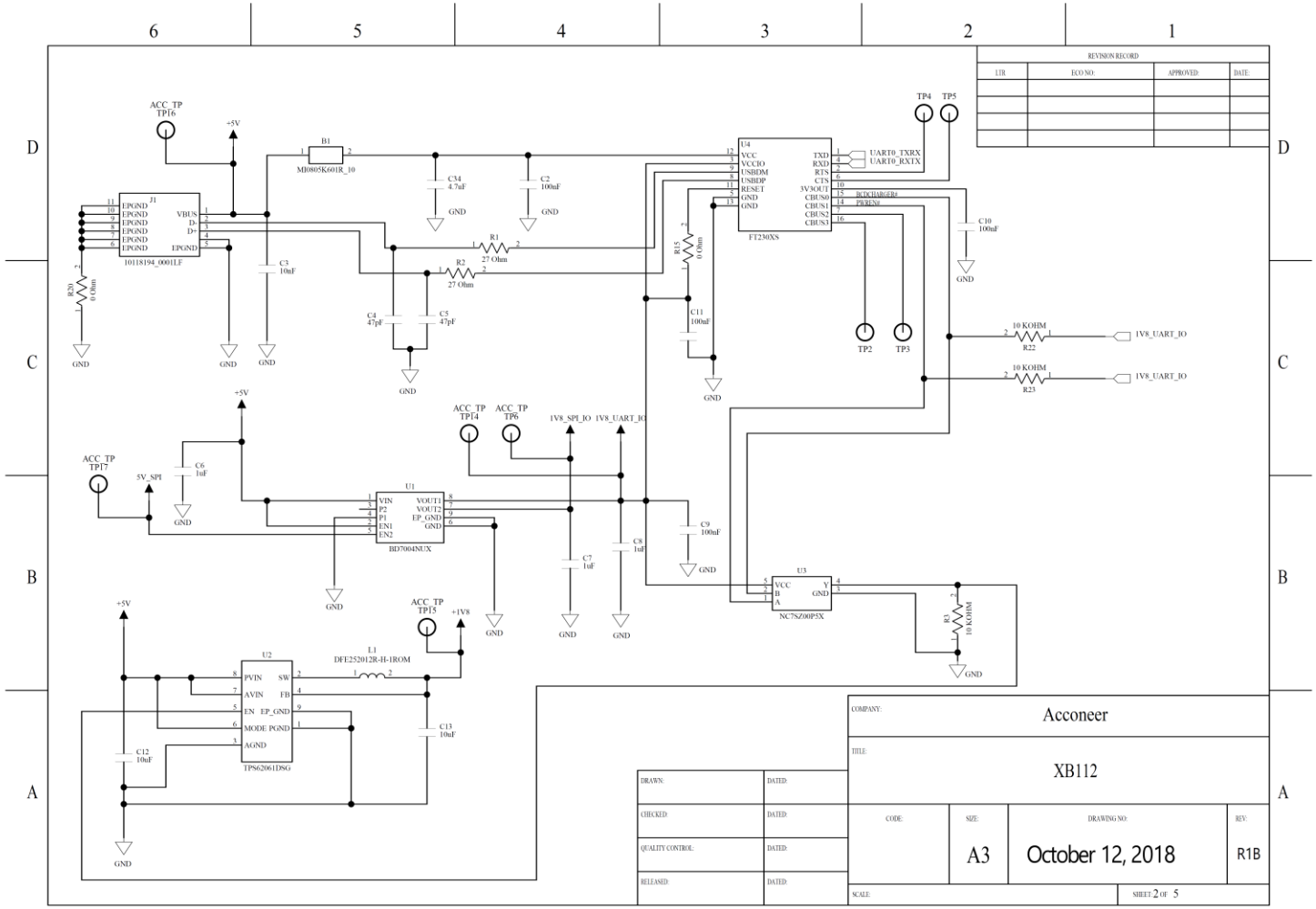
Except for the SPI interface there are four GPIOs on the FT4222H. The usage and XB112 default configuration of the GPIOs are listed in Table 11. The GPIOs can be controlled via an API provided by FTDI. For details regarding the FT4222H GPIO control, refer to the datasheet [2].

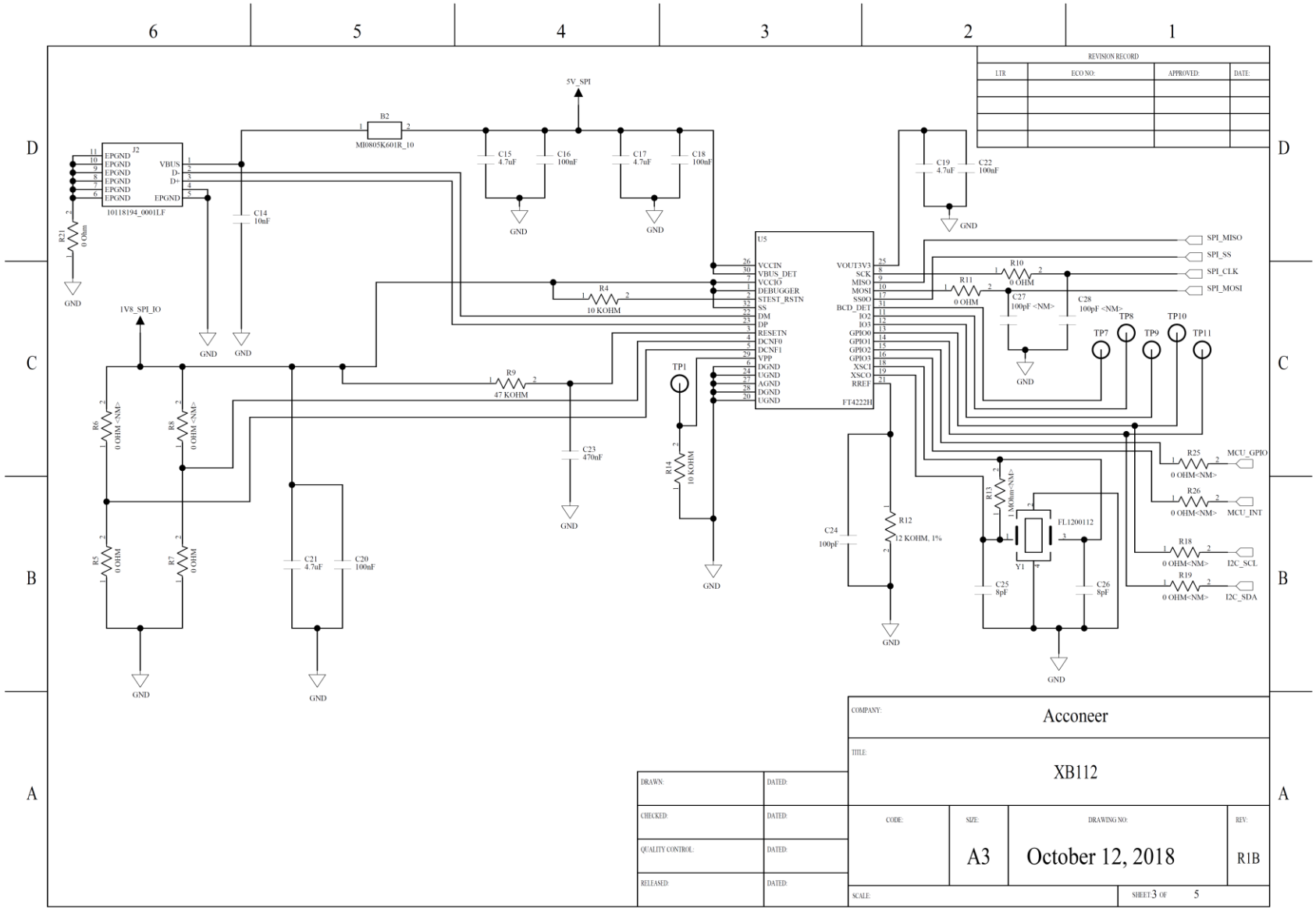
Table 11. The FT4222H GPIOs.

FT4222H Pin Name	XB112 Usage	Comment
GPIO0	Not used	Could be connected to XM112 I2C_SCL if 0 Ohm resistor, R18, is mounted.
GPIO1	Not used	Could be connected to XM112 I2C_SDA if 0 Ohm resistor, R19, is mounted.
GPIO2	Not used	Could be connected to XM112 MCU_GPIO if 0 Ohm resistor, R25, is mounted.
GPIO3	Not used	Could be connected to XM112 MCU_INT if 0 Ohm resistor, R26, is mounted.

2.7 Electrical Schematics

The electrical schematics for the XB112 are found on the following pages:

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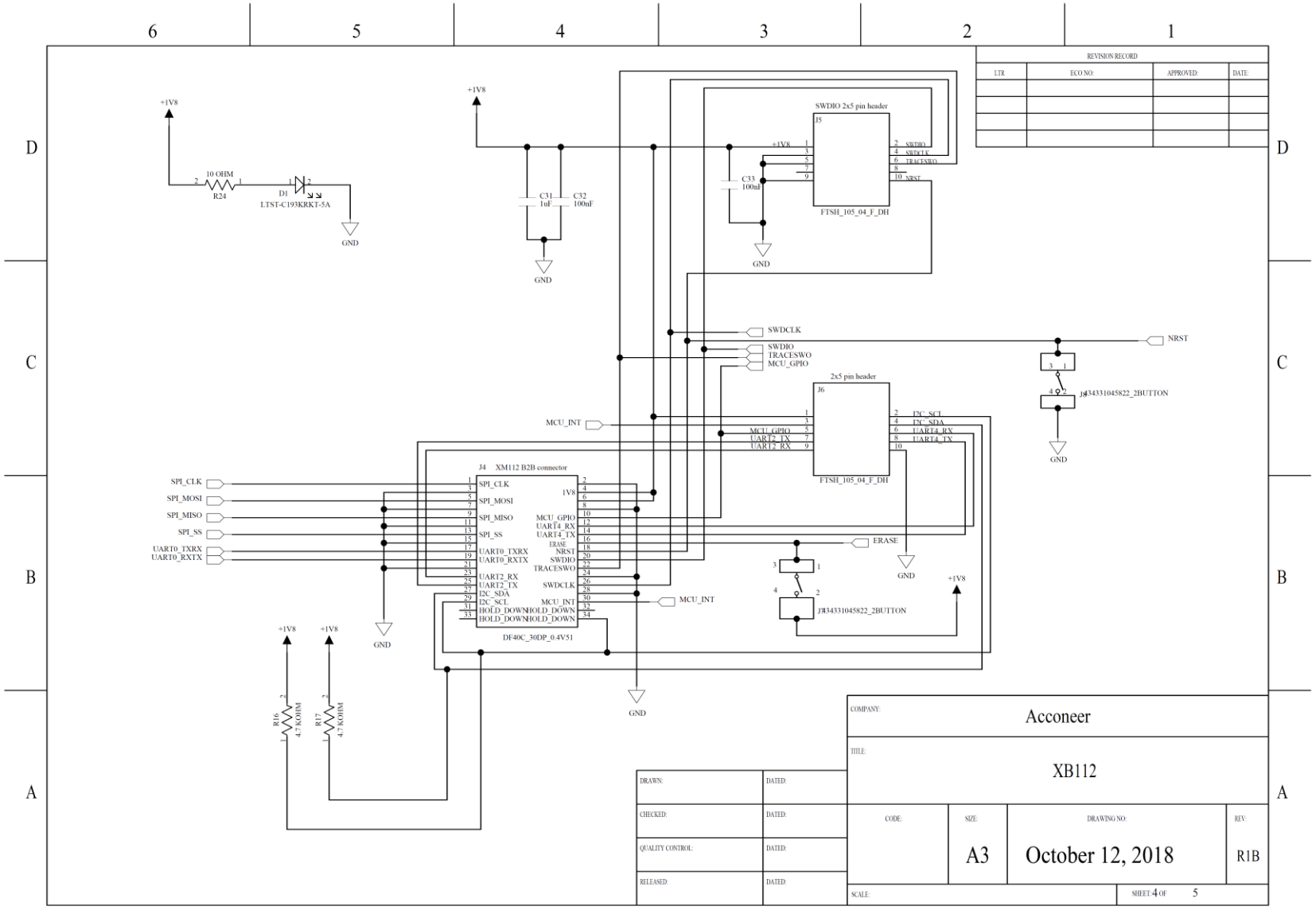
APPROVED:
DATE:
5V_SPI
B2
MI0805K601R_10
J2
10118194_0001LF
EPGND
VBUS
D-
D+
C14
10nF
C15
4.7uF
C16
100nF
C17
4.7uF
C18
100nF
C19
4.7uF
C22
100nF
R21
0 Ohm
GND
1V8_SPI_IO
U5
FT4222H
VCCIN
VBUS_DET
VCCIO
DEBUGGER
STEST_RSTN
SS
DM
DP
RESETN
DCNF0
DCNF1
VPP
DGND
UGND
AGND
VOUT3V3
SCK
MISO
MOSI
SSIO
BCD_DET
IO2
IO3
GPIO0
GPIO1
GPIO2
GPIO3
XSCI
XSCO
RREF
R4
10 KOHM
R9
47 KOHM
R10
0 OHM
R11
0 OHM
C27
100pF <NM>
C28
100pF <NM>
SPI_MISO
SPI_SS
SPI_CLK
SPI_MOSI
TP1
TP7
TP8
TP9
TP10
TP11
R6
0 OHM <NM>
R8
0 OHM <NM>
R5
0 OHM
R7
0 OHM
C21
4.7uF
C20
100nF
C23
470nF
R14
10 KOHM
C24
100pF
R12
12 KOHM, 1%
R13
1 MOhm<NM>
FL1200112
Y1
C25
8pF
C26
8pF
R25
0 OHM<NM>
MCU_GPIO
R26
0 OHM<NM>
MCU_INT
R18
0 OHM<NM>
I2C_SCL
R19
0 OHM<NM>
I2C_SDA
COMPANY:
Acconeer
TITLE:
XB112
DRAWN:
DATED:
CHECKED:
DATED:
QUALITY CONTROL:
DATED:
RELEASED:
DATED:
CODE:
SIZE:
A3
DRAWING NO:
October 12, 2018
REV:
R1B
SCALE:
SHEET 3 OF 5


REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
+1V8
10 OHM
R24
D1
LTST-C193KRKT-5A
GND
C31
1uF
C32
100nF
SWDIO 2x5 pin header
J5
FTSH_105_04_F_DH
C33
100nF
SWDIO
SWDCLK
TRACESWO
NRST
SWDCLK
SWDIO
TRACESWO
MCU_GPIO
NRST
J6
2x5 pin header
FTSH_105_04_F_DH
JS343331045822_2BUTTON
MCU_INT
I2C_SCL
I2C_SDA
UART4_RX
UART4_TX
UART2_TX
UART2_RX
J4 XM112 B2B connector
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_SS
UART0_TXRX
UART0_RXTX
1V8
MCU_GPIO
UART4_RX
UART4_TX
ERASE
NRST
SWDIO
TRACESWO
UART2_RX
UART2_TX
I2C_SCL
I2C_SDA
SWDCLK
MCU_INT
HOLD_DOWN
HOLD_DOWN
DF40C_30DP_0.4V51
ERASE
R16
4.7 KOHM
R17
4.7 KOHM
COMPANY:
Acconeer
TITLE:
XB112
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DATED:
CHECKED:
QUALITY CONTROL:
RELEASED:
CODE:
SIZE:
A3
DRAWING NO:
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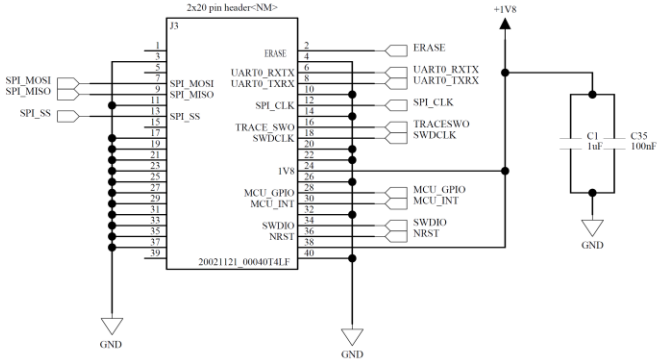
REV:
R1B
SCALE:
SHEET 4 OF 5

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



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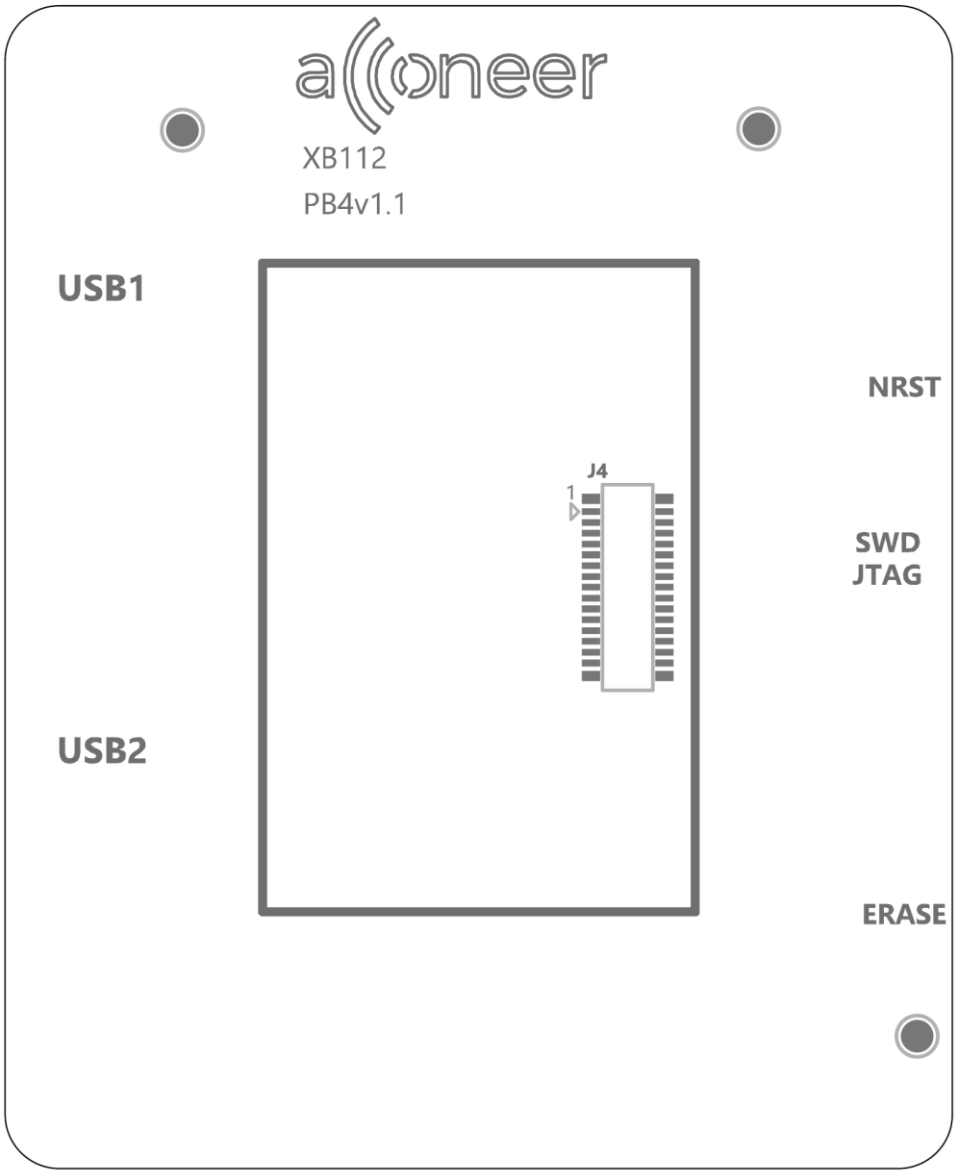
CHECKED:	DATED:	TITLE:	XB112		
QUALITY CONTROL:	DATED:	CODE:	SIZE: A3	DRAWING NO: October 12, 2018	REV: R1B
RELEASED:	DATED:	SCALE:		SHEET 5 OF 5	

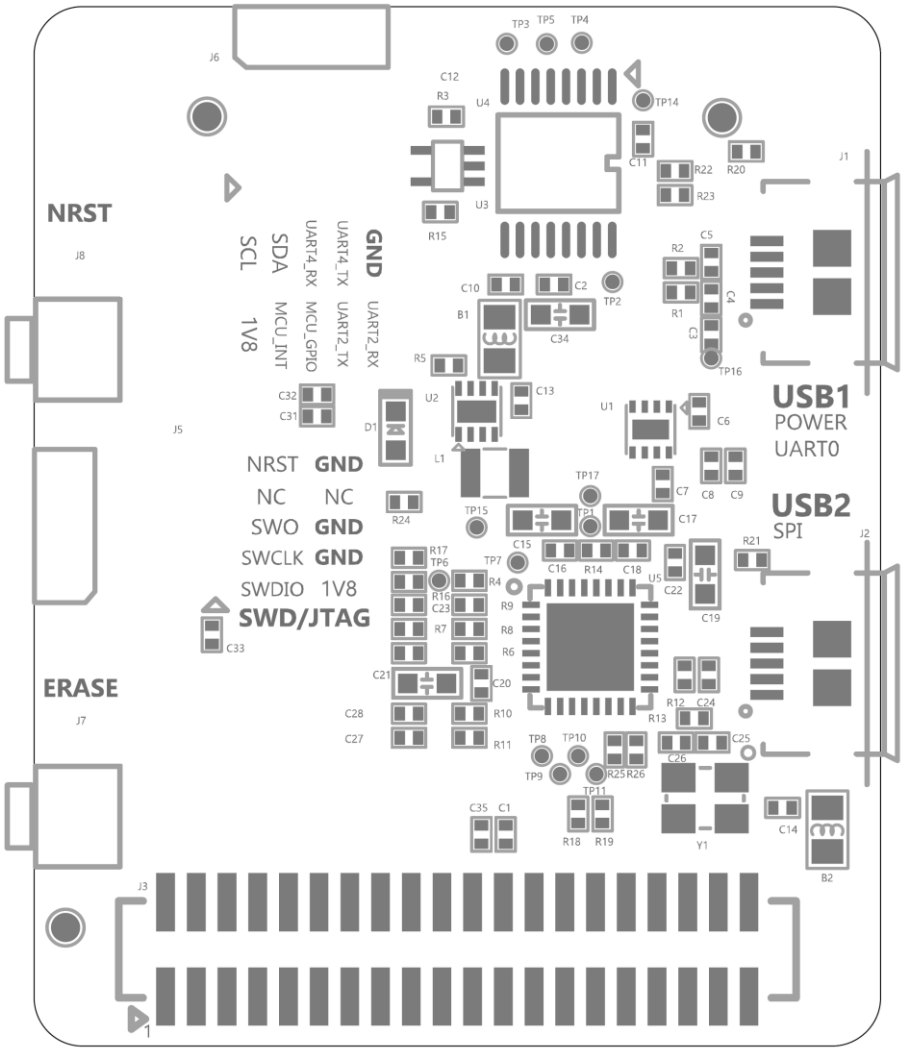
2.8 Component Placement Drawing

The component placement drawing of XB112 is found below.

Top Side:



Bottom Side:



2.9 Bill of Material

Table 12 shows the BOM for XB112.

Table 12. The BOM of XB112.

Component Ref.	Specification	QTY	Value	Comment
C2,C9,C10,C11,C16,C18,C20,C22,C32,C33,C35	100/NF/K/50V/X7R/1005	11	100nF	
C24	100/PF/J/10V/NP0,C0G/1005	1	100pF	
C3,C14	10/NF/K/16V/X7R/1005	2	10nF	
C12,C13	10/UF/M/10V/X5R/1005	2	10uF	
C1,C6,C7,C8,C31	1/UF/K/10V/X5R/1005	5	1uF	
C23	470/NF/K/10V/X5R/1005	1	470nF	
C4,C5	47/PF/J/50V/C0G/1005	2	47pF	
C25,C26	8/PF/C/50V/NP0,C0G/1005	2	8pF	
C15,C17,C19,C21,C34	1608 10% 10V X5R 4.7uF	5	4.7uF	
R5,R7,R10,R11,R15,R20,R21	1005 J 0	7	0 Ohm	
R3,R4,R14,R22,R23	1005 F 10K	5	10kOhm	
R12	1005 F 12K	1	12kOhm	Accuracy 1%
R1,R2	1005 F 27	2	27Ohm	
R9	47/KOHM/F/1005	1	47kOhm	
R16,R17	4.7/KOHM/F/1005	2	4.7kOhm	
R24	10/OHM/F/1005	1	10 Ohm	
J1,J2	10118194-0001LF/Micro B USB 2.0 Receptacle	2	N/A	Manufacturer: Amphenol
U1	BD7004NUX/Dual output 5V to 1.8V LDO	1	N/A	Manufacturer: Rohm
J4	DF40C-30DP-0.4V51/XM112 30 pin B2B connector plug	1	N/A	Manufacturer: Hirose
L1	DFE252012R-H-1ROM=p2	1	1uH	
Y1	FL1200112/CRYSTAL_12MHz	1	N/A	

U4	FT230XS-R/USB to UART bridge	1	N/A	
U5	FT4222H/USB to SPI bridge	1	N/A	
J5,J6	FTSH_105_04_F_DH/SWD Connector, Right angle 2x5 pin header	2	N/A	Manufacturer: Samtech
J7,J8	SWITCH TACTILE SPST-NO 0.05A 12 434331045822	2	N/A	Manufacturer: Wurth Electronics
B1,B2	MI0805K601R_10/Ferrite Bead	2	N/A	
U3	NC7SZ00P5X/NAND gate	1	N/A	
U2	TPS62061DSGR	1	N/A	
D1	LTST-C193KRKT-5A/LED RED	1	N/A	

References

1. FT230XS datasheet: https://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS_FT230X.pdf
2. FT4222H datasheet: https://www.ftdichip.com/Support/Documents/DataSheets/ICs/DS_FT4222H.pdf

3 Revision History

Date	Version	Changes
2018-12-19	1.0	Original Version
2021-04-21	1.1	ISO 14001 update

4 Disclaimer

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